

Harmonic Optimization of Cascade Multilevel Inverter with Unequal Dc Sources Using Genetic Algorithm

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Abstract: Multilevel inverter have been attracting increasing interest recently due to the increased power rating, improving harmonic performance, and reduced electromagnetic interference (EMI) emission. A voltage source inverter is commonly used to supply a variable frequency variable voltage to a three phase induction motor in a variable speed application. The output voltage contains harmonics the different type of harmonics elimination methods are available. But all the method having some limitations. This project deals with how to reduce the particular harmonics in the output voltage of inverter. The concept of the harmonic stepped waveform technique for the multilevel inverter to be presented. By applying this concept, selected harmonic can be eliminated, and the output voltage THD can be improved. A procedure to achieve the appropriate switching angle is to be proposed. The proposed project is to be simulated by using MATLAB and the results are to be compared with experimental setup. The ATmega Microcontroller is to be used for generating required pulses to the cascaded multilevel inverter.

Index Terms: Multilevel Inverter, Genetic Algorithm (GA), Selective Harmonic Elimination (SHE), MATLAB.

I .Introduction

Several topologies for multilevel inverters have been proposed over the years the most popular being the diode clamped, flying capacitor and cascaded H-bridge structures. One aspect which sets the cascaded H-bridge apart from other multilevel inverters is the capability of utilizing different DC voltages on the individual H-bridge cell which results in splitting the power conversion amongst higher-voltage lower-frequency and lower-voltage higher frequency inverters.

An alternate method of cascading inverters involves series connection of two three phase inverters through the neutral point of the load. An advantage of this approach is that isolated sources are not required for each phase. It should be noted that cascaded inverter system can be considered from a number of different viewpoints. Considering the cascaded inverter to be one unit, it can be seen that a higher number of voltage levels are available for a given number of semiconductor devices. Capacitors, batteries and or renewable energy voltage sources can be used as a DC unequal voltage sources.

II. Stages of Multilevel Inverter

The three stages of CMLI are high-voltage stage, medium voltage stage and low voltage stage. The high, medium and low voltage stages are made of three-level inverters constructed using cascaded H-bridge. This method is used to avoid the undesirable high switching frequency for all the voltage stages despite the fact that the inverter's dc sources are selected to maximize the inverter levels by eliminating redundant voltage state.

III. Multilevel Inverter Topologies

3.1 Introduction

The multilevel voltage source inverter is recently applied in much industrial application such as AC power supplies, static VAR compensators, drive systems, etc, one of the significant advantages of multilevel configuration is the harmonic reduction in the output waveform without increasing switching frequency of decreasing the inverter power output. The output voltage waveform of a multilevel inverter is composed of the number of levels of voltages, typically obtained from capacitors voltage sources.

As the number of levels reach infinity the output THD approaches zero. The number of the achievable voltages levels, is limited by voltage unbalance problems, voltage clamping requirement, circuit layout and packaging constraints.

3.2 Types of Multilevel Inverter

There are three types of multilevel inverter namely Diode-Clamped Multilevel Inverter, Flying-Capacitor Multilevel Inverter and Cascaded-Inverters with Separated Dc Sources. Multilevel inverters include an array of power semiconductors and capacitor voltage sources, the output of which generates voltages with stepped waveforms with less distortion, less high switching frequency, higher efficiency, lower voltage devices and better electro-magnetic compatibility. The commutation of the switches permits the addition of semiconductors must withstand only reduced voltages.

3.2.1 Diode-Clamped Multilevel Inverter (DCMLI)

The Diode-Clamped Multilevel Inverter uses capacitors in serried to divide up the Dc bus voltage into a set of voltage levels. To produce m level of the phase voltage, an m level diode-clamp inverter need m – 1 capacitors on the DC bus. A single phase five-level diode-clamped inverter is shown in Fig.3.1.

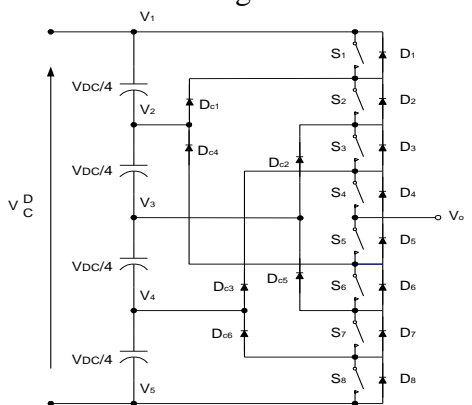


Figure 3.1: Diode-Clamped Multilevel Inverter (DCMLI)

Table 3.1 shows the phase voltage level and their corresponding switch states. When the switch is on the output voltage becomes one otherwise the value becomes zero. Table 3.1 shows the switching pattern of Diode clamped Multi- Level Inverter and the output phase voltage for the corresponding switching

states when the switch S1 and S8 is ON, the output phase voltage is produced by the voltage of V1 and V5.

Table 3.1: Switching Pattern of DCMLI

POWER INDEX VALUE	OUTPUT PHASE VOLTAGE (V _O)				
	V1	V2	V3	V4	V5
S1	1	0	0	0	0
S2	1	1	0	0	0
S3	1	1	1	0	0
S4	1	1	1	1	0
S5	0	1	1	1	1
S6	0	0	1	1	1
S7	0	0	0	1	1
S8	0	0	0	0	1

3.2.2 Flying Capacitor Multilevel Inverter

Capable of solving capacitor voltage unbalance problem and excessive diode count requirement in DCMI .Employs separate capacitors pre charged to $[(n-1)/(n-1) \times VDC]$, $[(n-2)/(n-1) \times VDC]$... $\{[n-(n-1)]/[n-1] \times VDC\}$. Size of voltage increment between two capacitors defines size of voltage steps in ICMI output voltage waveform.A flying capacitor multilevel inverter in fig 2.2 uses a ladder structure of DC side capacitor where the voltage on each capacitor differs from that of the next capacitor

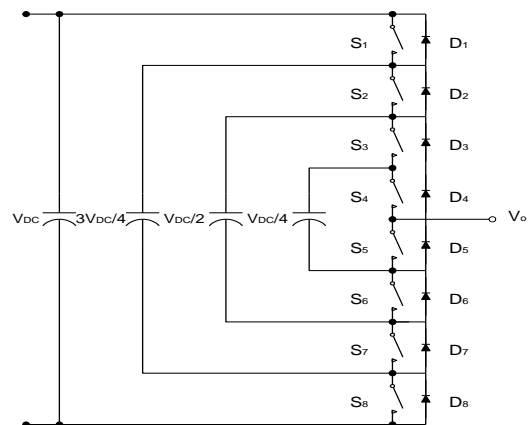


Figure 3.2: Flying Capacitor Multilevel Inverter (FCMLI)

To generate m-level staircase output voltage, m1 capacitors in the D bus are needed. Each phase-leg has an identical structure. The size of the voltage increment between two capacitors determines the size of the voltage levels in the output waveform.

Table 3.2 shows the phase voltage level and their corresponding switch states. From table 3.2, state 1 represents that the switch is on and state 0 represents the switch is off.

Table 3.2: Switching Pattern of FCMLI

OUTPUT V_{Ao}	SWITCH STATE							
	Sa1	Sa2	S _{am-1}	S _{am}	S _{a'1}	S _{a'2}	S _{a'm-1}	S _{a'm}
$V_5=V_{dc}$	1	1	1	1	0	0	0	0
$V_4=3V_{dc}/4$	1	1	1	0	1	0	0	0
$V_3=V_{dc}/2$	1	1	0	0	1	1	0	0
$V_2=V_{dc}/4$	1	0	0	0	1	1	1	0
$V_1=0$	0	0	0	0	1	1	1	1

3.2.3 Cascaded Multilevel Inverter

The general function of this multilevel inverter is the same as that of the other two previous inverters. This multilevel inverter using cascaded inverter with SDCSs synthesis a desired voltage from several independent sources DC voltages which may be obtained from batteries, fuel cells, all solar cells. of different level inverters are connected in series.

A. Circuit Diagram

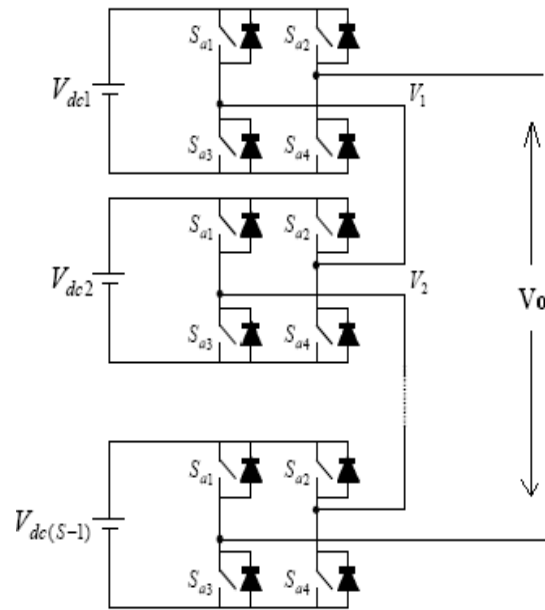


Figure 3.2: Cascaded Multilevel Inverter

3.3. Block Diagram

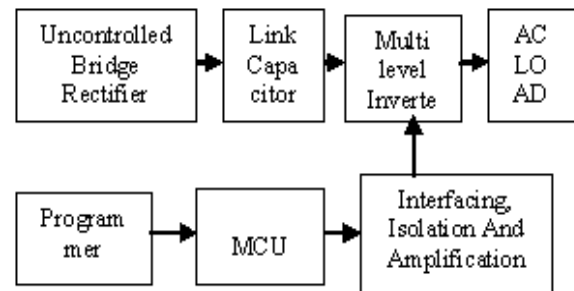


Figure 3.3 Block Diagram of CMLI

IV. Harmonic Reduction Technique

4.1 Fourier Analysis.

In multilevel inverter the Fourier series is used to find the expression for output voltage. The Fourier expression for the output voltage is found because the angles are related with output voltage expression and the output voltage is quarter wave symmetry. So the Fourier series constants a_0 , a_n become zero and we have to find only b_n .

$$V_o(wt) = \{ a_0 + \sum_{N=1, 2, 3, \dots} (a_n \cos nwt + b_n \sin nwt) \} \sin n\theta \dots\dots\dots 4.1$$

The output voltage expression For five level inverter is found as

$$V_o(wt) = \sum_{n=1, 3, 5, \dots} (4V_{dc}/n\pi) (\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3 + \cos n\alpha_4) \sin n\theta \dots\dots\dots 4.2$$

4.2 Harmonic Analysis

The proposed system analyses the frequency spectrum and Voltage control. In conduction angle control the lower order harmonics are reduced. By adjusting the turn on angle to various levels, it is possible to reduce the lower order harmonics. And the efficiency, power factor is improved. The Fourier expression is also obtained for the output voltage of five-level inverter.

For five level inverter

$$V_o(wt) = \sum_{n=1, 3, 5, \dots} (4V_{dc}/n\pi) (\cos n\alpha_1 + \cos n\alpha_2 + \cos n\alpha_3 + \cos n\alpha_4) \sin n\theta \dots\dots\dots 4.3$$

4.3 Genetic Algorithms

```

% A Program For Analysis of
Sinusoidal Pulse Width Modulation
Of An AC
% Signal.
% By: Yasin A. Shiboul
% Date 15/8/2003
% PART I (preparation)
% In this part the screen is
cleared, any other functions,
figures and
% variables are also cleared. The
name of the programm is displayed.
clc
clear all
disp('Sinusoidal Pulse Width
Modulation of AC Signal')
disp(' ')
% In this part the already known
variables are entered, the user is
% asked to enter the other
variables.
% Vrin is the rms value of the
input supply voltage in per unit.
Vrin=1;
% f is the frequency of the input
supply voltage.
Sinusoidal Pulse Width Modulation of AC Signal
    
```

The frequency of the input supply voltage, $f = 50$
 The modulation index, m_a , ($0 < m_a < 1$), $m_a = 0.1$
 The phase angle of the load in degrees = 30
 The number of pulses per half period = 12

Answer

Alpha	Beta	Width
7.3500	7.6500	0.3000
22.2000	22.8000	0.6000
37.0500	37.9500	0.9000
51.9000	53.1000	1.2000

The rms Value of the Output Voltage,
 $V_o = 0.2828$

The rms Value of the output voltage fundamental component
 $V_{rms} = 0.0799$

The RMS value of the load current is
 $CORMS = 0.0812$

The RMS value of the supply current is
 $CSRMS = 0.0217$

Performance parameters are

$THD V_o = 3.3924$

$THD I_o = 0.1760$

$THDIS = 3.6124$

$PF = 0.0796$

4.3. Harmonic Order

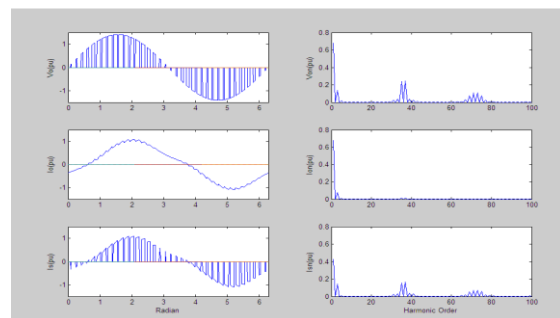


Figure 4.1 Harmonic Order

4.4. Generation of the output Voltage pulses

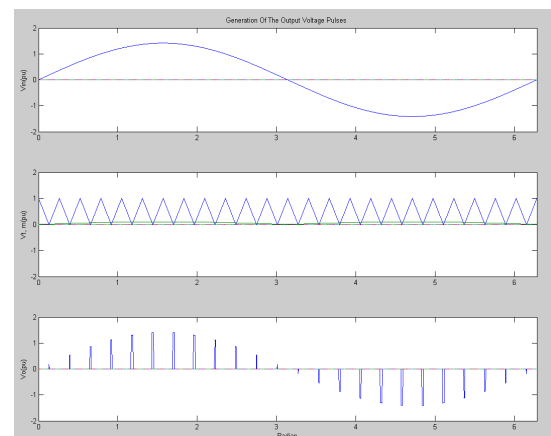


Figure 4.2 Generation of the output voltage pulses

4.5. MATLAB Model for 11 Levels CMLI

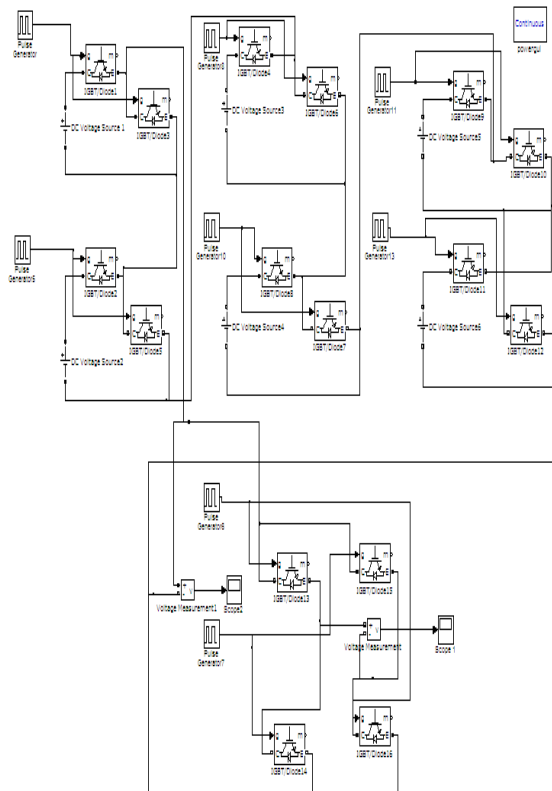


Figure 4.3 MATLAB Model Single Phase Inverter

4.6. Simulation Result of 11 Levels CMLI

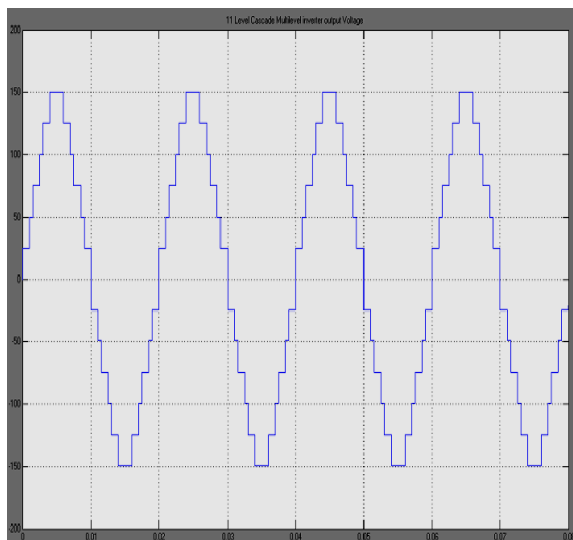


Figure 4.4 Simulation Results Of 11 Levels CMLI

4.7.11 Level Positive Half Wave Output

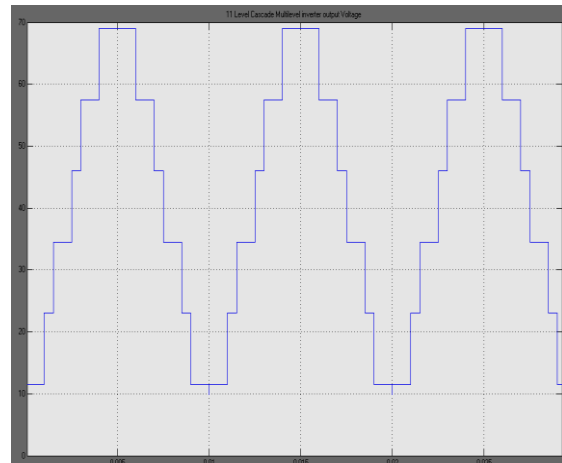


Figure 4.5 11 output waveform

V. Conclusion

The disturbances in power electronics equipment are often periodic and rich in higher harmonics. They have been frequencies and are often above the bandwidth of regulators used to control fundamental components. Therefore the ‘regular’ control can only partially reduce their effects on the distortion of control variables. The cascade multilevel inverter with unequal DC sources is illustrated and the gate triggering pulse is given by the step modulation Genetic algorithms technique.

In this project, the calculation time is insensitive to the switching frequency ratio and the stepped wave form had minimal total harmonic distortion. The fifth and seventh order harmonics are reduced by using the harmonic elimination method. The algorithms was able to efficiency eliminate fifth and seventh harmonics from the line current. for the fast convergences it was found to filter out fundamental components and use only the remaining signal(higher harmonic – distorted current) for adaptation. A simulation was performed to show the output of proposed method.

References

[1].Harmonic Elimination of Cascade Multilevel Inverters with Unequal DC Sources Using Particle Swarm Optimization by H. Taghizadeh and M. Tarafdar Hagh, Member, IEEE, IEEE Transactions on Industrial Electronics, Vol. 57, NO. 11, November 2010

[2].Carrasco. D.J., Franquelo L.G , Bialasiewicz J.T , Galvan “Power-electronic systems for the grid integration of renewable energy sources: A survey,” IEEE Trans. Ind. Electron., vol. 53, no. 4, pp. 1002– 1016, Jun. 2006.

[3].Cheng Y, Qian C, Crow M L , Pekarek S , and Atcitty S, “A comparison of diode- clamped and cascaded multilevel converters for a STATCOM with energy storage,” IEEE Trans. Ind. Electron., vol. 53, no. 5, pp. 1512– 1521, Oct. 2006.

[4].Chiasson J N, Tolbert L M., McKenzieK J, and Du Z, “Real-time computer control of a multilevel converter using the mathematical theory of resultant,” Math. Comput. Simul., vol. 63, no. 3–5, pp. 197–208, 2003.

[5].Chiasson J N, Tolbert L M, McKenzieK J, and Du Z,, “The use of power sums to solve the harmonic elimination equations for multilevel converters,” EPE J., vol. 15, no. 1, pp. 19–27, Feb. 2005.

[6].Clerc M and Kennedy J, “The particle swarm: Explosion, stability and Convergence in a multi – dimensional complex space,” IEEE Trans. Evol. Comput., vol. 2, no. 3, pp. 91–96, Jun. 1998.

[7].Enjeti P N, Ziogas P D , and Lindsay J L, “Programmed PWM Techniques to eliminate harmonics: A critical evaluation,” IEEE Trans. Ind. Appl., vol. 26, no. 2, pp. 302–316, Mar./Apr. 1990.

[8].Ozpineci E, Tolbert M , and Chiasson L M, “Harmonic optimization of multilevel converters using genetic algorithms,” IEEE Power Electron. Lett., vol. 3, no. 3, pp. 92–95, Sep. 2005.

[9].Patel H S and Hoft R G , “Generalized harmonic elimination and voltage control in thyristor inverters: Part I — Harmonic elimination,” IEEE Trans. Ind. Appl., vol. IA-9, no. 3, pp. 310–317, May/Jun. 1973.

Conferences



Periasamy.M. (2012). “Harmonic Optimization of Cascade Multilevel Inverter with Unequal DC Sources Using Genetic Algorithm”. Proceedings National level Conference on Recent Advancements & challenges in Electrical Engineering and applications, 18th-19th Feb. (2012), IRTT, Erode, Tamil Nadu. And received his B.E degree in Electrical and Electronics Engineering from Saphthagiri College of Engineering. Affiliated to Anna University Chennai in the year 2005. Currently she is pursuing her master degree in Power Electronics and Drives in Sasurie College of Engineering affiliated to Anna University of Technology, Coimbatore.