

Hardware Implimentation of FPGA based PID Controller

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Abstract — Proportional-Integral-Derivative controllers are widely used in automation systems. They are usually implemented either in hardware using analog components or in software using computer-based systems. In this paper, we focused our work on performance analysis and implementation of digital controller based on Field Programmable Gate Array device. In proposed system implementation of software module using 'VHDL' for Xilinx FPGA (XC3S400) based PID controller for temperature control system is presented. FPGA based system allows design up gradation in the field with no hardware replacement. FPGA is a superior alternative to mask programmed ASICs. It also offers good closed-loop performance while using less resource which results in cost reduction with high speed and low power consumption, this is desirable in embedded control applications.

Keywords— *Field Programmable Gate Array (FPGA); Proportional-Integral-Derivative (PID) controller; Very High Speed Integrated Circuit Hardware Description Language (VHDL); Pulse Width Modulation (PWM); Application Specific Integrated Circuits (ASICs).*

I. INTRODUCTION

A plant and controller are two subsystems of control system. The plant is an entity controlled by the controller. The controller can be either digital or analog. The proportional-integral-derivative (PID) controller is one of the most common types of feedback controllers that are used in dynamic systems. PID controller has been widely used in many different areas, such as temperature control, process control, manufacturing, robotics, automation, transportation systems and power electronics. Implementation of PID controllers has gone through several stages of evolution, from early pneumatic devices, followed by vacuum and solid state analog electronics before arriving at today's digital implementation via microprocessors or FPGA [1].

Generally, an implementation of digital PID controller includes the use of microprocessors or microcontrollers. The memory holds the application program while the processor fetches, decodes and executes the program instructions. Such methods has a disadvantage in speed of operations because the operations depend on software which has a sequence of instructions and commands which needs many machine cycles to execute [2]. Drawback in microprocessor based systems is, the demanding control requirements of modern power conditioning systems will overload most of the microprocessors and the computing speed limits the use of microprocessor in complex algorithms. Microcontrollers, Microprocessors and Digital Signal Processors (DSPs) can no longer keep pace with the new generation of applications that

requires more flexible and higher performance without increasing cost and resources. Further the tasks are executed sequentially which takes longer processing time to accomplish the same task in Microcontrollers and DSPs [3].

An FPGA-based digital feedback control system using a novel DA-based PID controller was presented. The complete system was designed using a modular approach and integrated and downloaded into both Xilinx and Altera FPGA chips [1]. Implementing the multiplierless PID controller on FPGA gives better rise time as well as settling time [2]. All Digital PID is the new aspect in the industrial controller. It is totally frequency base method of PID control. This avoids the use of analog to digital converter, which reduce the error and the cost of the system design [3]. A novel robust PID based controller was presented, for FPGA implementation. This research minimizes the Power Consumption and Delay as compared to conventional PID controllers [4]. The speed control using PI and PID control modes is explained and an implementation of the PID controller using OP-AMPS for the speed control of a DC motor is given [5].

Recently, Field Programmable Gate Arrays (FPGA) is becoming alternative solution for the realization of digital control systems. And the operations on FPGA are hardware compatible [4]. Building PID controllers on Field Programmable Gate Arrays (FPGAs) improves speed, power efficiency, accuracy, compactness and cost effectiveness. These are attractive features from the embedded systems design point of view. Previous work has reported the use of FPGAs in digital feedback control systems, such as magnetic bearings, pulse width modulation (PWM) inverters, ac/dc converters, induction motors, variable-speed drives, and anti windup compensation of controllers. Another advantage of FPGA-based platforms is their capability to execute concurrent operations which allows parallel architectural design of digital controllers [1]. When design is implemented on FPGA they are designed in such a way that they can be easily modified if any need arise in future. We have to just change the inter connection between these logic blocks. This feature is reprogramming capability of FPGA makes it suitable to make your design using FPGA. Using FPGA within a short time, fast implementation of design can also possible. Also implementation of FPGA-based digital control schemes proves less costly and hence they are economically suitable for small designs. Thus FPGA is the best way of designing digital PID controller [3].

II PID CONTROLLER

The PID algorithm consists of three modes proportional, integral and derivative mode. It has a simple control structure which was understood by plant operators which they found relatively easy to tune. Since many control systems using PID controller have proved its satisfactory performance, it still has a wide range of applications in industrial control and it has been an active research topic for many years [4].

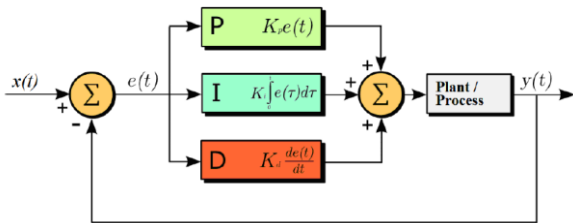


Fig. 1 Block diagram of a general PID based feedback control system.

The equation that describes the PID controller behavior in continuous time domain is

$$u(t) = Kp e(t) + Ki \int e(t) dt + Kd \frac{de(t)}{dt}$$

$$= Kp [e(t) + \frac{Ki}{Kp} \int_0^t e(t) dt + \frac{Kd}{Kp} \frac{de(t)}{dt}]$$

$$= Kp [e(t) + \frac{1}{Ti} \int_0^t e(t) dt + Td \frac{de(t)}{dt}]$$

Where, $K_p \rightarrow$ proportional gain

$K_i \rightarrow$ integral gain

$K_d \rightarrow$ derivative gain

Transfer function of PID controller, is by taking Laplace transform.

$$\frac{u(s)}{e(s)} = Kp [1 + \frac{1}{Ti S} + Td S]$$

Integral time constant,

$$Ti = \frac{Kp}{Ki}$$

Derivative time constant,

$$Td = \frac{Kd}{Kp}$$

$$\frac{u(s)}{e(s)} = Kp + \frac{Ki}{S} + Kd S$$

$$\frac{u(s)}{e(s)} = Kp [1 + \frac{1}{Ti S} + Td S]$$

Now apply the backward difference method, Then,

$$u(t) = e(t)Kp [1 + \frac{Ts}{Ti(1-z^{-1})} + Td \frac{1-z^{-1}}{Ts}]$$

$$u(t) = u(t-1) + Kp [e(t) - e(t-1)] + \frac{Kp Ts}{Ti} e(t) + \frac{Kp Td}{Ts} [e(t) - 2e(t-1) + e(t-2)]$$

$$u(t) = u(t-1) + Kp [e(t) - e(t-1)] + Ki Ts e(t) + \frac{Kd}{Ts} [e(t) - 2e(t-1) + e(t-2)]$$

$$= (Kp + Kd) e(n) + Ki \sum_{j=1}^n e(j) - Kd e(n-1)$$

$$= Kp e(n) + Kd e(n) - Kd e(n-1) + Ki \sum_{j=1}^n e(j)$$

$$= Kp e(n) + Kd [e(n) - e(n-1)] + Ki \sum_{j=1}^n e(j)$$

$$U(n) = (Kp + Kd) e(n) + Ki \sum_{j=1}^n e(j) - Kd e(n-1)$$

From above equation and following [7] we can construct the algorithm's block diagram as shown in figure 2.

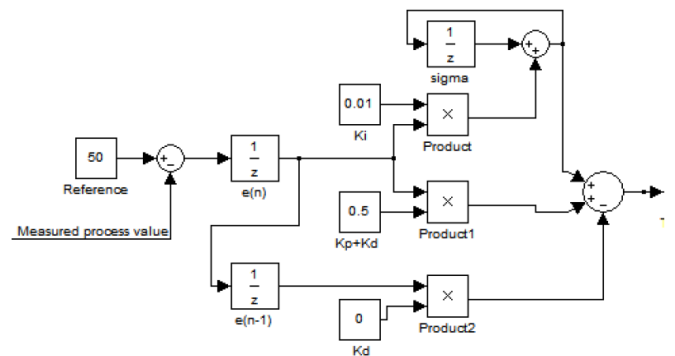


Fig 2: digital PID controller algorithm [7].

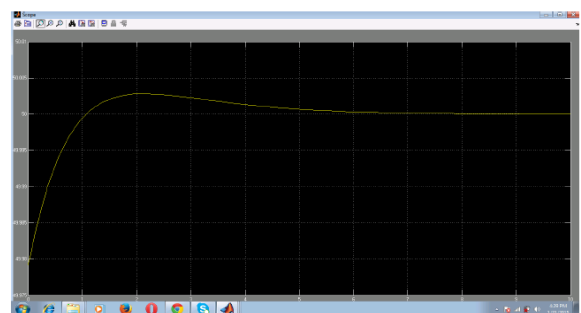


Fig 3. Simulation result for PID controller at set point 50 (from Fig. 2).

The proportional control (K_p) is used so that the control signal responds to the error immediately. But the error is never reduced to zero and an offset error is inherently present. In order to remove the offset error the integral control action is used. Derivative control is used to dampen out oscillations in the plant response. The presence of derivative control reduces the need of K_p being large to achieve stability [5].

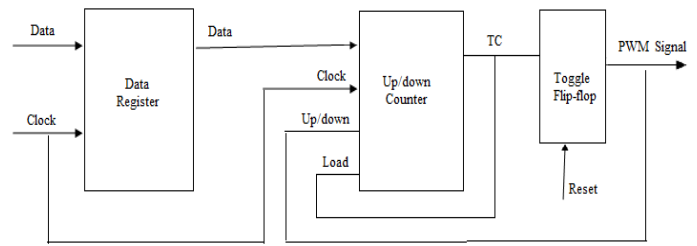


Fig.6. Block diagram of PWM modulator.

The basic principle is, a data register stores the value which is loaded on to the Up/Down counter. When the counter reaches its terminal count. This counter is used to generate the pulse width modulation. A data register is used to store the value for the counter. Value determines the width of the pulse. The Up/Down Counter loaded with a new value from the data register when the counter reaches its terminal count. PWM out is generated by Toggle Flip-flop. When data value is first loaded, counter counts-down from data value to zero. Now terminal count and PWM signals are Low. When counter goes through 0 transition state, terminal count (TC) is generated. Triggers Toggle Flip-flop drives PWM signal high. Now Data value is re-loaded and counting proceeds up to maximum value. Again Terminal count (TC) is generated when counter reaches its maximum value. This drives PWM signal to toggle from high to low. The cycle repeats when the Data value is re-loaded. The direction of counter is controlled by PWM signal. The counter is set to count down when PWM is Low, and count up when PWM is high. The Terminal count signal controls data value loaded to counter from data register. The data is loaded when terminal count is high. The duty cycle of PWM signal is controlled by data value.

IV. CONCLUSION

In proposed system, a FPGA-based design approach is applied to design a temperature control system. In general, embedded control designers need to go through three phases in the design of digital control systems: 1) software modeling/simulation in an environment such as Matlab/Simulink; 2) hardware implementation; and 3) post synthesis simulation of whole system including both hardware and software. The step response of the plant can be observed with the scope block As a result, the development time for designing efficient embedded software is greatly reduced. In future work we plan to implement multiplierless digital PID controller using distributed arithmetic architecture. The advantages are high processing speed, reduced power consumption and hardware compatibility for implementing on FPGA.

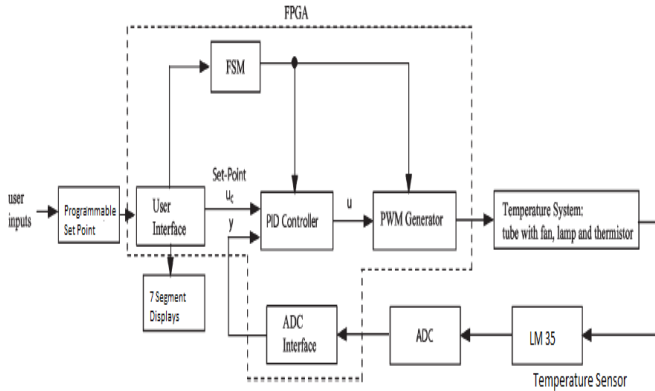


Fig .4 Application based block diagram.

III. PID CONTROLLER & PULSE WIDTH MODULATOR

The PID controller follows the classical structure. It contains two saturation blocks one for the overall sum and the other for integral part as shown in figure 5. The controller has a pipeline structure of three stages, in other words, it needs three clock cycles to perform all the operations. In order to improve the area and speed, hardware multipliers have been used. These multipliers are included in the Spartan 3 family of Xilinx and subsequent FPGAs. These multipliers have 15 bit input data bus and are signed. This leads to optimum implementation when the fixed point implementation uses less than 15 bit in two's complement [4].

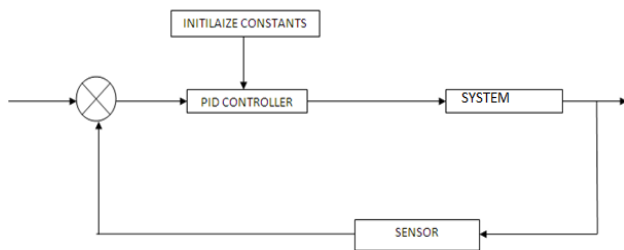


Fig. 5. Block diagram of robust PID controller.

The PWM modulator admits a two's complement input and transforms it into a PWM signal as shown in figure 6. The PWM module also generates the enable signal for the control loop. This makes the PID controller begin a new cycle and calculate a new PWM input value.

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