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Gate-All-Around FET based 6T SRAM Design Using a Device-Circuit Co-Optimization Framework

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***Abstract*:- Gate-all-around nanowire transistor is deemed as one of the most promising solutions that enables continued CMOS scaling. Compared with FinFET, it further suppresses shortchannel effects by providing superior electrostatic control over the channel. Due to the unique device structure, gate-all-around nanowire transistor also allows more efficient layout design by exploiting 3-dimensional stacking configurations. In this paper, we investigate the 6T SRAM cell design for gate-all-around nanowire transistors using a device-circuit co-optimization framework. At the device level, TCAD simulation and current source modeling method are applied to extract the model. Layout designs with horizontal, lateral, vertical stacking device structures are explored. At the circuit level, read and write assist techniques are studied to relieve the negative impact of low on-currents on SRAM stabilities incurred by nanowire channels. Operating at 300 mV, assist techniques can increase the read static noise margin and the write static noise margin of 6T SRAM up to 82% and 92%, respectively.**

I. INTRODUCTION

Multi-gate field-effect transistors (FETs) have been widely accepted as key device structures to aggressively scale down the device feature size while mitigating short-channel effects (SCEs) [1]. FinFET, which is also known as a tri-gate FET, has been widely adopted as an enabler of device scaling down at the 22 nm technology node [2]. For FinFET, the conducting channel, which is the “fin”, is wrapped around by dielectrics and gate materials at three sides. In contrast to planar CMOS transistors, the leakage current is reduced due to the better controllability. However, looking beyond sub-10 nm, the challenges of further scaling down FinFETs, such as strong threshold voltage variation and deterioration of mobility, are expected to increase dramatically incurred by continued reduction of the feature size. Proposed as a device structure for ultimately scaling down to the end, gateall-around (GAA) nanowire FETs have dielectrics and gate materials wrapped around all sides of the channel [3], [4]. With a better electrostatic controllability over FinFET, GAAFETs can relax the channel diameter by 30-40% in comparison to the fin width in FinFET and less leakage current.

Like FinFET, the conducting strength of GAA-FET must be controlled by discretely adjusting the number of nanowires. Instead of being limited in the horizontal direction along the device plane, nanowires of GAA-FET can also be stacked laterally or vertically, which allows more compact layout designs [6]–[8]. Previous works on GAA-FETs span both device fabrication [6], device modeling [9] and circuit design levels [10]. However, a device and circuit co-optimization framework is needed to address the increased complexity in design and optimization at both levels.

TABLE I : GAA-FET DEVICE PARAMETERS

GAA Type	ND cm−3	NS cm−3	NC cm−3	Φm eV	VT V
NMOS	2.0 × 10^20	2.0 × 10^20	undoped	4.46	0.17
PMOS	2.0 × 10^20	2.0 × 10^20	undoped	4.73	-0.17

In this paper, we investigate the GAA-FETs based SRAM design with the aid of proposed device and circuit cooptimization framework. Look-up table (LUT) based currentsource models are firstly extracted from device simulation using TCAD. Verilog-A models are then constructed and verified by the mixed-mode simulation and H-SPICE simulation. The influence of three geometrical stacking methods (horizontal, lateral and vertical) on SRAM layout design is studied. Finally, assist techniques for GAA-FETs based SRAM design are also explored to address the low on-currents issue brought by nanowire channels.

The rest of this paper is organized as follows. Section II describes device level simulations and model extractions. Section III shows the layout characterization of three stacking methods. The SRAM read and write assistant techniques are studied in Section III. The 6T SRAM simulation results and analysis are discussed in Section IV. Section V concludes this paper.

II. DEVICE LEVEL SIMULATION AND MODELING

The 3-D device structure and the channel region cross section of a GAA-FET is shown Fig. 1. “D”, “S” and “G” indicate drain, source and gate electrode, respectively. The nanowire, which is the conducting channel, is wrapped around on all sides by the dielectric and gate materials. Generally, The nanowire may be fabricated using Si/Ge sacrificial layer or repeated etching [11]. Therefore, edges of the rectangle nanowire should be rounded as shown on the right picture of Fig. 1. The size and shape of the nanowire can be defined using height

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(Hsi) and width (Wsi). In order to achieve a higher on-current, the raised drain/source structure is adopted.

A. Device Level Simulation

3-D device level simulations are performed using Synopsys Sentaurus [12] with the device structure shown in Fig. 1. Fermi-Dirac statistics, density gradient quantization model and Philips unified mobility model are used to capture the physical transportation mechanism. Gate length Lg and equivalent oxide thickness tox are fixed at 10 nm and 0.68 nm, according to ITRS specifications for the 11.9 nm technology node.

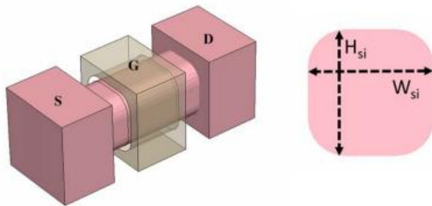

Fig.1. 3-D structure and channel region cross section of GAA-FET.

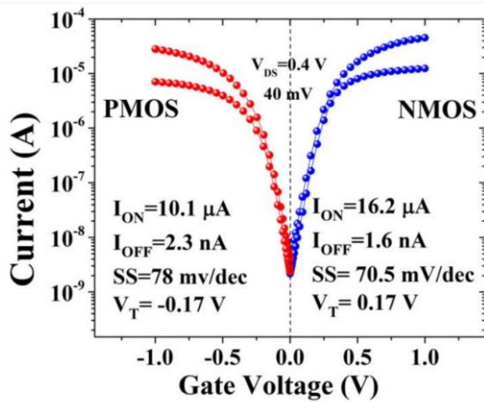

Fig. 2. VGS-IDS curves of GAA-FET NMOS/PMOS simulated by 3-D TCAD. ON/OFF currents, sub-threshold swing (SS) and threshold voltage (VT) are also shown.

The length of channel extension at the source/drain side is 5 nm. A Gaussian lateral (1-D) doping profile with peak concentration at the edge of the raised-source/drain regions is assumed. The peak drain doping (ND), peak source doping (NS) and channel doping (NC) are shown in the Table. I. The Hsi and Wsi are 10 nm for achieving a good electrostatic integrity. The leakage current (IOF F) is set to approximate 100 nA/um by choosing a suitable gate work function (Φm). Simulated VGS-IDS curves of NMOS/PMOS at VDS = 0.4 V and VDS = 40 mV and extracted parameters are shown in Fig. 2.

B. GAA-FET Stacking Structures

LUT based models of GAA-FETs are extracted using the current source modeling (CSM) technique, in which an NMOS or PMOS is modeled as a set of current sources and parasitic capacitances. Fig. 3 illustrates the equivalent circuit. By performing DC/AC sweeping at terminals of transistor, values of current sources and capacitances are pre-characterized and recorded into LUTs.

The total current flows out of gate (G), source (S) and drain.

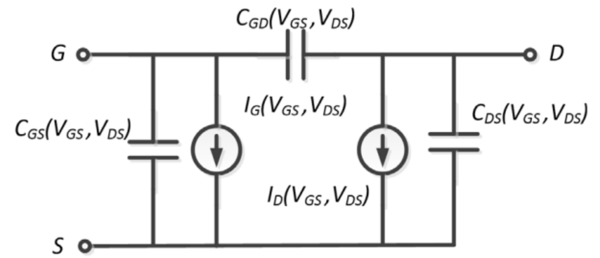

Fig. 3. Current source model for a GAA-FET. The output currents of the current source and the values of the parasitic capacitances are all functions of voltage pair (VGS, VDS).

(D) terminals can be calculated as follows:

I(G) = IG + CGD ∂VDG/∂t + CDS ∂VDS/∂t (1)

I(S) = IS + CGS ∂VSG/∂t + CDS ∂VSD/∂t (2)

I(D) = ID + CGD ∂VDG/∂t + CDS ∂VDS/∂t (3)

where I(·) is the total current. IG, IS and ID are currents of independent current sources. Finally, SPICE-compatible LUT based Verilog-A models are constructed for further circuit level simulations. The extracted Verilog-A model is verified by comparing H-SPICE simulations with mixed-mode simulations using TCAD sentaurus for a inverter at different supply voltages VDD, which is shown in Fig. 4.

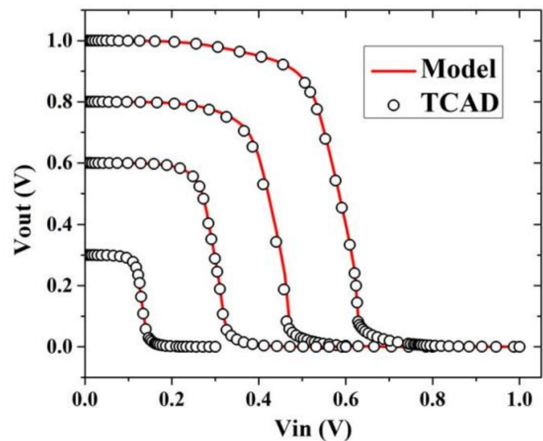

Fig. 4. Comparison of the extracted Verilog-A model against TCAD mixed mode simulations for a inverter at varied VDD.

C. GAA-FET Stacking Structures

The unique nanowire channel provides GAA-FET with extra freedom in stacking configurations. Fig. 5 shows the schematic structures of H-GAA (A), a laterally stacked GAA-FET (B) and a vertically stacked GAA-FET (C). Increasing nanowires in a horizontal GAA-FET (H-GAA) is similar to increasing “fins” in FinFET. For a lateral GAA-FET (L-GAA), nanowires are stacked on top of each other in parallel to the device plane. For a veritcal GAA-FET (V-GAA), the bottom electrode sits on the substrate and nanowires are vertical to the device plane, which allows a more compact layout design while relaxing the requirement of gate length. In this work, all vertical nanowire channels are assumed to stand on the (100) wafer with a surface orientation of (100).

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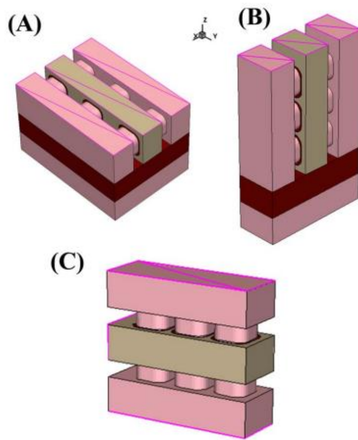

Fig. 5. Geometries of GAA-FETs with different stacking structures. (A). HGAA; (B). L-GAA; (C).V-GAA. Pink lines indicate the position of contacts.

III. GAA-FET BASED 6T-SRAM DESIGN

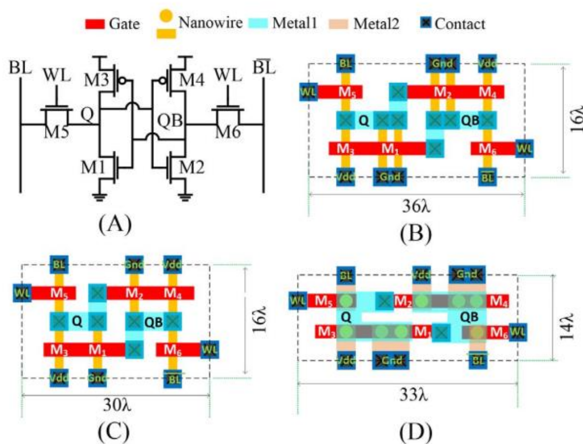

Fig. 6 shows the the 6T SRAM circuit schematic (A) and layout designs for (B) H-GAA, (C) L-GAA and (D) V-GAA.

The GAA-specific geometries and design rules are summarized in Table. II. Please note that all layout designs shown in Fig. 6 are in (2,1,1) configuration, which indicates the number of nanowires in pull-down transistor (Npd), access transistor (Nac) and pull-up transistor (Npu) are 2, 1 and 1, respectively. The area reduction achieved with L-GAA and VGAA are 16.7% and 19.8%. We can see that the V-GAA can achieve the most efficient layout design.

TABLE II GAA-SPECIFIC GEOMETRIES AND DESIGN RULES

Parameter	Value (nm)	Comment
LG	$2\lambda = 10$	gate length
WSi	10	nanowire width
HSi	10	nanowire height
PNW	$3\lambda = 15$	nanowire pitch
WC	$3\lambda = 15$	Minimum contact size
WM2M	$3\lambda = 15$	Minimum space between metal wires
WG2C	λ	Minimum space of gate to contact

The major issue associated with GAA-FETs is their low on-currents. Performance of the SRAM array is thus degraded which is mainly caused by the reduced read current, resulting in higher bitline (BL) delay. One can increase the on-current by increasing the number of nanowires using afore-mentioned stacking methods. However, the leakage current would also increase in this way. For this purpose, read and write assist techniques and their effects on stability metrics of the corresponding memory operation must be investigated. The static noise margin (SNM) quantifies the amount of voltage noise required at the internal nodes of a bitcell to flip the SRAM cells contents. SNMs at hold, read and write states are used as the criteria of stabilities.

A. VDD Boost for Read Assist

Having a large enough read static noise margin (RSNM) is the key to read the content in the SRAM cell without disrupting the storage. To enhance the read stability of the 6T SRAM, one can strength the pull-down transistor or weaken the access transistor using various techniques. In our paper, VDD boost technique is adopted, which increases the supply voltage VDD while the SRAM is being read.

B. WL Overdrive for Write Assist

Write static noise margin (WSNM) is an important metric to evaluate the write operation and is measured as the difference between the VDD and minimum wordline (WL) voltage that is needed to flip the cell content. In this paper, WL overdrive (WLOD) is chosen as the write assist technique, which sets VW L to a voltage level higher than VDD to strongly turn on the access transistor while the SRAM is being written.

IV. EXPERIMENTAL RESULTS AND ANALYSIS

This section presents the experimental results. GAA-FET based 6T SRAM with (1,1,1), (2,1,1) and (3,1,1) configurations are simulated. The results of leakage power for the three configurations are reported in Fig. 7. One can observe that increasing the number of nanowires could increase the leakage power. However, the gap between (1,1,1) and (3,1,1) configurations is monotonically reduced when the supply voltage decreases. Reducing the supply voltage and operating the SRAM at a near-threshold region can achieve energy saving.

Nevertheless, small supply voltages could damage the stability of SRAM cells, which necessitates assist techniques for read and write operations. Table III summarizes the HSNM, RSNM and WSNM for different 6T SRAM configurations with or without assist techniques. When the (1,1,1) SRAM cell is operated at 300 mV supply voltage, the RSNM and WSNM can increase up to 82% and 95% by applying 20% VDD boosting in both VDD boost and WLOD assist techniques. It can be observed that increasing the number of nanowires from (1,1,1) to (2,1,1) in pull-down transistors can result in a 28.6% increase of RSNM, but WSNM decreases by 17%.

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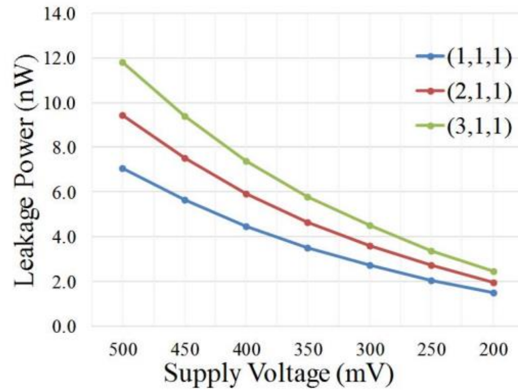

Fig. 7. Leakage power of GAA-FET based 6T SRAM design in different configurations with (Npd, Nac, Npu) = (1,1,1), (2,1,1) and (3,1,1), respectively.

TABLE III GAA-FET BASED 6T SRAM EXPERIMENTALRESULTS

Circuit	V_{DD} (mV)	N_{pd}	N_{ac}	N_{pu}	V_{DD} Boost	WLOD	HSNM (mV)	RSNM (mV)	WSNM (mV)
6T	500	1	1	1	0%	0%	191	76	147
6T	500	1	1	1	10%	0%	191	104	147
6T	500	1	1	1	20%	0%	191	132	147
6T	500	2	1	1	0%	0%	184	106	132
6T	500	3	1	1	0%	0%	178	120	125
6T	400	1	1	1	0%	0%	155	65	102
6T	400	1	1	1	10%	10%	155	90	142
6T	400	1	1	1	12.5%	12.5%	155	96	152
6T	400	2	1	1	0%	0%	151	84	91
6T	400	3	1	1	0%	0%	148	95	86
6T	300	1	1	1	0%	0%	116	49	63
6T	300	1	1	1	20%	20%	116	89	123
6T	300	1	1	1	40%	20%	116	116	123
6T	300	2	1	1	0%	0%	115	63	52
6T	300	3	1	1	0%	0%	112	68	48

V. CONCLUSION

In this paper, we investigate the 10 nm gate length GAAFET based 6T SRAM design using a device and circuit cooptimization framework. First, NMOS and PMOS characteristics are simulated using sentaurus TCAD. Device parameters are also tuned and optimized in this phase. LUTs based Verilog-A models are constructed via current source modeling method for fast circuit simulations. Layout designs of horizontal, lateral and vertical stacking GAA-FET are also studied. The vertical GAA-FET design can achieve the least area footprint. Read and write assist techniques are investigated to increase the stability of GAA-FET based 6T SRAM at various supply voltages.To address the low on-current issues incurred by nanowire channels, read and write assist techniques are proposed. Our experimental results show that the negative impact of low on-currents on noise margins of SRAMs can be relieved.

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