# Full Chip Thermal Analysis using Generalized Integral Transforms

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***Abstract*—The estimating the temperature variation is critically important for timing analysis, leakage reduction, power consumption, hotspot avoidance and reliability concerns during modern IC design. In this paper, highly efficient full chip thermal simulator analysis is used in advance stage temperature aware chip design. Here the generalized integral transforms (GIT), used to estimate the temperature distribution of full-chip with a truncated set of spatial bases which only needs very small truncation points. Then, we develop a fast Fourier transform like evaluating algorithm to efficiently evaluate the derived formulation. The proposed GIT-based analyzer can achieve an order of magnitude speedup compared with a highly efficient Green's function-based thermal simulator.**

***Keywords— Circuit simulation, generalized integral transforms (GITs), physical design, simulation, thermal analysis,3-DIC.***

## I. INTRODUCTION

Now a days the CMOS technology scales down in using electronics components so that the power density of VLSI circuits increases monotonically as an increase of components. The power dissipated produced in the circuit's converts into heat and as a result, it raises the temperature of dies and induces hot spots. These thermal related phenomena significantly reduce the performance and reliability of circuits [1]–[16]. For example, the resistance of copper interconnect increases 39% as the temperature rises from 20 C to 120 C, and the mean-time-to-failure of the interconnect exponentially decreases as the temperature increases [1]. Thermal analyser is used to precisely predict the thermal impacts on design performance, an efficiently and accurately .The thermal simulators can be classified into two classes, numerical and analytical methods. The numerical methods use the finite difference method or the finite-element method (FEM) to transfer heat equations to resistance–capacitance(RC) network equations. Based on the RC network equations, several methods have been proposed to save the runtime. Wang et al. [2] utilized the alternating-direction-implicit method to split the equivalent RC system into different alternating directions, andalternately performed the line smooth scheme in each direction. In [3], the model order reduction technique was employed to improve the efficiency of transient analysis. Li et al. [4] applied the multi-grid method to speed up the convergence rate of iterative methods, and developed an order reduction scheme to save the runtime of dynamic thermal simulation. Because of the flexibility for dealing with the complicated structure, the numerical framework is the main stream in back-end design stages such as the post layout thermal verification. As pointed out in [1], [5], and [6], temperature-aware designshould be brought to early design stages such as thermal-aware floor-planning and placement. To give a reasonably accurate temperature prediction with little computational effort, [1] proposed a compact thermal model which modeled the package and interconnect layers as effective heat transfer coefficients for the boundary conditions of die. With the modeled heat transfer coefficients for the heat sink, prelayout interconnect and package, recently, an efficiently numerical thermal simulator developedby Yong et al. [7] is very suitable for early temperature-aware design stages. Because their simulator applies an adaptive discretization algorithm for spatial and temporal domains to analyse the temperature profile without degrading the accuracy, the number of temperature variables and simulating time steps can be significantly reduced. The other category of thermal simulators being suitable for early design stages is the analytical method. The primary advantage of analytical approaches is that they avoid the volume meshing procedure of entire substrate, and have closed-form representations for the temperature distribution of the entire die. Hence, they are flexible to obtain the temperature distribution of certain user-specified regions without performing the thermalsimulation for the entire die. Furthermore, based on the closedform representations, the fast temperature evaluation of the die can be achieved for early design stages.One analytical thermal solver is the Green's function-based method [6]. First, the steady-state Green's function of chip with a unity impulse power source is calculated. After that, its steadystate temperature distribution with arbitrary power source map is got by taking the convolution of Green's function and its power density distribution with a table lookup method. To enhancethe efficiency for lots of power sources, they used a seriesof cosine waveforms to approximate the power density map, andthe temperature map of all grid cells were cast into the form ofdiscrete cosine transform (DCT). Although their computationalcost is, where and are numbers of divisionsin the power density map along - and -directions, respectively,they can only provide the steady state thermal simulation. Moreover, as indicated in [6], a large number of truncation points for the Green's function is usually required

to achieve an accurate solution. To overcome these shortcomings, our major contributions are as follows.

• Compared with a highly efficient Green's function-based method [6], improve the bound of the error decaying rate of analytical solution for the steady state temperature distribution and provide a transient temperature simulation by utilizing the generalized integral transforms (GITs) [17]–[19] to construct a set of spatial bases and calculate their time-varying coefficients.

• Develop a fast Fourier transform (FFT) like evaluating algorithm to efficiently evaluate the temperature map of all grid cells, and its computational cost is in the order of O(MN $\log_2 N_x N_y$), where $N_x$,$N_y$ are truncationpoints of bases in the - and -directions, respectively.

• Build an efficient 3-D IC thermal simulator by combining the GIT and numerical schemes, and its efficiency and accuracy are demonstrated by experimental work.

## II. THERMAL MODELING FOR EARLY DESIGN STAGES

A compact thermal structure of the chip, as illustrated in Fig. 1, can be used for early design stages. This model consists of three portions [1]: the primary heat flow path, the secondary heat flow path, and the heat transfer characteristic of each macro/block on the silicon die. The primary heat flow path is composed of thermal interface material, heat spreader and heat sink. The secondary heat flow path contains interconnect layers, input/output (I/O) pads and the print circuit board (PCB). The functional blocks are modelled as many power generating sources attached to a thin layer close to the top surface of die with the thickness being equal to the junction depth. The major concerns of early-stage temperature-aware optimization procedure are to reduce the temperature or the thermal gradient of die. Here, the main focus on estimating the temperature distribution.

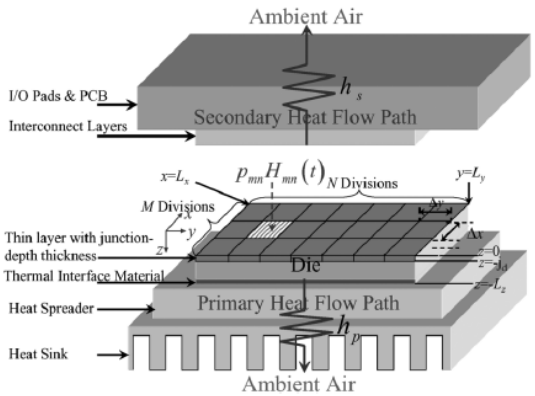


Fig. 1. Compact thermal model for early design stages

According to energy conservation law, the changing rate ofenergy in a unit volume of substrate equals to the conductionheat through the unit volume [17]. Based on this heat conduction mechanism,the temperature $T_d(r,t)$ of die can be governed by thefollowing heat transfer equations [2], [4], [5], [7]:

$$\sigma(T_d)\frac{\partial T_d(\mathbf{r},t)}{\partial t} = \nabla\cdot(\kappa(T_d)\nabla T_d(\mathbf{r},t)) + p(\mathbf{r},t); \quad \mathbf{r}\in D$$

$$\kappa(T_d)\frac{\partial T_d(\mathbf{r},t)}{\partial n_{b_s}} + h_{b_s}T_d(\mathbf{r},t) = f_{b_s}(\mathbf{r}).$$

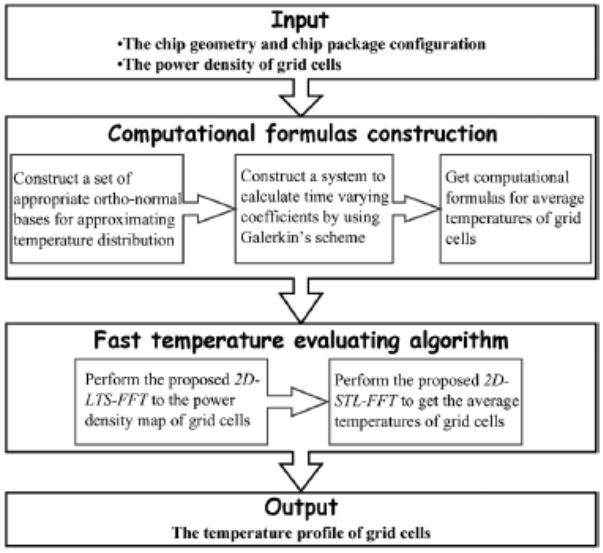


Fig.2. Executing flow of the proposed GIT-based thermal simulator

## III. FULL CHIP THERMAL SIMULATION

The executing flow of our GIT-based thermal simulator is summarized in Fig.2.The GIT-based computational formulas for the full-chiptemperature distribution was used. The two efficient FFT like evaluating algorithms,2D-LTS-FFT and 2D-STL-FFT to getthe transformed coefficients for the power density map of gridcells and the desired temperature distribution, respectively.In reality, the leakage power of chip is temperature dependent.

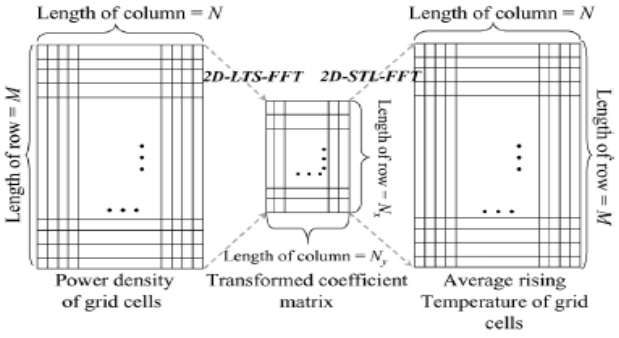


Fig .3.Overview of using 2D-SLT-FFT and 2D-LTS_FFT to evaluate the average rising temperature of grid cells.

## IV. EXPERIMENTAL RESULTS

Here GIT-based thermal simulator and the Algorithm of a highly efficient Green's function based method [6] in C++ language. The results are compared with a commercial computational fluid dynamic software ANSYS.

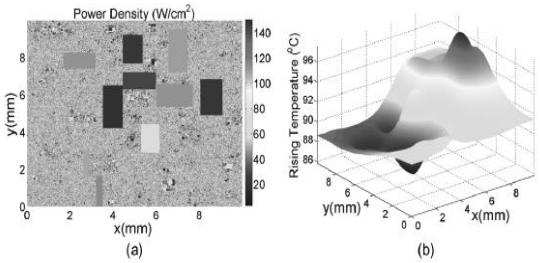


Fig 4.Powerdensity and temperature distribution

## CONCLUSION

An accurate and efficient GIT-based thermal simulator has been explained. The proposed algorithm only takes0.13 s for a chip with one million functional blocks and overone million grid cells, and 0.48 s for a 3-D IC with 3.146million grid cells in the post-calculating stage to achieve accuratelysteady state temperature distribution. Therefore, theproposed GIT-based thermal simulator is very suitable for thethermal-aware design flow.

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