FPGA Implementation of Nine Level Inverter

Karleena.l[1], Shailaja.B[2,] Aravind. M.R[3]
PG scholar, Department of Electronics & Communication
M.S Engineering Collage,
Bangalore, India.

Venkateshappa[4]
Associate professor, HOD Department of Electronice communication, M.S Engineering College
Bangalore, India.

***Abstract*— This paper presents a nine level Cascaded H-bridge multilevel inverter topology in which a low switching frequency is made use taking up the advantages of the low frequency, such as low thermal stress and high conversion efficiency. Standard cascaded multilevel inverter requires 'n' number of DC sources for '2n+1' levels. In actual practice to obtain nine- levels we need three H- bridges to be cascaded. Instead we make use of only two H- bridges in cascaded to derive nine- level output. Normally, Inverter produces square wave ac output and so it is called as two-level inverter. Compared to two-level inverter, Multilevel Inverters (MLI's) are having high efficiency since they produce accurate sinusoidal (staircase) output. Cascaded H-bridge multilevel inverter consists of separate full bridge inverters which are connected to individual dc sources for producing different levels in the output voltage. This type is advantageous because, it does not require additional clamping diodes and balancing capacitors as in the case of diode-clamped and flying capacitor types respectively. The Unique feature of MLI is, "the more the number of output voltage levels, the less the harmonic content in it". But, if the number of output voltage level is increased, it requires more number of switches which leads to circuit complexity. Therefore, the proposed topology provides reduced switch inverter topology which produces nine level output and high quality output power due to its high number of output levels, high conversion and low thermal stress. MATLAB/SIMULINK is used to verify the performance of the proposed model. FPGA based implementation of the nine inverter is implemented on the Spartan 3E FPGA and analysed**

Keywords—component; formatting; style; styling; insert (key words)

I. INTRODUCTION

The Multilevel inverter is a promising power electronics topology for high-power applications because of its low electromagnetic interference (EMI) and high efficiency with low-switching-frequency control method. Traditionally, each phase of a cascaded multilevel inverter requires n dc sources [1-5] for 2n + 1 levels. For many applications, obtaining so many separate dc sources may preclude the use of such an inverter. To reduce the number of dc sources required when the cascaded H- bridge multilevel inverter is applied to a motor drive, a scheme is proposed in this paper that allows the use of a single dc source (such as battery or fuel cell). Previous works has shown that Pulse Width Modulation (PWM) control can be used on HCMLI. Compared to the traditional cascaded H-bridge multilevel inverter, the proposed HCMLI has a low number of dc sources and retains the low switching-frequency advantage .In a multilevel converter the output of each phase leg can attain more than two levels leading to improved quality of the output voltage and current. The circuit comprising each leg and its proper operation ensure that voltage blocked by the switches reduces as the number of levels is increased. In addition, multilevel converters are modular to some extent, thereby making it easy to scale voltage ratings by increasing the number of "cells". There are three types of multilevel inverters used in general (1) diode-clamped inverter, (2) capacitor-clamped inverter, and (3) cascade inverter. The type of multilevel inverter made use here is cascaded. The AC power supply is converted into DC power using any of the known bridge rectifier configurations. Two levels of DC voltages (say 24 Volts and 12 Volts) are obtained with proper arrangements. The DC voltages are given as input to the H-Bridge inverters designed using MOSFETs. These MOSFETs are driven by individual driver circuits. The required Gate pulses are given through the output port of the PIC controller. The two inverters are cascaded or connected in series to form the obtained arrangement. Driver performs the operations of Buffering, Isolation and Amplification. For buffering purpose IC,,s are incorporated. For amplification and isolation purposes, opto couplers are used. The cascaded inverter provides output voltages at different levels for the gate pulses given to the MOSFETs through the Microcontroller unit. The output voltage obtained from the cascaded inverter bridge is the summation of the output voltages of the different outputs of the inverters (say +V, 0, -V).

II. H-BRIDGE MULTILEVEL INVERTER

Usually two or three levels inverter totally do not eliminate the harmonics using the multilevel inverter is introduced as an alternative to traditional PWM inverters. In this topology phase voltage levels at the converter terminals is 2N-1, where N is the number of cells or DC link voltages. Each H-bridge cell may have positive, negative or zero voltage. Nine level inverter requires 16 IGBT switches and Four Dc sources. A cascaded H-bridges multilevel is a series connection of multiple H-bridge inverters. Single H-bridge module is capable of producing five level output voltage. Each inverter module is capable of producing 2E, E, 0, -E, -2E. That means by using two bridges 9 level output voltage is produced. The total output voltage is sum of the outputs of the inverter modules and the nine voltage levels are 4E, 3E, 2E, E, 0, -E, -2E, -3E, -4E. The advantages of this proposed circuit is number of switches are reduced. The cost and complexity is less in this circuit. To synthesize nine output voltage levels, it employs two independent dc voltage sources of 2*E* which are divided into two input sources *E* in order to secure an

additional dc voltage source of *E*. The inverter module having a bidirectional switch produces 5-levels of output voltage (-2*E*, -*E*, 0, *E*, 2*E*) by controlling of the switches. Since every output terminal of the inverter module is connected in series, the output voltage becomes the sum of the terminal voltages of each inverter. The circuit for nine level cascaded H-bridges is shown in figure 2, the gating signals for the inverter is generated by using square PWM. This circuit is simulated using the MATLAB software. FPGA based implementation of the nine inverter is implemented on the Spartan 3 FPGA and analysed.

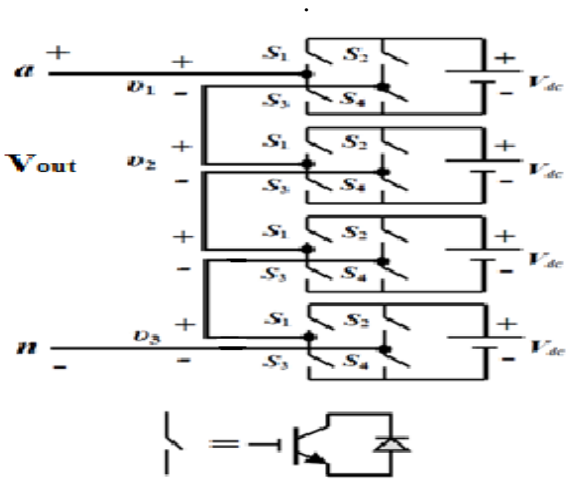


Fig.1 cascaded H-bridge 9-level inverter

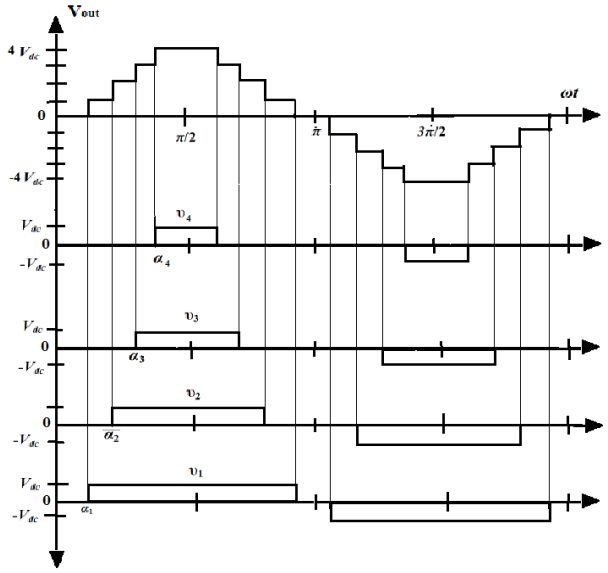
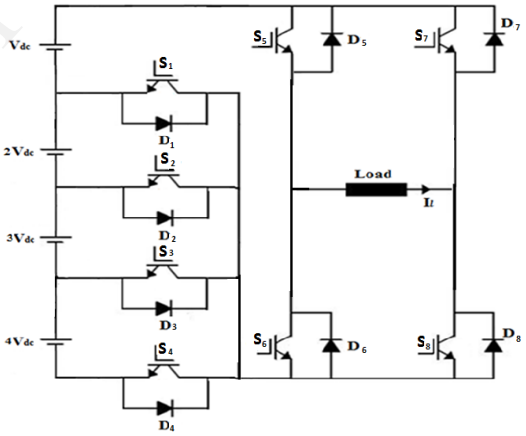


Fig.2 Output Wave form of Nine level Inverter

III. PROPOSED TOPOLOGY



The objective of the proposed topology is to improve the quality of the output voltage of the multilevel inverter with reduced number of switches and to generate nearly sinusoidal output voltage waveforms. The operation of the nine levels is explained with the switching diagram above. In the positive half cycle when the output voltage is vdc the current pass comprises; the lower supply,D2,S5,Load,S8,and back to the lower supply .when the output voltage is 2vdc,current pass is;lowersource,S2,the upper source,S5,load S8,and back to the lower source. When the output voltage is 3vdc, the current pass; upper supply, S5, load, S8, S3, lower supply. When the output voltage is 4vdc the current comprises; upper supply, S5, load S8, S4, lower supply. In the negative half cycle S5 and S8 are replaced by S6 and S7 respectively.

Switch level	S1	S2	S3	S4	S5	S6	S7	S8
0	0	0	0	0	0	0	0	0
vdc	1	0	0	0	1	0	0	1
2vdc	0	1	0	0	1	0	0	1
3vdc	0	0	1	0	1	0	0	1
4vdc	0	0	0	1	1	0	0	1
3vdc	0	0	1	0	1	0	0	1
2vdc	0	1	0	0	1	0	0	1
vdc	1	0	0	0	1	0	0	1
0	0	0	0	0	0	0	0	0
-vdc	1	0	0	0	0	1	1	0
-2vdc	0	1	0	0	0	1	1	0
-3vdc	0	0	1	0	0	1	1	0
-4vdc	0	0	0	1	0	1	1	0
-3vdc	0	0	1	0	0	1	1	0
-2vdc	0	1	0	0	0	1	1	0
-vdc	1	0	0	0	0	1	1	0

Table.1 Switching diagram of proposed topology

The simulation model was designed using MATLAB/Simulink software. Gating signals for the inverter are generated by square pulse modulation technique. The circuit was simulated with RLC load.

IV. SIMULATION AND RESULT

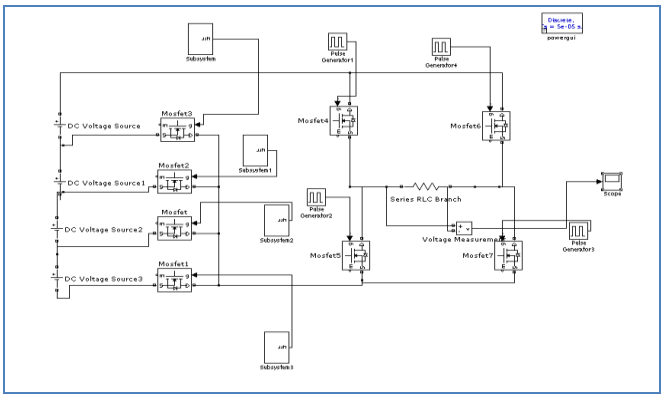


Fig.3 Simulation Work in Matlab Software

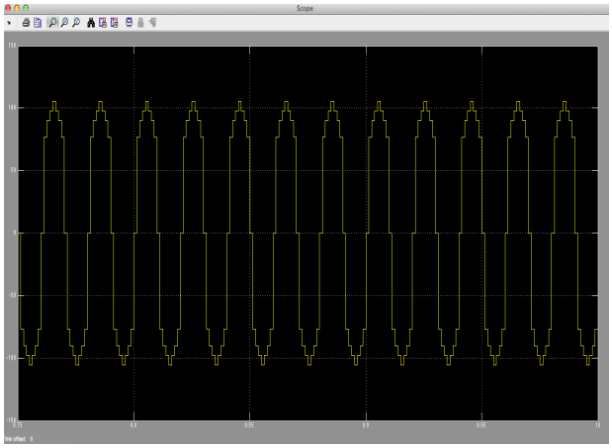


Fig.4 Output Waveform of Simulation

V. FPGA IMPLEMENTATION

The FPGA become key components in implementing high performance digital signal processing system. In this paper inverter is simulated by using Xilinx software 10.1 simulation tool by using VHDL language verilog coding program is written for switching strategies .FPGA is chosen for hardware implementation of switching strategy mainly due its high computation speed that can ensure the accuracy of the instants that that gate signals are generated. PWM pulses was downloaded in FPGA (XC3S400PQ208) from Spartan 3.simulation results which will be compared with the experimental results. These pulses are tested with CRO.

BLOCK DIAGRAM

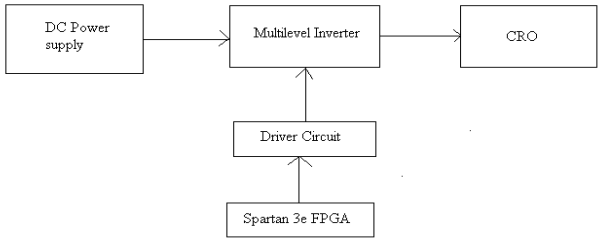


Fig.5 Block diagram for FPGA Implementation

The different points like 0, 50,100,150 are taken for the reference. The check pulses are taken at the reference points .thus the eight pulses are generated .generated pulses cannot given directly to the inverter circuit. To avoid the short circuit problem and to provide the isolation between FPGA device which is working as control circuit and the inverter circuit which is power circuit, the opto-isolator are used. Pulses are given to the MOSFETs through interfacing and driving circuit .it contains buffer and opto-isolator.

V. EXPERIMENTAL RESULTS AND DISCUSSION

To validate the proposed topology and theory, hardware of the 9 level cascaded H-bridge multilevel inverter has been built using the MOSFET as the switching devices. DC source voltage is getting by using diode rectifier circuit which is placed in front of the inverter circuit. Four equal DC source voltages are applied which is equal to 75 volts. Hence finally the output AC voltage for each phase is equal to 225 volts. The MOSFET driver ICs are employed to drive the MOSFET switches. The MOSFETs are switched ON and OFF by using the PWM pulses which are generated by using the FPGA Controller. Switching is written in the high level language VHDL or verilog code and then it is dumped in the FPGA kit. The output terminal of the inverter is connected to CRO. The experimental results are compared with the simulation result . The output of the 9 level inverter is 400 volts with frequency of 50Hz.

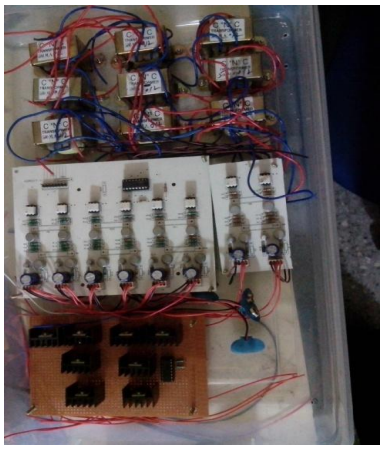


Fig 6. Hardware Setup

CONCLUSION

Switching patterns adopted are applied at the eight inverterer to generate sixteen output voltage levels at different modulation on s. Xilinx FPGA enable to make easy, fast and flexible design and implementation. The experimental and simulated results are show satisfactory results in term of total harmonic distortion and tput voltage and current waveform shapes.

Inverter type		Nine level
Nembure of Switches Used	Cascaded H-Bridge	16
	proposed topology	8
% of switch reduction		50%

Table 2: percentage of reduction in switches

REFERENCES

1. Chunmei Feng and Vassilions G Agelidis. 2000. On the Comparison of fundamental and high frequency Carrier based techniques for multilevel NPC Inverters. IEEE PES Conf. 2: 520-525.
2. Golubev AN andIgnatenko SV. 2000. On the Influence of number of stator winding phases on noise characteristic of 41- 46.
3. Gopukumar K, Biswas SK, S atishkumar S and Joseph Vithyanthil. 1984. Modified current source inverter fed induction motor drive with reduced torque pulsation. IEE Proc. 313(4): 150-164.
4. Haoran Zhang, Annette Von Hounne, Shaoan Dai et al. 2000. On Multilevel inverter Modulation schemes to Eliminate Common Mode Voltages. IEEE Transactions on Industry Applications.36 : 1645-1653.
5. Juan Dixon and Luis Moran. 2006. High-Level Multi-step Inverter Optimization Using a Minimum Number of Power Transistors. IEEE Transactions on Power Electronics. 21(2): 330-337.
6. Mohapatra. KK, Gopukumar K, Somashekhar VT and Umanand L. 2002. A Modulation scheme for six phase induction motor with an open-end winding. 25th Annual Conference IECON 02, Spain. pp. 810-815.
7. Muhammad H Rashid. 1996. Power Electronics Circuits Devices and Applications. 2nd Ed. PHI, New Delhi. pp. 566-572.
8. Shivakumar E.G, Gopukumar K, Sinha S.K and Ranganathan V.T. 2001. Space vector PWM control of dual inverter fed open-end windingion motor drive. IEEE APEC Conf. 1: 399-.
9. Somashekhar V.T and Gopukumar K. 2003. Three level inverter configuration cascading two two-level inverter.
10. Thomas M Jahns. 1980. Improved reliability in solid state ac drives by means of multiple independent phase drive units. IEEE Trans. Ind. Appl. 16(3): 321-331.