FPGA implementation of multimodulus flexible divider for phase locked loop

SHOBANA.J
ME vlsi design
Srinivasan engineering college
Perambalur-621212
Shobanaj28@gmail.com

K.VIJAYA KANTH M.E
Assistant professor
Srinivasan engineering college
Perambalur-621212
k.vijayakanth85@gmail.com

***Abstract*-The two major challenges for modern communication are low power and low voltage. Frequency divider is a good example. Here an Extended True single phase clock (ETSPC) based divide by 2/3 is designed that is applied for low supply voltage & low power consumption. Wired OR scheme is nothing but only one is needed to implement both counting logic & mode selection control. The working frequency of the counter is enhanced due to reduced critical path between E-TSPC FF's. The proposed design consists of multiband flexible divider instead of E-TSPC based divide by 2/3 counter.**

Keywords-Dual modulus prescaler, DFF, Extended True Single Phase Clock, frequency synthesizer, Phase locked loop.

I.INTRODUCTION

The basic module for frequency synthesizer is prescaler or high speed divide by N/N+1 counter. Its design is critical because the operating frequency is high and it consumes high power. A divide by N/N+1 counter consists of flip-flops (FF's) and extra logic which is used to determine the terminal count. The conventional design uses current mode logic latches. The disadvantage is large load capacitance. It limits the maximum operating frequency and current drive capabilities and also increases the total power consumption. Next, FF based divide by N/N+1 counter designs are adopted by the dynamic logic FF's. Dynamic logic is nothing but True Single Phase Clock (TSPC). The enhanced design uses E-TSPC FF's for high speed low power applications. Here the transistor stacked structure is removed and all transistors become free from body effect.

In former time, the optimized prescaler design mainly focused on the simplification of logic part. It reduces the circuit complexity and the critical path delay. An E-TSPC design is fixed with one extra pMOS /Nmos transistor and it can form an integrated function of FF. The control logic of first flip flop reduces the FF toggling and yield another version. These two designs have 16 transistors inside. In this, 4 transistors are used for mode control logic and the ratioed structure is used to achieve the simple circuit. A general TSPC logic family adopts both ratioed and ratioless inverter. So the transistor stacking height is up to 5 and it loses the advantage of low V_{dd} operation.

A power gating technique, between V_{dd} and FF extra pMOS is inserted and it employs a two divide by 2/3 counter designs. In divide by 2 mode of operation the ff is not used ie., shunt down. It has more number of transistor and it is not suited for low V_{dd} operations.

For high-rate data transmission, HiperLAN II and IEEE 802.11 a/b/g are identified and for low rate data transmission, IEEE 802.15.4are identified. The power hungry blocks in the RF front-end is frequency divider and it is usually implemented by a phase locked loop. In a frequency synthesizer, the first stage of frequency divider uses a large amount of power and it is implemented using injection locked divider consumes large chip area and has a narrow locking range. The application of multiband flexible divider is WLAN in the multi gigahertz range.

In the implementation of first stage divider uses source coupled logic circuits at high frequency but it consumes more power. Dynamic latches are faster and

consume less power compared to static dividers. The TSPC and E-TSPC have the ability to drive the dynamic latch with a single clock phase and it avoids clock skew problem. Clock skew is the difference in the arrival time between the two sequentially adjacent registers. The phase locked loop consists of phase frequency detector, loop filter, VCO and frequency divider. In PLL, the frequency divider block is replaced by E-TSPC based divide by 2/3 counter and multiband flexible divider.

II. CONVENTIONAL E-TSPC BASED DIVIDE BY 2/3 COUNTER

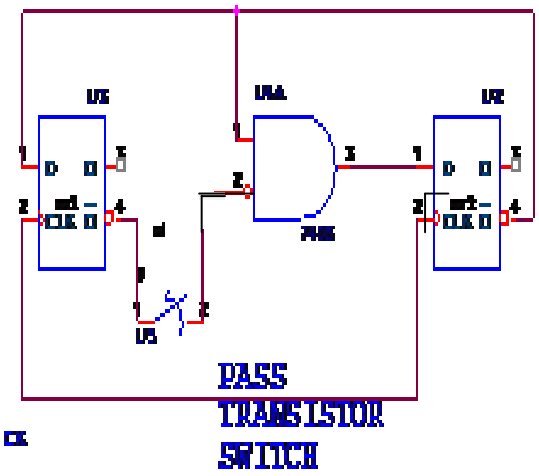

Fig. 1.conventional E-TSPC based divide by 2/3 counter

The conventional E-TSPC based divide by 2/3 counter consists of two FF's and the AND gate. The OR gate is replaced with the switch for the purpose of divide control. The one input of AND gate has a negation bubble. The FF1 output Q is complemented before being given into the FF2. When the switch is open, the input coming from FF1 is disabled and FF2 only performs the divide by two operation ie., the input clock frequency is divided by 2. When the switch is close, FF1 and FF2 connected to form a counter and perform the divide by 3 operation. The E-TSPC FF's has the minimum number of transistor and is suitable for low voltage operation. Except two E-TSPC FF's the divide by 2/3 counter contains only one pMOS transistor. The pMOS transistor serves as the function of the switch.

III. WIDEBAND E-TSPC 2/3 PRESCALER

E-TSPC 2/3 prescaler consumes large short circuit power and having high operating frequency than compared to TSPC 2/3 prescaler. The wide band single phase clock 2/3 prescaler consists of two D FF and two NOR gate. The first NOR gate is placed at the output of FF1 and the second NOR gate is placed at the input of FF2. Here the division ratios are controlled by the logic signal MC.

IV. MULTIBAND FLEXIBLE DIVIDER

The multi band flexible divider consists of a multi modulus 32/33/47/48 prescaler, a 7-bit programmable P-counter and a 6-bit swallow S-counter.

A. Multi modulus prescaler

The input frequency can be divided by 32, 33, 47 and 48 are done by using wide band multi modulus prescaler. It is same as to the 32/33 prescaler. The difference between the two is an additional inverter and a multiplexer. It also performs an additional division (divide by 47 and divide by 48) without the need of any extra flip flop, a considerable amount of power is saved and the complexity of multi band divider is reduced. It consists of wide band 2/3 prescaler, four asynchronous TSPC divide by 2/3 circuits and combinational logic circuits for the purpose of achieving multiple divisions ratios. The MOD signal is used for controlling divisions. Additional Sel signal is used to switch the prescaler between 32/33 and 47/48 modes.

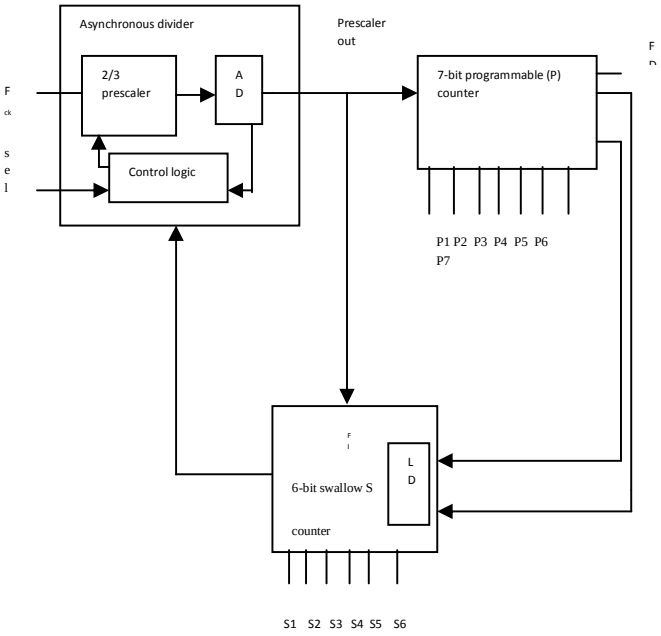

Fig.2. Diagram of multi band flexible divider

B. Swallow counter

The 6-bit S-counter consists of six asynchronous loadable bit-cells, a NOR-embedded DFF and additional logic gates to allow it to be programmable from 0 to 31 for low-frequency band and from 0 to 47 for the high-frequency band. At first, MOD=0, the multi modulus prescaler selects the divide by 33 or divide by 48 and P, S counters started down counting the input clock cycles. When S counter completes it counting the control signal switches to logic 'o' for that the prescaler changes to divide by 32 or divide by 47. By the use of programmable input the counter is loaded to a specified value from 0 to 31 for low band and 0 to 41 for high band of operation.

C. Programmable (P) counter

A programmable P- counter is a 7-bit asynchronous down counter which consists of 7 loadable bit cells and additional logic gates. The p7 bit is attached to the Sel signal of the multi modulus prescaler. P4 and p7 bits are always kept at logic '1'. The remaining bits are externally programmed from 75 to 78 for lower frequency band and 105 to 122 for higher frequency band. 7-bit P- counter is used for low frequency band and 8-bit P-counter is needed for high frequency band.

V. PHASE LOCKED LOOP

It is a control system that generates an output signal whose phase is related to the phase of an input reference signal. It is an electronic circuit. It consists of phase detector, loop filter, VCO and frequency divider.

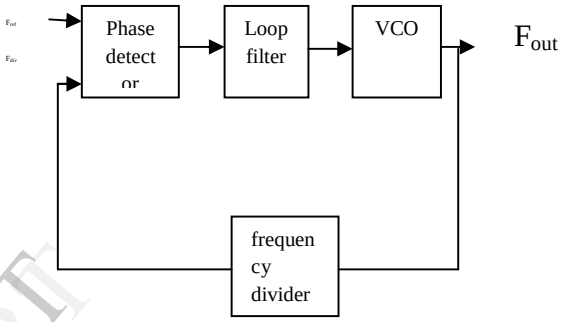

Fig.3. phase locked loop diagram

Here comparison is made between the phase of the input signal and the phase of the signal derived from it's output oscillator in a feedback loop is controlled by the signal coming from phase detector.

A. Phase detector

Phase detector has two inputs. One is reference input and another one is feedback from the VCO. The phase detector output controls the VCO for making negative feedback system, the phase difference between the two input's are kept constant.

If the phase of the VCO is lagged with the reference phase, the output of the phase detector produces an up pulse. If it is forward to the reference phase the output is down pulse. Then it is given to a loop filter or charge pump for the purpose of converting into an analog electrical signal. Charge pump circuit is an optional circuit. This type of circuit, the

output of the phase detector is directly given to the loop filter.

B. *Loop filter*

Loop filter is usually a low pass filter. It has two functions. The first function is to determine the loop dynamics, also called stability. Based on this, the changes in the reference frequency and the changes of the feedback divider are determined. The second function is to limit the amount of ripple appeared at the output of phase detector that is applied to the VCO control input.

The phase detector output is a tristate output, and then it drives an op-amp loop filter. Loop filter is a based on an integrator loop. It is more advantageous compared to other type of filters. It has zero steady state phase error. Loop filter is an analog quantity. By using verilog, we can't simulate analog loop filter. But in the digital loop filter it is possible to simulate loop filter by using verilog, because it uses a sampled data control system.

C. *Oscillator*

VCO is a circuit module that oscillates at a controlled frequency. The oscillating frequency is controlled using voltage $v_{control}$. $v_{control}$ must be in the steady state for the VCO to operate properly.

D. *Frequency divider*

The frequency divider is placed between the oscillator and the feedback input to the phase detector. It produces a frequency synthesizer. Some pll has the frequency divider in between the reference clock and the reference input to the phase detector. In case the divider is placed in the feedback path means it divides the frequency by N and the reference input divider divides by M.

VI.EXPECTED RESULTS

The multi band flexible divider was modeled using VHDL & simulated using model sim 5.7 & Xilinx 9.2ISE was used as synthesis tool for implementing the design in Spartan 3E FPGA.F ig.4 shows (a) simulation output of divide by 2 counter and (b) simulation output of divide by 3 counters. Table gives comparison results of device utilization

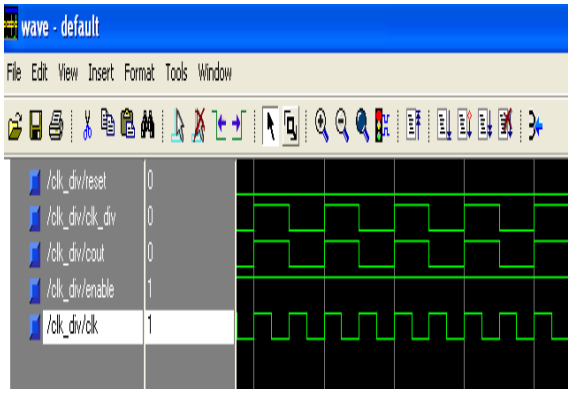

Fig. 4(a). Simulation output of Divide by 2 counter

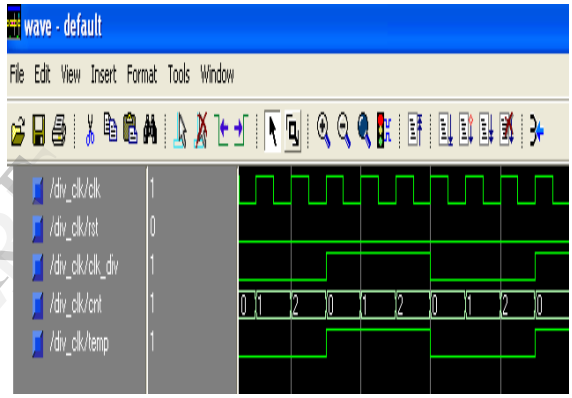

Fig. 4(b). Simulation output of Divide by 3 counter

Table 1 Device utilization

DEVICE UTILIZATION	DIVIDE BY 2 COUNTER	DIVIDE BY 3 COUNTER
Number of slices	1	39
Number of slice flip flop	1	33
Number of 4 input LUT'S	1	73
Number of IO's	4	3
Number of bonded IOB's	1	3
Number of Gclk's	1	1

VII.CONCLUSION

The E-TSPC based divide by 2/3 counter design simplifies the control logic and pmos transistor alone serves the purpose of both select control and counter excitation logic. This simple circuit leads to a shorter critical path and reduces its power consumption. In the design of proposed wide band multi modulus 32/33/47/48 prescaler a wideband 2/3 prescaler is verified. A dynamic logic multi band flexible integer-N divider is designed. It uses the wideband 2/3 prescaler, multi modulus 32/33/47/48 prescaler. Since the multi modulus 32/33/47/48 prescaler has maximum operating frequency in the giga hertz range (GHz). The values of P and S counters can be programmed to divide over the whole range of frequencies from 1 to 6.2 GHz with finest resolution of 1 MHz and variable channel spacing. The proposed multiband flexible divider also uses an improved loadable bit-cell for Swallow S counter and consumes in 2.4- and 5-GHz bands, respectively, and provides a solution to the low power PLL synthesizers for Bluetooth, Zigbee, IEEE 802.15.4, and IEEE 802.11a/b/g WLAN applications with variable channel spacing.

REFERENCES

[1] Yin-Tsung Hwang and Jin-Fa Lin," low voltage and low power divide by 2/3 counter design using pass transistor logic circuit technique" IEEE VLSI Trans.,vol. 20, no. 9, sep. 2012.

[2] X.-P.Yu, M. A. Do,W.M. Lim, K. S.Yeo, and J. G. Ma, "Design and optimization of the extended true single-phase clock-based prescaler," *IEEE Trans. Microw. Theory Techn.*, vol. 54, no. 11, pp. 3828–3835, Nov. 2006.

[3] Z. Deng and A.M. Niknejad, "The speed-power trade-off in the design of CMOS true-single-phase-clock dividers," *IEEE J. Solid-State Circuits*, vol. 45, no. 11, pp. 2457–2465, Nov. 2010.

[4] M. V. Krishna, M. A. Do, K. S. Yeo, C. C. Boon, and W. M. Lim, "Design and analysis of ultra low power true single phase clock CMOS 2/3 prescaler," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 57, no. 1, pp. 72–82, Jan. 2010.

[5] L. Lai Kan Leung *et al.*, "A 1-V 9.7-mW CMOS frequency synthesizer for IEEE 802.11a transceivers," *IEEE Trans. Microw. Theory Tech.*, vol. 56, no. 1, pp. 39–48, Jan. 2008.

[6] M. Alioto and G. Palumbo, *Model and Design of Bipolar and MOS Current-Mode Logic Digital Circuits*. New York: Springer, 2005.

[7] Y. Ji-ren *et al.*, "Atrue single-phase-clock dynamic CMOS circuit technique," *IEEE J. Solid-State Circuits*, vol. 24, no. 2, pp. 62–70, Feb. 1989.

[8] S. Pellerano *et al.*, "A 13.5-mW 5 GHz frequency synthesizer with dynamic-logic frequency divider," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 378–383, Feb. 2004.

[9] V. K. Manthena *et al.*, "A 1.8-V 6.5-GHz low power wide band single phase clock CMOS 2/3 prescaler," in *IEEE 53rd Midwest Symp. Circuits Syst.*, Aug. 2010, pp. 149–152.