Fpga Implementation Of Mimo-Ofdm For Baseband Modem Parallel Architecture

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Abstract: In this investigation we are proposed ultra wide band systems for MIMO-OFDM, The ultra wide band system is a high data rate, short range technology, It transmits the information over a minimum bandwidth of 500 MHZ. Modern UWB systems use Modulation techniques such as OFDM (Orthogonal Frequency Division Multiplexing). The MB- OFDM proposal is selected for UWB system model. Multiband OFDM (MB-OFDM) is a short-range wireless technology that permits data transfers at very high rates, between 53.3 and 480 Mbps. For the requirement of Multiband-OFDM system, the processor should work on a few hundred MHz, which makes it difficult to implement. And since the system targets for the wireless portable devices, small area and low power consumption are also imperative. Therefore a 8-way parallel architecture based on bi-orthogonal encoder is proposed in this paper. In order to satisfy the performance requirement, the proposed MIMO-OFDM architecture reduces the power consumption and utilize more bandwidth and also detects and corrects both random and burst errors. It is used for multiuser transmission scheme and also works at high speed. The detailed analysis shows that the proposed technique could reduce the gate count by 30% on average. With 0.18-µm CMOS process, clock rate of the entire baseband modem was about 66 MHz clock rate.

Index terms-multi-band orthogonal frequency division multiplexing (MB-OFDM,)multi input multi output(MIMO-OFDM) parallel architecture, ultra wide band (UWB), resource optimization.

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I.INTRODUCTION

Multiband orthogonal frequency-division multiplexing (MB-OFDM) is one of ultra wideband (UWB) radio standards, which provides high-speed connectivity in a wireless personal area network (PAN) [1] with specification of the data rates from 53.3 to 480 Mbps [2]. Due to the high data rates, the MB-OFDM standard requires to process large amount of computations in very short time; its modem has to compute one symbol that consists of 165 complex numbers in every 312.5 ns. Even though its performance requirement results in large hardware complexity, a low power design with small chip size is absolutely essential for applying this technology to portable handheld devices. Also, an operating frequency of a circuit is one of the dominant factors that determine power consumption. In MB-OFDM, the standard specification defines a sampling frequency of 528 MHz. Such high frequency is problematic when we use it as a system clock speed; it consumes too much power and it is hard to implement due to timing constraints. Therefore, parallel architectures have been proposed in an effort to reduce power consumption as well as to relax timing constraints [3], [4]. Exploiting parallelism with -way parallel architecture enables to keep throughput constraint at -times lower clock speeds, whereas it may increase the hardware resources by a factor of . Despite of the increased hardware resources, it is possible to reduce power consumption as well as to relax timing constraints due to two reasons. First, -way parallel architecture compensates for -times longer gate delays.

Therefore, the parallel hardware can operate at reduced supply voltages and consequently consume less power [5]. However, supply voltage scaling is beyond this paper's scope: our work focused on high level resource optimization. Second, a resource efficient design, on which this paper focuses, is able to avoid the linear, i.e., -times, resource increments. It is possible to share hardware resources among independent parallel data-paths. For example, a packet synchronizer with the cross correlation scheme requires a single set of shift

registers which holds only one OFDM symbol. Four parallel data-paths can share an output of a single coefficient generator at cost of negligible performance loss in a carrier frequency offset (CFO) compensation unit [3]. However, the topic of this paper is resource efficient designing without hurting the overall system performance at all. We used the 8-way parallel architecture in order to use 8-times lower clock frequency for saving power consumption and demonstrating our proposal on the field-programmable gate-array (FPGA)-based prototyped system. This paper is the first presentation about an 8-way parallel architecture in MB-OFDM baseband modem design which is optimized by new processing structures and algorithm reconstruction. While several 4-way parallel architectures have been already introduced [3], [4], we believe that more highly parallel systems are desirable to satisfy strong demand of battery-long operation of mobile devices. The previous literature presented only one resource optimization technique which sacrifices the overall Performance.

II.RELATED WORK

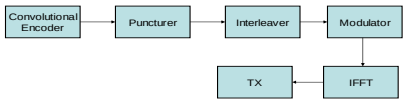
The main drawback of TDS-OFDM is that, the time-domain TS and the OFDM data block will cause IBI to each other. Thus, the iterative interference cancellation algorithm has to be used for channel estimation and equalization [7], [8], i.e., the IBI from the OFDM data block to the TS must be eliminated before the TS-based time-domain channel estimation, while the IBI caused by the TS to the OFDM data has to be removed to achieve reliable channel equalization. On one hand, the interference cancellation before channel estimation needs the equalized OFDM data information to calculate the IBI caused by the OFDM block, while on the other hand, channel estimation is prerequisite to obtain the equalized OFDM block. Therefore, channel estimation and channel equalization are mutually conditional in TDS-OFDM, and the iterative interference cancellation algorithm would suffer from high complexity as well as poor performance over fast fading channels [10].

Some alternative solutions have been proposed either to decrease the complexity or to enhance the performance [11], [12], but the performance gain is not obvious. One exciting solution to the interference problem of TDS-OFDM is the cyclic postfix OFDM scheme [13], [14], whereby the TS serving as the cyclic postfix is not independent of the OFDM block like that in TDS-OFDM, but is generated by the redundant frequency-domain comb-type pilots within the OFDM symbol. In this way, the IBI from the TS to the OFDM data block can be avoided. However, the cyclic postfix OFDM scheme does not solve the problem of the interference from the OFDM data block to the next TS, thus the iterative interference cancellation with poor performance over fast time-varying channels is still required for channel estimation and OFDM equalization [15]. In addition, the inserted redundant pilots have much higher average power than the normal OFDM data [16], thus the equivalent signal-to-noise ratio (SNR) at the receiver will be reduced if the identical transmitted signal power is permitted. Such SNR loss can be slightly alleviated by changing the positions of the redundant pilots or adding more pilots in the frequency domain [17], [18], but the effect is not obvious. The most effective solution to the interference problem of TDS-OFDM is to duplicate the TS twice, resulting in the dual-PN OFDM (DPN-OFDM) scheme [19].

The second received PN sequence immune from the interference caused by the preceding OFDM data block can be directly used for channel estimation, and the interference cancellation before channel equalization can be replaced by the cyclic prefix reconstruction which is accomplished by the simple add-subtraction operation [19]. In this way, the iterative interference cancellation algorithm could be avoided, leading to the reduced complexity and improved performance over fast fading channels. However, the spectral efficiency of the DPN-OFDM solution is remarkably decreased by the doubled length of the TS. For example, when the length of the single TS is 1/9 that of the OFDM data block, the spectral efficiency of TDS-OFDM is 90%, which is reduced to 82% in DPN-OFDM.

Therefore, to achieve high spectral efficiency and good performance over fast fading channels at the same time is really challenging for the currently available OFDM-based transmission schemes, including CP-OFDM, ZP-OFDM, TDS-OFDM, cyclic postfix OFDM, and DPNOFDM.

Tx System Model:



A.Convolutional Encoder:

Generator representation shows the hardware connection of the shift register taps to the modulo-2 adders. A generator vector represents the position of

the taps for an output. A "1" represents a connection and a "0" represents no connection. For example, the two generator vectors for the encoder are **g1** = [111] and **g2** = [101]. where the subscripts 1 and 2 denote the corresponding output terminals.

(2,1)Convolutional Codes Encoder Structure

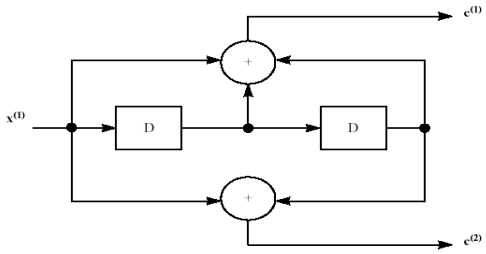


Figure.1.Convolutional Encoder

- The code rate r for a convolutional code is defined as

r=k/n

- where k is the number of parallel input information bits and n is the number of parallel output encoded bits at one time interval.

B.MRS Interleaver:

Conventional interleaver systems perform many intra sub-processes for interleaving the data. Their implementation requires dedicated memories for each step for bit permutation. Consequently this approach costs much chip resource for such storages between sub-processes and tends to have long latency for a series of the sub-processes. In order to resolve the problem, a new novel interleaving method based on mixed radix system (MRS) is proposed in this project. By applying MRS on interleaving processes, a powerful interleaver architecture was derived to perform all the three sub-processes concurrently. Its structure is a 2-D array of simple cells and each cell consists of two flip-flops with multiplexing logics.

Symmetric Structure

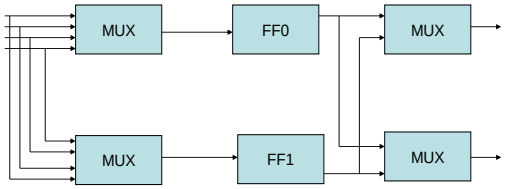


Figure.2.MRS Interleaver

C.Puncturer:

The puncturer omits some of coded bits in order to support different code rates with one convolutional encoder. Puncturer is used to increase the code rate of the designed convolutional encoder. The depuncturer inserts dummy bits for the omitted bits.

III.PROPOSED SYSTEM DESIGN

MIMO-OFDM DESIGN:

Fig.3. shows the overall architecture of the MIMO-OFDM transmitter. The proposed architecture is designed to process eight complex numbers of at one time with 8-way parallel data paths. By having the high degree of parallel data paths, the baseband modem can operate at 66MHz

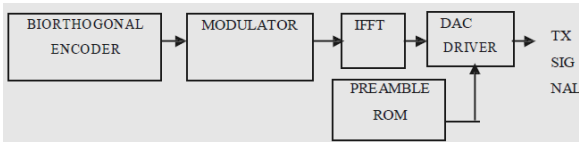


Fig 3: Overall architecture of MIMO-OFDM baseband Transmitter to use 8-way parallel data-paths.

UWB band (3432, 3960, and 4488 MHz) radio frequency (RF) signals are up/down-converted from/to baseband analog signals through RF/analog circuits And the analog signals are converted from/to digital signals by DAC and ADC at the sampling frequency of 528 MHz The DAC and ADC drivers, which are interface logics for the converters, are basically parallel-to-serial and

serial- to-parallel data converters between 66 and 528 MHz clock domains.

The preamble ROM contains complex numbers of preamble sequences to be transmitted. Based on the preamble sequence, the packet synchronizer detects a received packet. The inverse fast Fourier transform (FFT) module is used to convert the frequency domain signal to time domain[5]. It supports orthogonally. The IFFT block computes the inverse fast Fourier transform (IFFT) of each channel of a P-by-N or length-P input, u. The IFFT implementation is carried out by simply swapping the real and imaginary parts of the incoming data, performing the forward FFT and finally by swapping once again the real and imaginary parts of the data output.

The proposed novel architecture makes use of biorthogonal encoder instead of convolutional encoder. But biorthogonal encoder produces 2n-1 output for n+1 input. Also bandwidth utilization is high for biorthogonal encoder

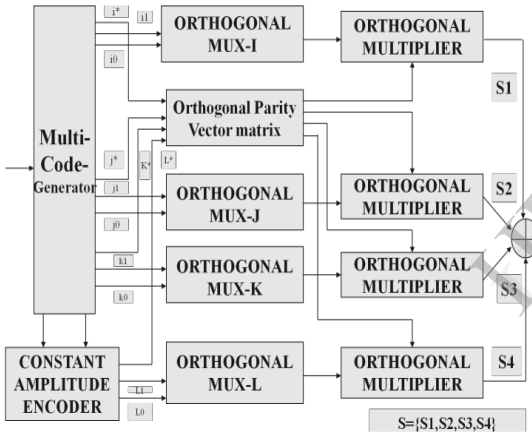


Figure.4. Biorthogonal Encoder

A multi code generator consists of Serial-to- Parallel Converter and gold convertor. The S/P Converter converts the data bits in to number of branches according to the length of Gold Sequence.

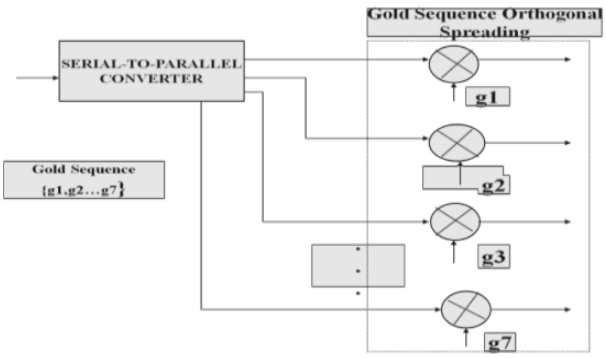


Figure.5. Multicode Generator

A Gold code, also known as Gold sequence, is a type of binary sequence. A set of Gold code sequences consists of (2^n)-1 sequences each one with a period of (2n)-1. It is generated by the exclusive-or of the two maximum length sequences of the same length in their various phases.

The output of the multicode generator consists of the (2n)-1output of the gold code sequence and n-1 dummy bits.

In this Project, MIMO can be used to achieve high data rate for wireless Communications. The Multiple transmit antennas(Multi-input-Multi output) are the important tool to improve Space diversity. Here, Space–time block coding (STBC) can achieve the Space diversity of a frequency-selective channel with N transmit and M receive antennas. STBC is the type of MIMO Architecture. Space-time coding refers to channel coding techniques for transmission with multiple transmit and receive antennas. The Space time coding can be used in Signal transmission between the Base Station's.

Space Time Trellis Code.

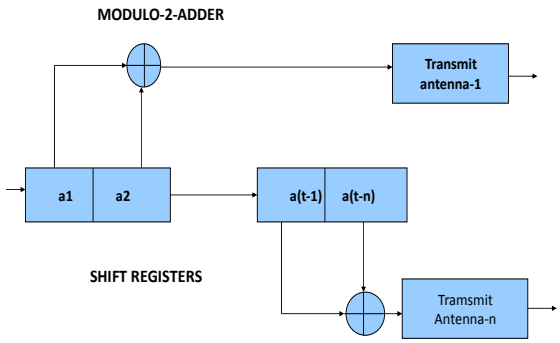


Figure 6. Space time trellis codes

Space time trellis codes operates on a one input symbol at a time and then produce a sequence of vector symbols whose length represent the number of transmit antennas. STTC are the type of space time code used in multiple antenna wireless communications. This scheme transmits multiple, redundant copies of a trellis code distributed over time and number of antennas. These multiple ,'diverse' copies of the data are used by the receiver to attempt to reconstruct the actual transmitted data. For STC to be used, there must be a multiple transmit antennas, but only a single receive antenna is required. Nevertheless multiple receive antennas are often used since the performance of the system is improved by so doing. The Number of Memory Elements (m) depends on the number of transmit antennas. The Number of Transmit antennas(N)=(m/2). The Number of receive antennas(N1)=N.

IV.SIMULATION RESULTS

In proposed architecture, the higher throughput, less power consumption and less area are achieved .The architecture is implemented using spartan3E family and XC3S500E device in Xilinx 9.2i.The proposed system is written in VHDL language and synthesized in Xilinx 9.2i and stimulated using Modelsim 5.7. Dynamic power is defined as amount of power consumed by switching activities of FF, where as static power is power consumed by leakage current. In 200MHz operation the Coprocessor consumes 79mW in static and 96mW in dynamic in the total summation of 175mW.

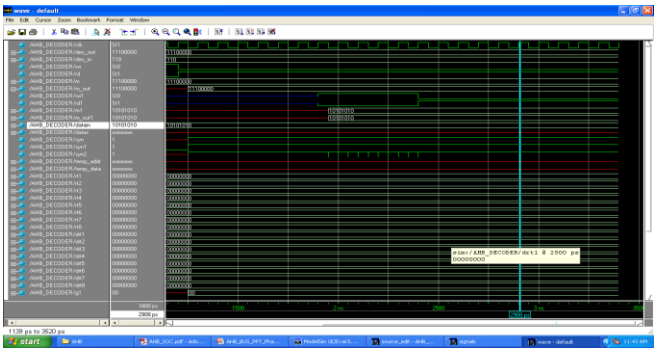


Figure.7.Simulation Result

COMPONENTS	CONVOLUTIONAL ENCODER	BIORTHOGONAL ENCODER
LUT	8	4
SLICE	4	2
GATE	117	79
NON-CLOCKNET	3.50ns	3.13ns
PATH DELAY	6.78ns	6.58ns
POWER	79.81µw	39.52µw

Table.1.Comparison between Convolutional and Bi-orthogonal Encoders

V.REFERENCES

[1] F. Adachi and E. Kudoh, "New direction of broadband wireless technology," Wirel. Commun. Mob. Com., vol. 7, no. 8, pp. 969–983, Oct.2007.

[2] X. Yuan, Q. Guo, X. Wang, and L. Ping, "Evolution analysis of lowcost iterative equalization in coded linear systems with cyclic prefixes,"IEEE J. Sel. Areas Commun., vol. 26, no. 2, pp. 301–310, Feb. 2008.

[3] B. Muquet, Z. Wang, G. Giannakis, M. De Courville, and P. Duhamel, "Cyclic prefixing or zero padding for wireless multicarrier transmissions?" IEEE Trans. Commun., vol. 50, no. 12, pp. 2136–2148, Dec. 2002.

[4] C. yen Ong, J. Song, C. Pan, and Y. Li, "Technology and standards of digital television terrestrial multimedia broadcasting," IEEE

Commun.Mag., vol. 48, no. 5, pp. 119–127, May 2010.

[5] X. Wang, P. Ho, and Y. Wu, "Robust channel estimation and ISI cancellation for OFDM systems with suppressed features," IEEE J. Sel. Areas Commun., vol. 23, no. 5, pp. 963–972, May 2005.

[6] J. Wang, J. Song, and L. Yang, "A novel equalization scheme for ZPOFDM system over deep fading channels," IEEE Trans. Broadcast.,vol. 56, no. 2, pp. 249–252, Jun. 2010.

[7] J. Wang, Z. Yang, C. Pan, and J. Song, "Iterative padding subtraction of the PN sequence for the TDS-OFDM over broadcast channels," IEEE Trans. Consum. Electron., vol. 51, no. 11, pp. 1148–1152, Nov. 2005.

[8] J. Song, Z. Yang, L. Yang, K. Gong, C. Pan, J. Wang, and Y. Wu, "Technical review on Chinese digital terrestrial television broadcasting standard and measurements on some working modes," IEEE Trans. Broadcast., vol. 53, no. 1, pp. 1–7, Feb. 2007.

[9] Framing Structure, Channel Coding and Modulation for Digital Television Terrestrial Broadcasting System. Chinese National Standard, GB 20600-2006, Aug. 2006.

[10] S. Zhou and G. Giannakis, "Single-carrier space-time block-coded transmissions over frequency-selective fading channels," IEEE Trans. Inf. Theory, vol. 49, no. 1, pp. 164–179, Jan. 2003.

[11]S. Tang, K. Peng, K. Gong, J. Song, C. Pan, and Z. Yang, "Novel decision-aided channel estimation for TDS-OFDM systems," in Proc. IEEE International Conference on Communications (ICC'08), Beijing, China, May 2008, pp. 946–950.

[12] F. Yang, J. Wang, and Z. Yang, "Novel channel estimation method based on PN sequence reconstruction for Chinese DTTB system," IEEE Trans. Consum. Electron., vol. 54, no. 4, pp. 1583–1588, Nov. 2008.

[13] J. Kim, S. Lee, and J. Seo, "Synchronization and channel estimation in cyclic postfix based OFDM system," in Proc. IEEE 63rd Vehicular Technology Conference (VTC'06-Spring), Melbourne, Vic, May 2006, pp. 2028–2032.

[14] "Synchronization and channel estimation in cyclic postfix based OFDM system," IEICE Trans. Commun., vol. E90-B, no. 3, pp. 485–490, Mar. 2007.

[15]S. Tang, K. Peng, K. Gong, and Z. Yang, "Channel estimation for cyclic postfixed OFDM," in Proc. International Conference on Communications, Circuits and Systems (ICCCAS'08), Fujian, China, May 2008, pp. 246–249.

[16] M. Huemer, C. Hofbauer, and J. Huber, "Unique word prefix in SC/FDE and OFDM: A comparison," in Proc. IEEE Global Telecommunications Conference (GLOBECOM'10), Miami, USA, Dec. 2010, pp. 1321– 1326.

[17]A. Onic and M. Huemer, "Direct vs. two-step approach for unique word generation in UW-OFDM," in Proc. the 15th International OFDMWorkshop (InOWo'10), Los Alamitos, CA, Sep. 2010, pp. 145–149.

[18] C. Hofbauer, M. Huemer, and J. Huber, "On the impact of redundant subcarrier energy optimization in UW-OFDM," in Proc. 4th International Conference on Signal Processing and Communication Systems (ICSPCS'10), Gold Coast, Australian, Dec. 2010, pp. 1–6.

[19] J. Fu, J. Wang, J. Song, C. Pan, and Z. Yang, "A simplified equalization method for dual PN-sequence padding TDS-OFDM systems," IEEE Trans. Broadcast., vol. 54, no. 4, pp. 825–830, Dec. 2008.

[20] L. Bomer and M. Antweiler, "Perfect N-phase sequences and arrays, IEEE J. Sel. Areas Commun., vol. 10, no. 4, pp. 782–789, May 1992.