FPGA Implementation of Echo Canceller for a Network Extender

Ananya Devraj
M.Tech (VLSI Design and Embedded Systems)
T.John Institute of Technology, Bangalore

Dr. Ganesh Kumar M.T
Professor & Dean (PG)
T.John Institute of Technology, Bangalore

***Abstract*— With the advent of wireless communication there has been considerable concerns regarding the quality of the communication signals and ability to communicate at all places irrespective of the distance of user equipment from the base station.**

This problem can be solved with the help of Network Extenders whose basic function is to boost the base station signals to facilitate uninterrupted communication irrespective of the user equipment distance from the base station or hand-off issue or at any weak signal areas. Thus, these days Network Extenders have become a necessity. But in the case of Network Extender, there exists a feedback path between the network extender's transmitter and receiver. This feedback path signal itself is called echo in the path. Thus an additional signal will be added along with the original signal which degrades the actual signal that is being handled. This necessitates for an echo canceller block in the Network Extender.

The logic used in the echo canceller block is called as echo cancellation logic and this is the logic that will be implemented in the present work. The echo canceller module with the help of this echo cancellation logic algorithm cancels the echo by estimating the channel through correlation and other delay estimations. In these kind of situations, generally the received signal at the Donor receive antenna (with respect to user equipment) will have the actual signal to be received from the donor side and some part of the signal from the local transmit antenna of the Network Extender/RF Repeater (which is also called as Echo signal).The addition of this local signal along with other noise signal is referred as echo signal. In this case, echo power is expected to be more than the actual received power, thus degrades the original signal.

Keywords*— *Network Extender, FPGA, Echo Canceller, Hand-off, Preamble Generation LUT, Correlation, Delay estimation, Channel estimation, Channel estimate update timing selection, Channel estimates LUT and updating, Equalization;

I. INTRODUCTION

Practically, the signals that are being transmitted from the base station are not available at all the places; Even the signal strength cannot remain as a constant high, across the area of signal availability. Due to which RF repeaters [1] is used these days. This paper concentrates about the implementation of a module design inside these network extenders also called as RF repeaters on a hardware platform mainly, where its function is to cancel the echo through correlation and delay estimation. Thus the echo canceller module performs the cancellation [2] of the echo in the system when implemented.

II. METHODOLOGY

In general the functionality of the echo canceller algorithm is mainly handled by modules named: Preamble Generation LUT (Look Up Table), Correlation, Delay estimation, Channel estimation, Channel estimate update timing selection, Channel estimates LUT and updating, Equalization. The input for the echo canceller block may be obtained from an input buffer, where the blocks of samples will already be available. The echo cancelled signal may be further used as an input for the next block (with respect to Network Extender) like Gain control, where gain can be efficiently controlled due to the cancellation of echo. The algorithm implementation can be verified through MATLAB, Simulink (software platform) and then on a FPGA (similar to [3]) using Vivado Design Suite or Xilinx Integrated Synthesis Environment (ISE).

Fig. 1 (a) shows the Echo Canceller (EC) module that can be implemented in any RF repeater with some modifications as necessary. The input given to the EC module that has echo will be cancelled with the help of correlation and estimation techniques, which is explained briefly in figure 1.1. The buffer is used to store input and output, which can be latter used for calculations. Buffer in case of hardware is referred to memory and it is BRAM with respect to the FPGA that is being used here. The FPGA referred in here in a Kintex 7 series Xilinx board. The hardware platform for implementation may also include RF transceivers.

Along with the modules in figure 1. (b), there are other modules in the design that has to be considered. Out of those is Preamble Generation LUT and this module will be used to store the reference signal. Zadoff-Chu sequence is the reference signal in this case. As the Zadoff-Chu sequence is fixed, we will be storing the sequence in the buffer so that it can be used later. In Correlation and Delay Estimation, the correlation method will be used to estimate the delay in the echo path by measuring the peaks of the correlating signals. Latter, it estimates the delay in the echo path and the phase shift of RF components. The maximum peak in the correlation result will be used to estimate delay.

In case of Channel estimation and averaging module, the channel in the echo path will be estimated from the received samples and the buffered signal. The channel estimates will be calculated for each block and averaging will be done for configured number. The averaging period can be configurable

and will be updated during the testing with hardware. When the averaging module updates the estimates, it will be used immediately for compensation. Updating the channel will be done during the calibration and whenever there is change in the echo power. To get the better channel estimates, the continuous channel estimates will be stored and averaged. The number of blocks used for channel estimation and averaging can be configured. The averaged channel estimates will be used for equalization.

The averaged channel estimates and buffered signal will be used for the equalization. The received data will have the strong component of the previously transmitted data which will be available in the buffer. So, the estimated delay will be applied on the buffered signal and equalized with the average channel estimates. This delayed and equalized signal will be subtracted from the received signal to get the echo cancelled data.

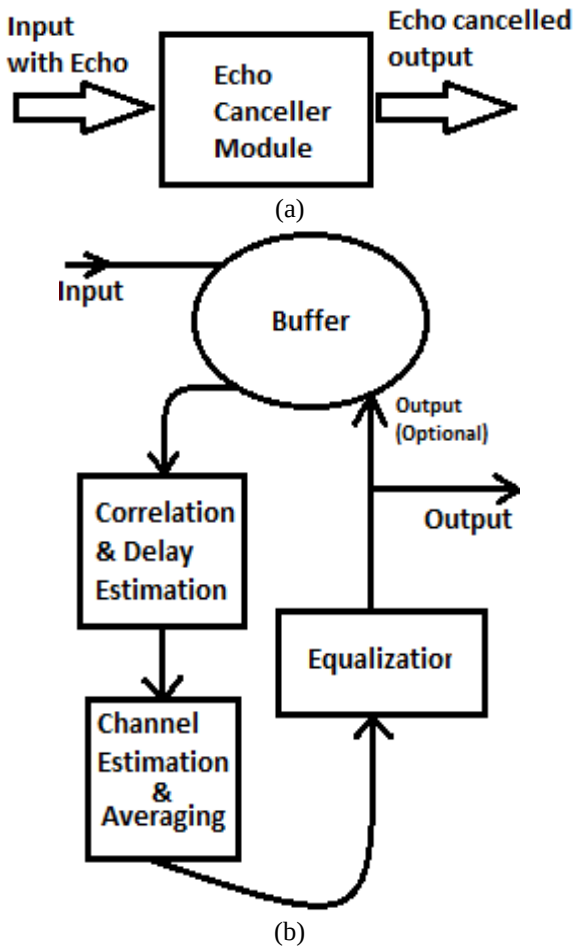

Fig. 1.(a) Echo Canceller (EC) Block Diagram (b) EC module.

III. IMPLEMENTATION

The implementation of the design is done using hardware description language, particularly using Verilog language. This requires both RTL and test bench. The simulation of the module can be obtained only with the help of test bench. The test bench provides the stimulus required for verifying the design. The EC DUT used here is verified using Xilinx ISE and ISIM. Other than this the design can be validated using Vivado design suite by Xilinx.

Based on the methodology the RTL design was implemented using Verilog language.

For implementation of the hardware platform Vivado Design Suite was used. The platform is designed in such a way as to receive any input through an RF front end transceiver, then pass those received data through the EC module in the FPGA after digitization. The output of EC module is sent back to the real world using another transceiver, which can be used for latter calculations.

The proposed hardware platform was validated using Kintex and transceiver boards form XILINX and ANALOG DEVICES INC. Where the transceivers were controlled using SDK of XILINX, where embedded C programs were used. The interface between FPGA and transceivers was through XILINX GPIOs and SPIs.

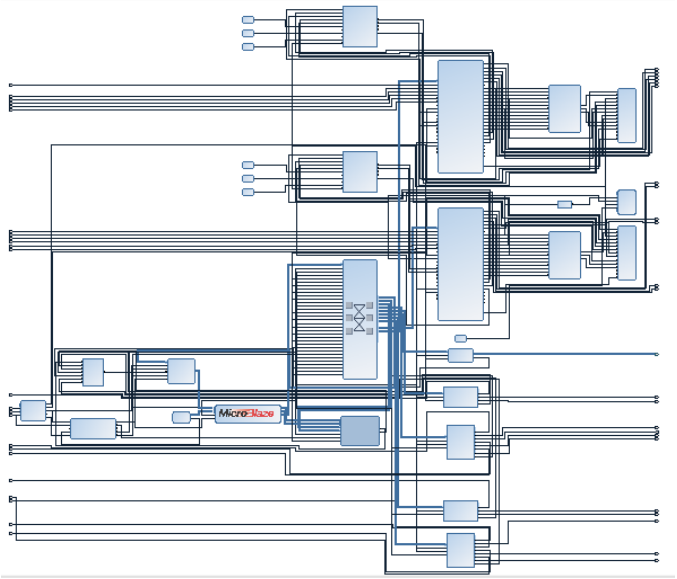

Fig. 2. General visualization of hardware platform using Vivado Design Suite.

IV. RESULTS AND CONCLUSION

In this paper we have presented the practical implemtation Echo Canceller [EC] module and the possible hardware platform solution for its implementation on the hardware.

The simulated output for the EC module is as shown figure 3. With the help of simulation, design can be verified. The verification was done by comparing the inputs given to the module with the output of the same EC module. The design helps to remove the echo caused during the usual communication process.

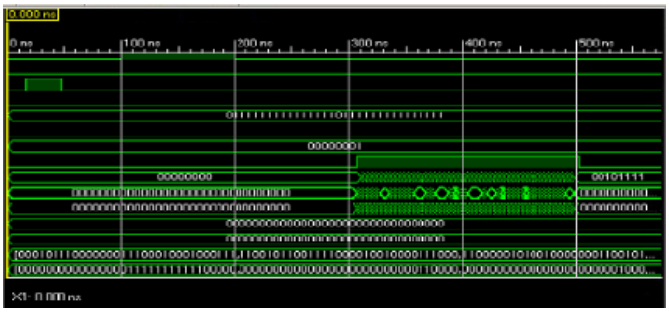

Fig. 3. Echo Canceller (EC) Block Diagram

Thus, it can be concluded that by using EC module in the RF repeater design [1], the echo can be removed effectively. Thus the overall systems efficiency also increases.

The future work will address the usage of the Echo Canceller module in a Network Extender.

REFERENCES

[1] Wu, X.W., Prosser, F.P. "CMOS ternary logic circuits," Circuits, Devices and Systems, IEE Proceedings, Feb 1990, Volume: 137 Issue: 1, pp: 21 – 27.

[2] Echo Cancellation and Application by Murano, K., Fujitsu Lab., Kanagawa, Japan; Unagami, S. ; Amano, F. IEEE 2002.

[3] FPGA Implementation of an Acoustic Echo Canceller using a VSS-NMLS algorithm by Anghel, Paleologu, Benesty, Ciochina.