

# FPGA Implementation of Binary Morphological Processing for Image Feature Extraction

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**Abstract-** The present digital world requires the need for image feature extraction from images, videos, moving object etc in the applications of medical, surveillances, authentication and automated industry inspection. The image extraction can be performed by using different digital techniques like image segmentation, image enhancement, image analysis, image restoration, image representation, image description and morphological techniques.

The mathematical morphology is a process of accepting image pixel values and performing algorithmic computations like dilation, erosion, opening and closing etc. The mathematical morphology can be designed and implemented by using software, Digital Signal Processing (DSP) and FPGA/ASIC. The Software and DSP implementations are slow in operation and cannot be used for high speed applications. Hence, FPGA implementation can be used for high speed applications. The proposed design accepts an input image from a video/ photo and converts into image pixels matrix. This image pixel array matrix of [255\*255] is structured with structuring element of [3\*3] array matrix for the mathematical morphology feature extraction. The selection of structuring element is based on the type of shapes of an image.

The proposed system is designed by using Verilog HDL, MATLAB software and implemented using Xilinx – System Generator, Xilinx ISE design tools and targeted for Spartan-3E- XC3E-500-4FG320 FPGA board.

**Keywords-** Binary Image Processing; Mathematical Morphology; Xilinx ISE System Generator; FPGA.

## I. INTRODUCTION

In Digital Image Processing, Mathematical Morphology is used for image feature extraction. The nonlinear mathematical tools can be used to manipulate the shape or understand the structure of functions or objects (clusters of pixels). The word morphology is a combination of morphe, means “form” or “shape”, and the suffix -logy, which means “the study of”. Consequently, the word morphology means the study of shapes. The technique was originally developed by “Mat heron” and “Serra” at the ‘encore des mines’ in Paris [2]. It is a theory and technique for the analysis and processing of geometrical structures, which started to develop in the late 1960s, stands as a relatively separate part of image analysis.

The Image Processing is a method to convert an image into digital form by performing operations on it for getting an enhanced image or to extract some useful information from it. The Image Processing is a type of signal distribution in which input can be image, video frame or photograph and output may be image or submerge with some characteristics. Usually Image Processing includes treating images as two dimensional signals on which set signal processing methods are applied. In Image Processing operations both the input and the output are images. Mathematical morphology is also one of the important terms in Image Processing for image feature extraction.

Generally, the word morphology refers to the scientific branch that deals with the forms and structures of images. This is middle level of image processing technique in which the input is image but the output is extracted feature from an image [2]. The language of the Morphology comes from the set theory, where image objects can be represented by sets. Hence the concept of mathematical set theory is used for extracting features from the image. Morphological image processing is a powerful tool for extracting or modifying information using the shape and structure of objects within an image. The basic design flow for mathematical morphology is shown in Fig.1.

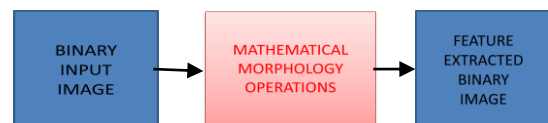


Fig.1. Design flow of Mathematical Morphology

The overall objective of this paper is design of a mathematical morphology method for image feature extractions and also performs binary morphology operations on the extracted image, for computer vision applications. The overall design theory of mathematical morphology used in digital image processing and the design architecture of binary mathematical morphology processing are explained in section II. The section III describes about the system level mathematical morphology design flow and simulation results of Xilinx System generator. The section IV gives the design analysis and simulation results of mathematical morphology operators algorithms using Xilinx ISE design suite on Spartan 3E FPGA. The conclusion is presented in section V followed by references.

## II. BINARY MORPHOLOGY PROCESSING

In the Image processing applications the Image feature extraction can be done by using a human eye. However, unlike humans, who are limited to the visual band of the Electro Magnetic (EM) spectrum, imaging machines with the help of computer vision can extract maximum features of an image. The image feature extraction is the mixture of image processing and computer vision for digital images. The Digital image is composed of a finite number of elements, each of which has a particular location and value called as picture elements or image elements or pels or pixels. One example of image to pixel conversion is shown in Fig 2.

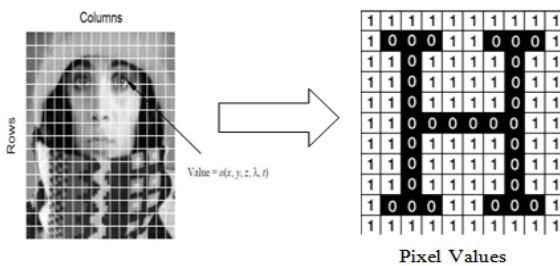


Fig.2. Image pixel generation

In Digital Image Processing the digital image feature extraction can be done by using the methods whose outputs are either images or attributes extracted from the images. The mathematical morphology is a tool for extracting or modifying information on the shape and structure of objects within an image. The Morphological operators, such as dilation, erosion are particularly useful for the analysis of binary image feature extraction. The basic block diagram of binary morphology is as depicted below in Fig 3.

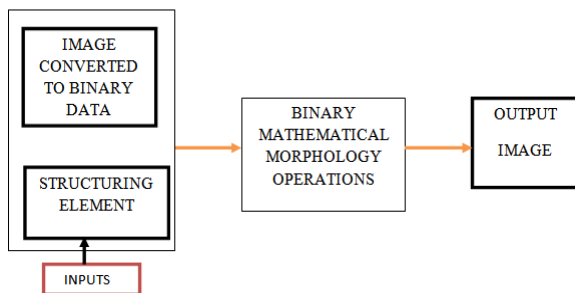


Fig.3. Basic Block Diagram of Binary Morphology

The image feature extraction can be done by using two steps. i.e. First, extract the binary pixels data of an image using segmentation. Second, apply the binary morphology algorithm on segmented image and then reconstruct the feature extracted image. This design flow of morphology process for image feature extraction is shown in Fig.4.

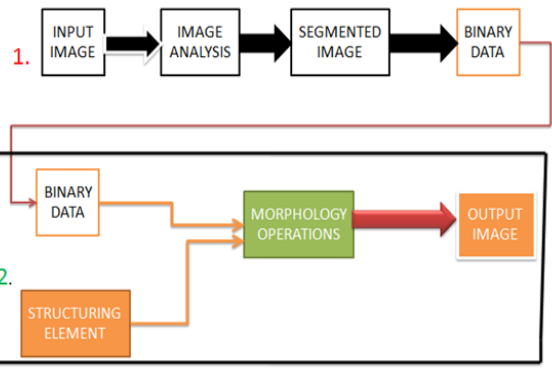


Fig.4. Design Flow of Morphology based Digital Image Extraction

In first phase of design flow the input image is analyzed and segmented to get binary pixels data. This binary data can be structured with structuring element according to the type of application and required feature that is to be extracted. The structuring element consists of a 0's and 1's matrix patterns specified as the coordinates of a number of discrete points suitable to some origin. These structuring elements can be a 3x3 or 5x5 or 7x7 array of matrices. The centre pixel of the structuring elements is called the origin and it identifies the pixel of the interest of the pixel being processed. The pixels in the structuring elements containing 1's define the neighbourhood of the structuring element. The matrix size is selected based on neighbourhood pixel relationships.

### A. MORPHOLOGY OPERATORS

There are four morphological operations to extract the feature of an image. They are Dilation, Erosion, Opening and Closing. The dilation adds the number of white pixels with the help of logic 1's. The Erosion deletes the white pixels with the help of logic 0's. The opening operation can be done by using first erosion and then dilation. The closing is reverse of opening operator. Based on the required feature extraction and type of structuring element the type of morphology operator will be selected. [1] The block diagram of binary morphology algorithm using structuring element and the operators is shown in Fig.5.

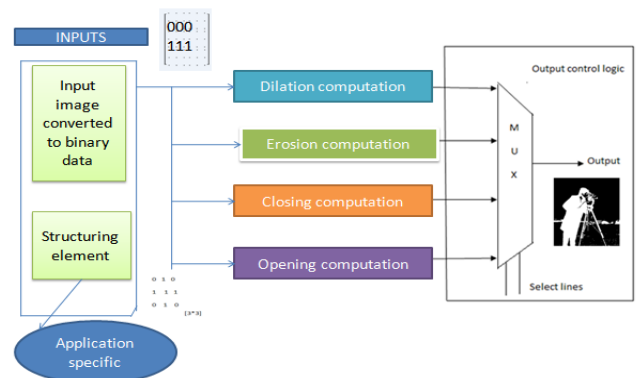


Fig.5. Block diagram of morphology algorithm using morphology operators

### III. DESIGN ANALYSIS OF BINARY MORPHOLOGY PROCESSING

The binary morphology processing algorithm for [255x255] digital image size and [3x3] structuring element is designed using Xilinx System Generator, MATLAB and Xilinx ISE Design suite and targeted for Xilinx Spartan 3E FPGA board. The basic flow chart for the proposed design is shown in Fig.6.

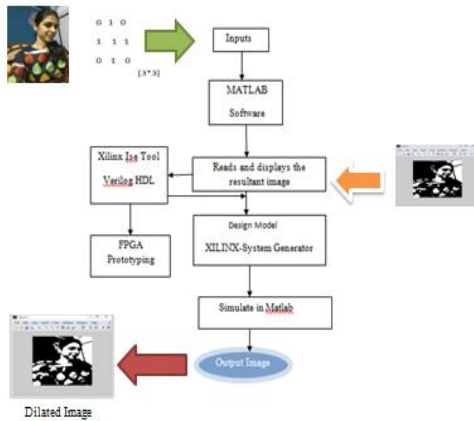


Fig.6. Flow chart for Implementation of Binary Morphology Processing

The image is considered as input to the MATLAB and then pixel values in matrix form are generated. The generated pixel values along with the structuring element are given as inputs to the Xilinx FPGA Implementation system of Binary morphology algorithm. The Xilinx System generator module is created for the given MATLAB pixels data to integrate Xilinx FPGA morphology design with segmented image feature extraction designs.

The MATLAB image input and the selected structuring element is shown in Fig.7.

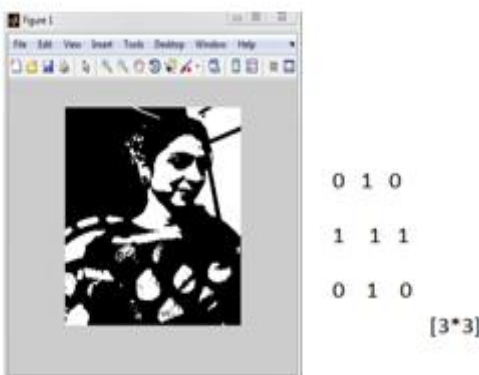


Fig.7. Input Image and Structuring element

The pixel values for the selected input image are shown in Fig.8.

```
x =
Columns 1 through 15
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
0 0 0 0 0 0 0 0 0 0 0 0 0 0 0
```

Fig.8. Pixel values of the input image

The detailed design model for all morphological operators for image feature extraction is shown in Fig.9.

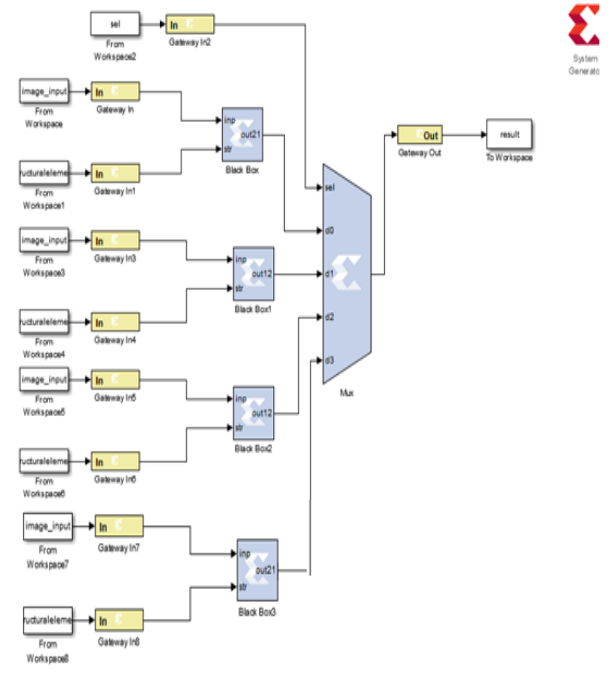


Fig.9. Proposed Morphology Operators System

The selection of morphological operator and their selection lines are given in Table 1.

Table 1. Morphological Operation selection

Selection lines	Operation
00	Dilated output
01	Eroded output
10	Opening output
11	Closing output

### IV. FPGA IMPLEMENTATION AND SIMULATION RESULTS

The proposed binary morphology processing operators of system generator blocks are designed using Verilog HDL, Xilinx ISE and implemented using Spartan 3E FPGA. All the basic individual morphological operators are synthesized and simulated for different input test vectors. The list of design tools and design entries are given in Table 2.

Table 2. Design Tools

Design Action	Tool Name
Design Entry	Verilog HDL
Synthesis	Xilinx Synthesis Tool(XST)
Simulation	ISE Simulator, MATLAB
Implementation	FPGA Editor, Plan Ahead
FPGA Configuration	iMPACT
Target Device	
Generating image/pixels	MATLAB
FPGA Board	XC3E-500-FG320-4

The design models for dilation, erosion, opening and closing are designed using Xilinx System Generator and Xilinx ISE Design tools. The design model for dilation, erosion operator and its RTL schematic are shown in Fig.10, Fig.11, Fig.12, Fig.13 respectively.

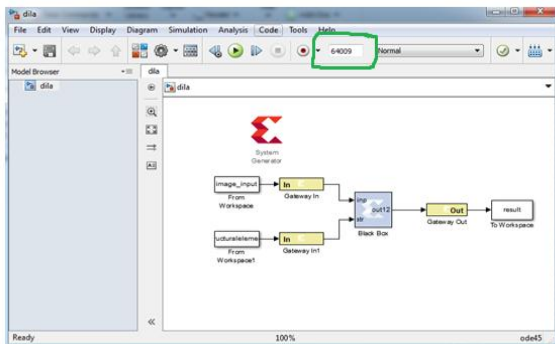


Fig.10. Design Model of Dilation Operation

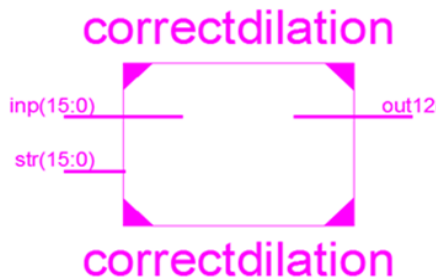


Fig.11. RTL-Schematic of Dilation

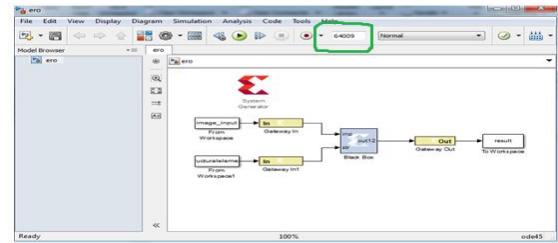


Fig.12. Design Model of Erosion Operation



Fig.13. RTL-Schematic of Dilatin

The FPGA simulation results for dilation, erosion, opening and closing operations using structuring element as 010111010 are shown in Fig.14 a, b, c, d respectively.

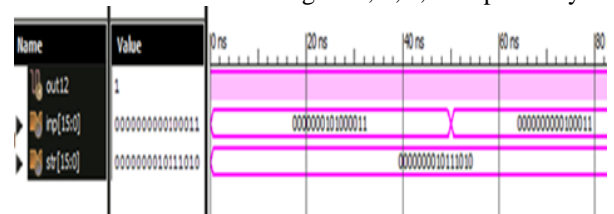


Fig.14a. Simulation Results of Dilation

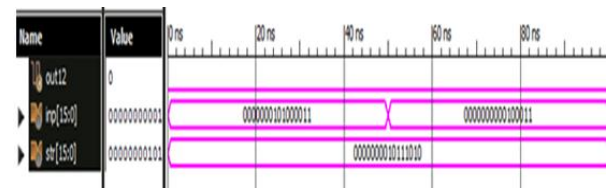


Fig.14b. Simulation Results of Erosion



Fig.14c. Simulation Results of Opening

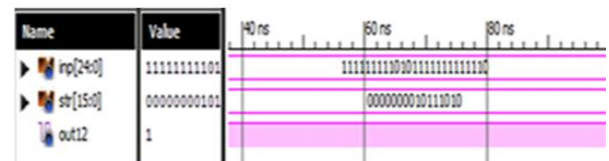


Fig.14d. Simulation Results of Closing



The result of morphology operators such as dilation, erosion, opening and closing for the test input shown in Fig.7 is shown in Fig.15 a, b, c, d respectively.

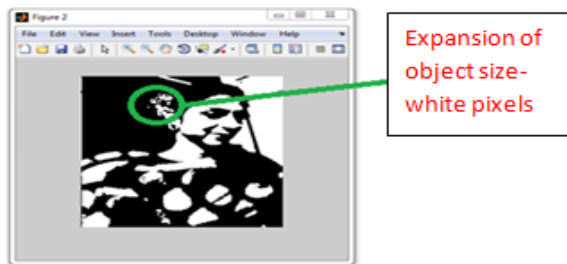


Fig.15a. Simulated Results of Dilation (Dilated)

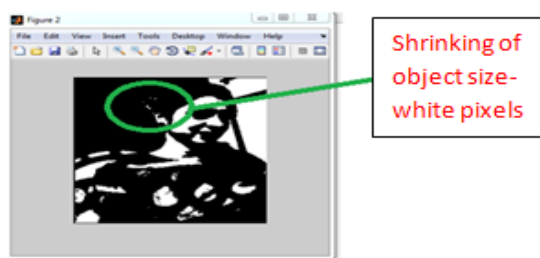


Fig.15b. Simulated Results of Erosion (Eroded)

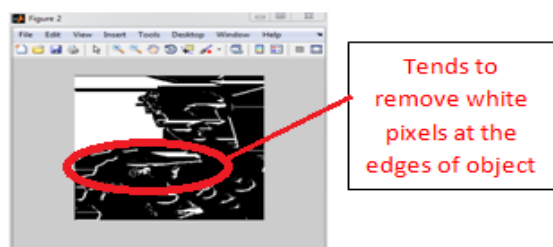


Fig.15c. Simulated Results of Opening (With noise)

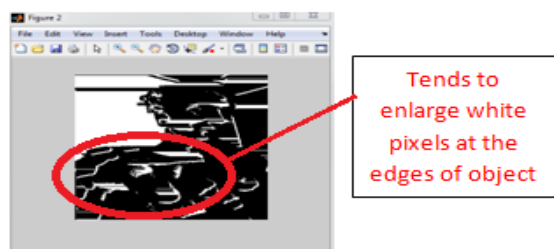


Fig.15d. Simulated Results of Closing (With noise)

The design of morphology dilation operation is verified on Spartan 3E, XC3E-500-4G320. The output of dilation operation on Spartan 3E FPGA board with bouncing pattern of LED's indicating the different values of dilation output for the given test input is shown in Fig.16



Fig.16. Output of Morphology Dilation operation on Spartan 3E-XC3E-500-4FG320 Evaluation board

### V.CONCLUSION

The mathematical morphology operators for dilation, erosion, opening and closing for image feature extraction is designed and implemented using Xilinx ISE and System Generator for Spartan-3E FPGA platform. The simulation results for all morphological operators and the implementation results for different test input images are observed and analyzed for performance improvements mainly in biomedical applications such as detection of tumours and in counting of blood cells.

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