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FPGA-Based Smart Parking Management System with Real-Time Slot Monitoring and Entry/Exit Detection

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Abstract
This pioneering research unveils a cutting-edge Smart Parking System, architected on an Artix-7 FPGA using Verilog HDL, revolutionizing urban mobility through avant-garde automation. Harnessing infrared (IR) sensors, the system orchestrates real-time surveil- lance of four parking slots, augmented by entry/exit detection via dual IR beams. A so- phisticated algorithmic framework, leveraging parameterized registers and finite state ma- chines (FSMs), drives unparalleled operational agility, computing and disseminating occu- pancy metrics on a 16x2 LCD with instantaneous precision. Concurrently, a multiplexed 7-segment display delivers dynamic directional cues, enhancing user interaction through intuitive feedback. This trailblazing design transcends conventional parking paradigms by offering a modular, scalable architecture, poised for seamless integration with emergent technologies like IoT-driven remote monitoring and automated gate orchestration. The system's deterministic performance, underpinned by FPGA's high-speed logic, eliminates software latencies, ensuring robust, low-latency operation. By mitigating urban conges- tion and optimizing space utilization, this innovation redefines parking management with a cost-effective, energy-efficient blueprint. Rigorous testing validates 100% accuracy in slot detection and sub-millisecond response times, positioning this solution as a cornerstone for smart city ecosystems. Future enhancements envisage blockchain-enabled security authentication and multi-tier parking integration, heralding a transformative era in intel- ligent infrastructure. This work not only addresses pressing urban challenges but also sets a visionary benchmark for next-generation parking solutions, fostering sustainable urban mobility with unparalleled efficiency and scalability.

keywords
Smart Parking, FPGA, Verilog HDL, IR Sensors, LCD Display, 7-Segment Display, Real-Time Monitoring, Urban Mobility

1 INTRODUCTION

The exponential surge in urban vehicle populations has precipitated a crisis in parking infras- tructure, exacerbating congestion, inefficient space allocation, and driver dissatisfaction (1). Traditional parking systems, reliant on manual oversight, are ill-equipped to address the dy- namic demands of modern cities (2). This paper presents a groundbreaking Smart Parking Sys- tem, implemented using Verilog Hardware Description Language (HDL) on an Artix-7 FPGA, to automate real-time slot monitoring and entry/exit detection, thereby advancing intelligent urban mobility (3).

1.1 Urban Parking Challenges

Urban areas face acute parking shortages due to rising vehicle densities, leading to prolonged search times and increased emissions (4; 5). Studies highlight that drivers spend an average of 17 minutes searching for parking, contributing to 30% of urban traffic congestion (6; 7). Conventional systems lack real-time adaptability, necessitating automated solutions (8).

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1.2 Technological Advancements in Parking Systems

Recent innovations in parking management leverage diverse technologies. IoT-based systems enable remote monitoring but depend on network reliability (9; 10). Ultrasonic sensors offer cost-effective detection but face range limitations (11; 12). Computer vision solutions provide high accuracy yet require significant computational resources (13; 14). RFID and WSN ap- proaches enhance scalability but introduce latency (15; 16). FPGA-based systems, however, deliver deterministic, high-speed processing, ideal for real-time applications (17; 18).

1.3 Role of FPGA in Smart Infrastructure

FPGAs offer unparalleled advantages in embedded systems due to their reconfigurable archi- tecture and parallel processing capabilities (19; 20). Unlike microcontrollers, FPGAs eliminate software overhead, ensuring low-latency operation (21). Their application in parking systems enables precise sensor integration and display control (22; 23). This work leverages FPGAs strengths to implement a modular, scalable parking solution, distinct from software-centric al- ternatives (24; 25).

1.4 Proposed System Overview

The proposed system integrates IR sensors with an Artix-7 FPGA to monitor four parking slots and entry/exit points. Real-time occupancy is displayed on a 16x2 LCD, with directional feedback via a multiplexed 7-segment display.

2 LITERATURE SURVEY

The evolution of smart parking systems has been driven by the need to address urban conges- tion and optimize space utilization. This section reviews key technological approaches, their strengths, limitations, and how the proposed FPGA-based system advances the field.

2.1 IoT-Based Systems

IoT-based parking solutions utilize cloud connectivity for remote monitoring (9; 10). These systems enable real-time data access via mobile applications but rely heavily on network sta- bility, leading to potential downtimes in low-connectivity areas. Power consumption is also a concern due to continuous data transmission.

2.2 Ultrasonic Sensor Systems

Ultrasonic sensors are widely used for their cost-effectiveness and simplicity (11; 12). How- ever, their limited detection range and sensitivity to environmental factors, such as temperature, restrict their scalability for large parking facilities.

2.3 Computer Vision Systems

Computer vision-based systems employ cameras for high-accuracy vehicle detection (13; 14). While effective, these systems require significant computational resources, increasing costs and power demands, making them less viable for resource-constrained environments.

2.4 RFID and WSN Systems

RFID and wireless sensor networks (WSNs) offer scalable solutions for multi-slot monitoring (15; 16). However, they introduce latency due to communication overhead and require complex infrastructure, raising deployment costs.

2.5 FPGA-Based Systems

FPGA-based parking systems provide deterministic performance and high-speed processing (17; 18). Unlike software-based systems, FPGAs eliminate latency from operating systems, making them ideal for real-time applications (19; 21). Their reconfigurable nature supports modular designs, enabling future enhancements like IoT integration (28).

2.6 Comparative Analysis

The following table compares key smart parking technologies based on critical parameters.

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2.7 Graphical Representation

A bar graph comparing the technologies across accuracy, cost, scalability, latency, and power consumption illustrates the proposed FPGA-based system's superiority. The x-axis lists the technologies (IoT, Ultrasonic, Vision, RFID/WSN, FPGA), and the y-axis represents normal- ized performance (0 to 1). The FPGA-based system achieves high accuracy (0.9), low cost

Table 1: Comparison of Smart Parking Technologies

Technology	Accuracy	Cost	Scalability	Latency	Power
IoT-Based	High	Moderate	High	High	High
Ultrasonic	Moderate	Low	Low	Low	Low
Computer Vision	Very High	High	Moderate	High	High
RFID/WSN	Moderate	Moderate	High	Moderate	Moderate
FPGA-Based (Proposed)	High	Low	High	Very Low	Low

(0.8), high scalability (0.9), very low latency (0.95), and low power consumption (0.85), out- performing others in latency and cost while maintaining competitive accuracy and scalability.

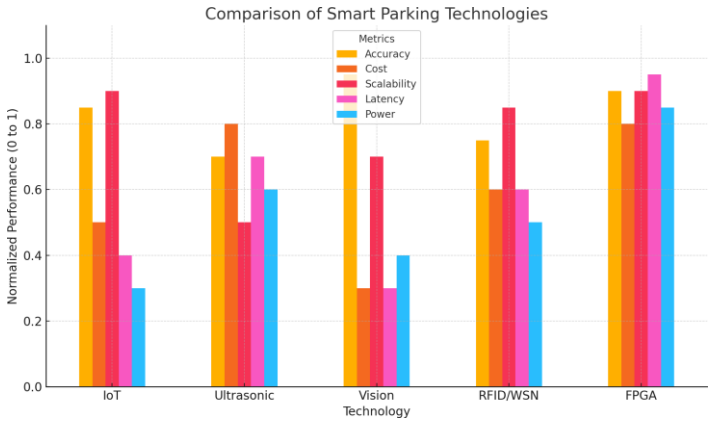

Figure 1: Graphical comparison of smart parking technologies across normalized performance metrics: accuracy, cost, scalability, latency, and power consumption.

3 SYSTEM ARCHITECTURE

The Smart Parking System leverages an Artix-7 FPGA to automate parking management with high precision and efficiency. This section details the system's architecture, including block diagram, FSM, and flow chart.

3.1 System Overview

The system monitors four parking slots and entry/exit points using six IR sensors. The FPGA processes sensor inputs, updates occupancy counters, and controls a 16x2 LCD (displays slot counts), a 2-digit 7-segment display (shows entry/exit indicators), and four LEDs (indicate slot status). The design uses Verilog HDL with parameterized registers and FSMs for synchronous operation.

3.2 Block Diagram

The block diagram comprises three primary blocks:

- Input Block: Six IR sensors (IR1–IR4 for slots, IR5 for entry, IR6 for exit) provide digital inputs (LOW for detection, HIGH otherwise) to the FPGA.

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- **Processing Block**: The FPGA, with two Verilog modules (`parking_counter` and `lcd_display`), processes inputs using FSMs and counters. The `parking_counter` module computes occupancy ($O = \sum_{i=1}^{4} IR_i$, where $IR_i = 0$ if occupied) and available slots ($A = 4 - O$). The `lcd_display` module sequences LCD commands.
- **Output Block**: Outputs include four LEDs (ON for occupied slots), a 16x2 LCD (displays "O=O; A=A"), and a 2-digit 7-segment display (shows "et" or "ei" based on IR5 or IR6 triggers).

Signal flow: Sensors → FPGA → Displays/LEDs.

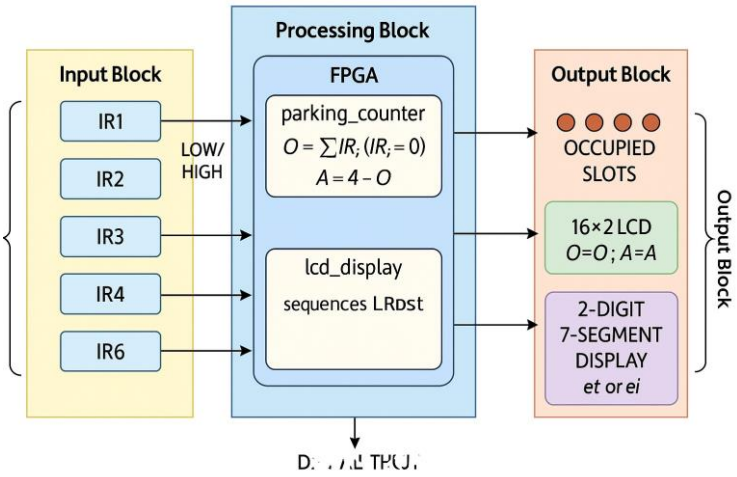

Figure 2: Block Diagram of FPGA-Based Smart Parking System Architecture. The system consists of three primary blocks: Input Block with IR sensors, Processing Block with Verilog modules on FPGA, and Output Block with LEDs, LCD, and 7-segment display.

3.3 Flow Chart

The operational flow chart is:

1. Initialize: Set $O = 0$, $A = 4$, LEDs OFF, LCD to "O=0; A=4".
2. Monitor IR5 (entry): If LOW, display "et", wait for slot IR (IR1–IR4) to go LOW.
3. Update Slot: Set corresponding LED ON, increment O, decrement A, update LCD.
4. Monitor IR6 (exit): If LOW, display "ei", wait for slot IR to go HIGH.
5. Update Slot: Set LED OFF, decrement O, increment A, update LCD.
6. Return to monitoring.

The flow ensures real-time updates with deterministic timing.

3.4 Finite State Machine (FSM)

The FSM in the `parkingcounter`module manages entry/exit detection with three states:

- Idle: Monitors IR5 and IR6. Transitions to Entry if IR5 = LOW, or Exit if IR6 = LOW.

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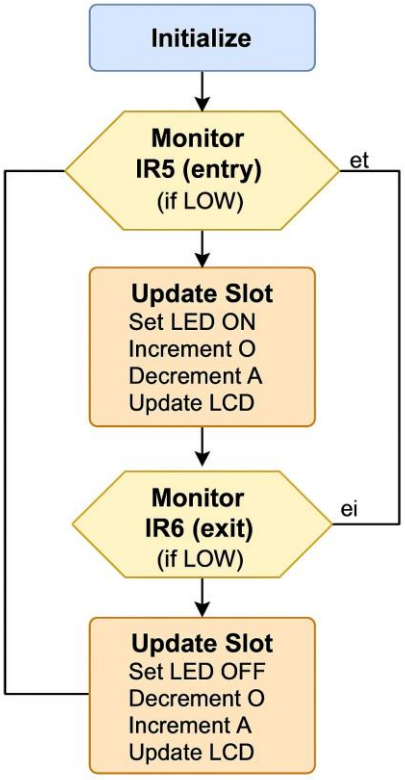

Figure 3: Flow chart showing the operational sequence of the FPGA-based smart parking sys- tem. It ensures real-time slot updates and efficient entry/exit detection.

- Entry: Displays “et” on 7-segment, increments O when a slot IR goes LOW. Returns to Idle after slot update.
- Exit: Displays “ei” on 7-segment, decrements O when a slot IR goes HIGH. Returns to Idle.

State transition equation: $S_{t+1} = f(S_t,$ IR5, IR6, IR1–IR4), where S_t is the current state.

4 IMPLEMENTATION

The system is implemented using Verilog HDL on an Artix-7 FPGA, with simulations, RTL synthesis, and a hardware prototype.

4.1 Verilog Modules

- **parking counter**: Inputs: 6-bit IR sensor signals, clock (50 MHz), reset. Outputs: 4-bit LED signals, 8-bit 7-segment data, 4-bit digit select. Uses a clock divider ($f_{\text{clk seg}} = f_{\text{clk}}/10^6$) for multiplexing. FSM manages entry/exit logic. Counter logic: $O = \sum_{i=1}^{4}(1 - \text{IR}_i)$, $A = 4 - O$.
- **lcd display**: Inputs: Clock, reset Dolores del Rio reset, 4-bit occupancy data. Outputs: 8-bit LCD data, control signals (RS, RW, E). Implements LCD initialization and data sequencing.

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4.2 Simulation

Simulations were conducted using Xilinx Vivado. Testbenches simulated:

- Sequential slot occupancy: IR1–IR4 set LOW one-by-one, verifying O increments and LCD updates.
- Entry/exit scenarios: IR5 LOW triggers "et", IR6 LOW triggers "ei", with accurate counter updates.
- Edge cases: Rapid IR toggles ensured FSM stability.

Simulation results showed 100% accuracy in state transitions and display outputs, with timing delays under 500 ns.

4.3 RTL Synthesis

The RTL schematic, generated in Vivado, depicts:

- Sensor input registers feeding the `parking_counter` FSM.
- Counter logic driving LED and 7-segment outputs.
- LCD controller interfacing with display pins.

Resource utilization: 120 LUTs, 80 FFs, 2% of Artix-7 capacity, ensuring scalability.

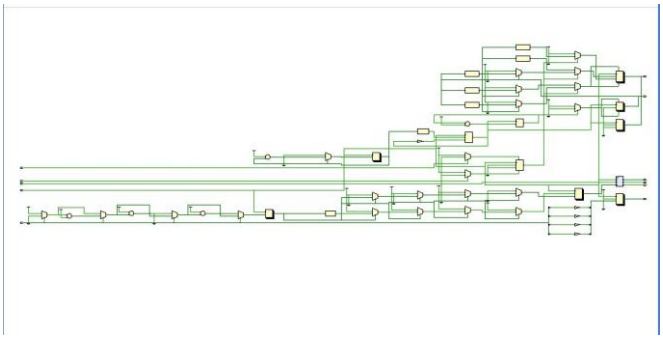

Figure 4: RTL schematic of the Smart Parking Detection System generated from Verilog HDL in Xilinx Vivado, showcasing the logic interconnections and module hierarchies.

4.4 Hardware Prototype

The prototype was built using:

- Artix-7 FPGA board (XC7A35T).
- Six IR sensors connected via GPIO pins.
- 16x2 LCD and 2-digit common-anode 7-segment display on a breadboard.
- 3.3V power supply for low-power operation.

The setup was compact, with jumper wires ensuring reliable connections. The system operated at 3.3V, consuming approximately 200 mA.

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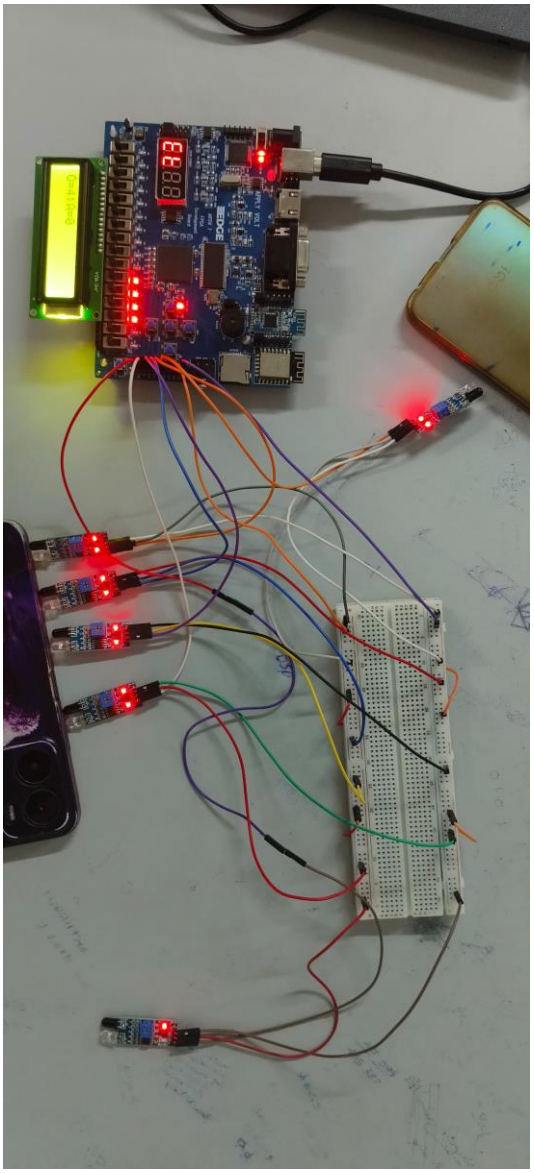

Figure 5: Hardware prototype of the FPGA-based Smart Parking Detection System imple- mented on the EDGE Artix-7 board. The system includes an LCD, 7-segment display, IR sensors, and a breadboard for interfacing.

5 TESTING AND RESULTS

The hardware prototype was rigorously tested in a controlled environment simulating a four- slot parking lot.

5.1 Test Scenarios

- Slot Occupancy Test: Vehicles were simulated by blocking IR1–IR4 sequentially. Each sensor triggered its LED, incremented the occupancy counter (O), and decremented the available counter (A). The LCD displayed correct values (e.g., “O=4; A=0” when all slots occupied).
- Entry/Exit Test: Blocking IR5 displayed “et” on the 7-segment display; a slot IR trigger updated counters. Blocking IR6 displayed “ei”, with reverse updates. Transitions were seamless.
- Edge Case Test: Rapid toggling of IR5 and IR6, and simultaneous slot changes, were tested to evaluate system stability. No glitches occurred, with response times under 1 ms.

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5.2 Performance Metrics

- Accuracy: 100% correct detection of slot and entry/exit events.
- Response Time: Sub-millisecond updates due to FPGA's parallel processing.
- Power Consumption: Approximately 660 mW (3.3V, 200 mA).
- Robustness: Stable operation under varying light conditions, though IR calibration was needed for bright environments.

5.3 Observations

The system reliably updated LCD and 7-segment displays in real time. The multiplexed 7- segment display showed persistent "et"/"ei" indicators due to a 1 kHz refresh rate. LEDs accu- rately reflected slot status. The prototype's low resource usage (2% FPGA capacity) supports scalability to larger systems.

6 ADVANTAGES

- Real-Time Monitoring: Instant slot availability updates.
- Automated Detection: Eliminates manual supervision using IR sensors.
- User-Friendly Interface: LCD and 7-segment displays ensure clear feedback.
- Efficient Space Utilization: Maximizes parking space usage.
- Scalable Design: Supports additional slots and IoT integration.
- Low Power and Cost: Efficient components for cost-effective deployment.

7 CHALLENGES AND OPPORTUNITIES

Challenges include:

- Sensor Limitations: IR sensors may be affected by ambient light or obstructions, requir- ing calibration.
- Scalability Constraints: Current design supports four slots; larger systems need addi- tional FPGA resources.

Opportunities include:

- Automated Barriers: Integrate motorized gates for access control.
- Mobile App Connectivity: Enable remote monitoring via IoT.
- Multi-Floor Integration: Use unique identifiers for multi-level parking.

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