FPGA based IP Core for High Performance Ethernet Frames

Vidya B H
Electronics and Communication
Sri Siddhartha Institute of Technology
Tumkur, Karnataka

C K Raju
Computer Science
Sri Siddhartha Institute of Technology
Tumkur, Karnataka

Abstract **- Millions of people all over the world are using internet for sharing information. Therefore information access has become important asset, which demands reliable and effective tools for processing information. Networking is a technology used to share information between systems. As the number of connection between systems increases the IP address used increases, the number of servers, routers also increases. This results in demand for advanced architecture for networking. Application specific processors are used as a solution to increased demand , but the draw back with Application specific processors is it needs low power consumption, high performance and it is not flexible to changes when General purpose processors is used. it fails in debugging and difficulty in testing. Therefore to overcome the draw backs FPGA is used to design Domain specific processor. In this project Ethernet packet processor (EPP) is designed which acts as Domain specific process.EPP is used to generate frames for Analyzers, which can take the form of SoC. the generated frame is captured using Wireshark.**

Keywords - Ethernet,SoC,FPGA,WIRESHARK,Analyzers,IP.

I. INTRODUCTION

In today's modern era, the basis for communication is through emails, online news paper blogs, social networking blogs and other internet services. Day by day demand for networking is widely increasing due to advancement in networking technology which facilitates fast communication and easy resource sharing. The dominant technologies managing networking in today's communication world are Ethernet and IP. Ethernet and IP technologies transports and manages packets at high speed .In order to achieve different speeds like 1/10/20/40/100 gigabits electrical and optical interfaces are used. After interfacing packets, they are processed using hard ware solution which adds new capabilities it. Packets are formed by assembling the frame at transmitter and decoding frame at receiver. Network layer adds header and trailer to the assembled frames.

During the process of frame formation the first segment is addition of start of frame delimiters (SFD), SFD are bits which indicates receiver that the coming bits are frames. SFDs are mainly used for synchronization between receiver and transmitter. Before transmitting the frames, headers and footers are added the process is called frame encapsulation. In order to ensure that the frame can reach the target address properly physical media access control address is added as header to the frames. The trailers of the frame consist of frame check sequence. Cyclic Redundancy Check is the Frame check sequence used in Ethernet frame generation.

At the end of each Ethernet frame the cyclic redundancy sequence is added. At transmitter side before transmitting the CRC of the frame is calculated, the CRC is calculated for the bits starting from destination address bits of the Ethernet frame till the data bits, CRC is calculation is therefore done for destination address bits, source address bits, type bits and data bits. At the receiver the CRC is calculated for received frame. If the condition associated with CRC is satisfied then the frame is transmitted to the next destination or upper layer for processing. If the resultant value does not satisfy the condition then negative acknowledge is sent to the source address. Fig 1 shows Ethernet Frame Format [1]

PREAMBLE	SFD	DA	SA	TYPE	DATA	CRC
7 octet	1octet	6octet	6octet	2octet	46-15600OCTET	4 octet

Fig 1: Ethernet Frame Format [1]

The different fields in Ethernet frame format is as shown in fig 1.

First seven bytes in the frame are called Preamble. It consists of alternating sequence of ones and zeros that will inform the receiving point that a frame is coming, and helps in synchronization of frame [1].

After preamble comes one byte Start-Of-Frame Delimiter. The start of frame consist of alternating pattern of ones and zeros, along with two consecutive ones .which indicates that the next bit following it is the left most bit of destination address [1].

Third field is Destination address which is of one byte. The Destination address field consists of address bits of the destination where the frame should reach. Fourth field are Source addresses which is of one byte. The Source address field consists of address bits of the Source from where the frame arrived [1].

Fifth field is Type field it is of two bytes. This field consists of MAC- data bytes in the data field of the Ethernet frame; it can be used to identify type of frame version [1].

Sixth field is Data field it is a group of bytes ranging from 46 to 1500 bytes [1].

Seventh field is frame check sequence it is of four bytes. This sequence contains a 32-bit cyclic redundancy check [1].

A. *System on Chip (Soc)*

- System on chip is concept of including different functionality in side single chip.
- Embedded system applications require the concept of system on chip.
- As the design complexity is more and also due to the power consumption issue ASP processors cannot be integrated in SoC.
- SoC can inhibit the properties of different operating systems

B. *Objective*

- Generating Ethernet frame of desired length.
- FPGA is used to provide high speed processing.
- To provide design with high performance, low power and high degree of programmability which results in domain specific processors
- Capturing the generated frames in FPGA using WIRESHARK

C. *Motivation*

- With the advanced networking technology.
- Ethernet and IP technologies are becoming mandatory for networking.
- Data transmission speed is changing from mega bits per second to giga bits per second range.
- Therefore necessity of improved networking technology is increasing.
- Improved technologies add strength to the frame.
- This can result in improved speed and performance

D. *Problem description*

In today's networked era increased network traffic, drives demand for increased high speed Internet which in tern drives the need for large data transmission , real time communication over IP and High Definition multimedia transferring over IP and VoIP applications, is declining the capacity of communication media [2]. Therefore the internet based network architecture design must evolve. Application specific processors expects high through put, low power consumption, high degree of programmability, include lacking flexibility for changes, difficulty to test and debug is the limitation in many general processor based applications[3].

E. *Solution to the problem*

- Designing of SoC based EPP.
- VHDL coding is used for designing and implemented in SP605 FPGA.
- Main packet processing tasks like fragmenting and decoding is done by EPP.
- In order to achieve high throughput pipelined and parallel deigning concept is used
- As a result high speed can be achieved.
- EPP can be used as SoC application and can be used as IP core

F. *Methodology*

The coding for the project is written in VHDL language. CRC, SFD, IFD, Frame Count, SRC MAC, DST MAC, L2, and L3 are the coding parts. Once coding is done next step is synthesizing of VHDL code and simulating using Xilinx 14.2. After synthesis, it is implemented on FPGA using SP605 family.

1) The project requirements are:
2) Xilinx 14.2 software
3) FPGA ,SP605
4) PHY 10/100/1000 Mbps chip
5) RJ45 connector
6) Keypad
7) LCD Display

II. SYSTEM DESIGN

System designs consist of designing different parts of the project using VHDL code. The major components used in designing the system are rj45 connector which connects the Ethernet cable, PHY Marvella Alaska chip which is used to send the frame from FPGA to system .The main steps in designing are

- The counter is designed such that it should take eight bits of inputs at a time
- Inputs or data bits to fill the respective fields starting from the preamble are given to output as ever count raises
- Counter counts until predefined counts required for frame
- CRC field is designed separately and called as component
- The major steps in designing CRC are
- Taking the message bit of length ‘t’ bits
- Appending ‘r’ bits of zeros
- Where is the length of generator polynomial used in calculating CRC
- Dividing ‘t +r’ number of bits with ‘r’ bits
- The remainder bits are treated as checksum
- Which is added with the message bits and transmitted along with the other fields in the frame
- While coding for CRC the xoring and shifting is done

- The generator polynomial used for CRC coding is 'EDB88320'

Fig 2 shows the system design for generating Ethernet frame and fig 3 and 4 shows the flow diagram for generating Ethernet frame. The fig 5 shows the rtl schematics of Ethernet frame generation.

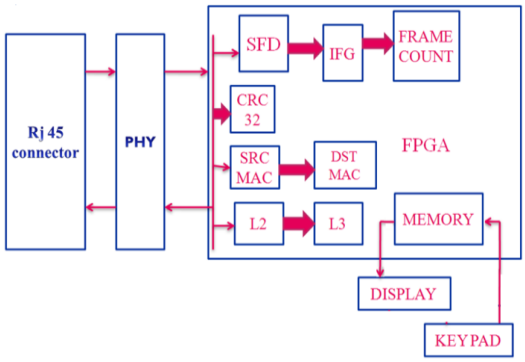

Fig 2: System Design of Ethernet Frame

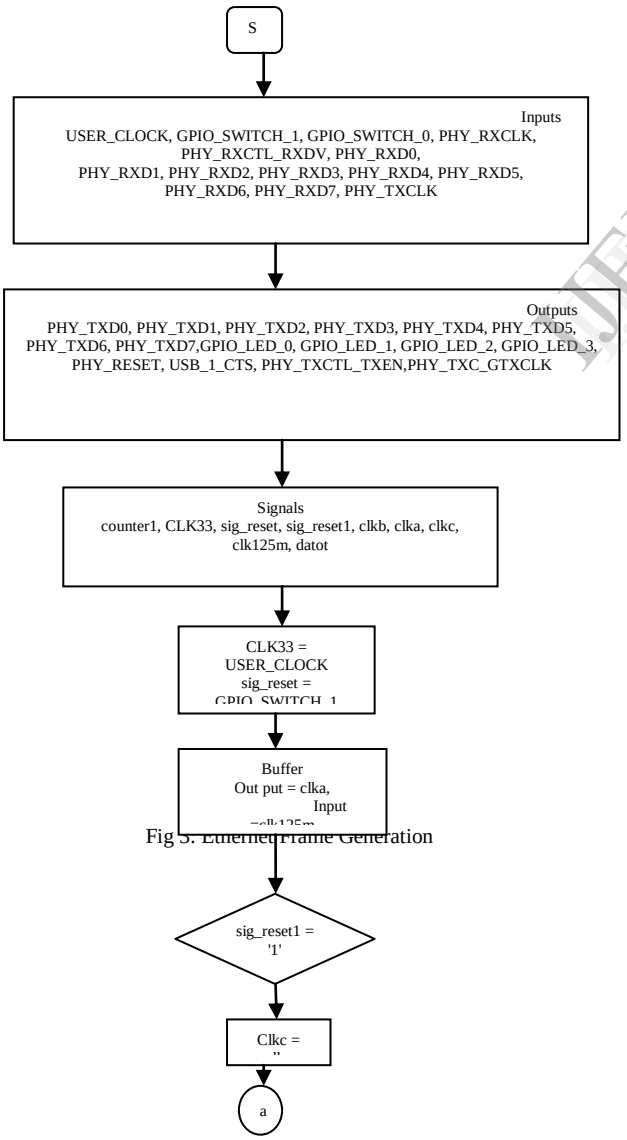

Fig 3: Ethernet Frame Generation

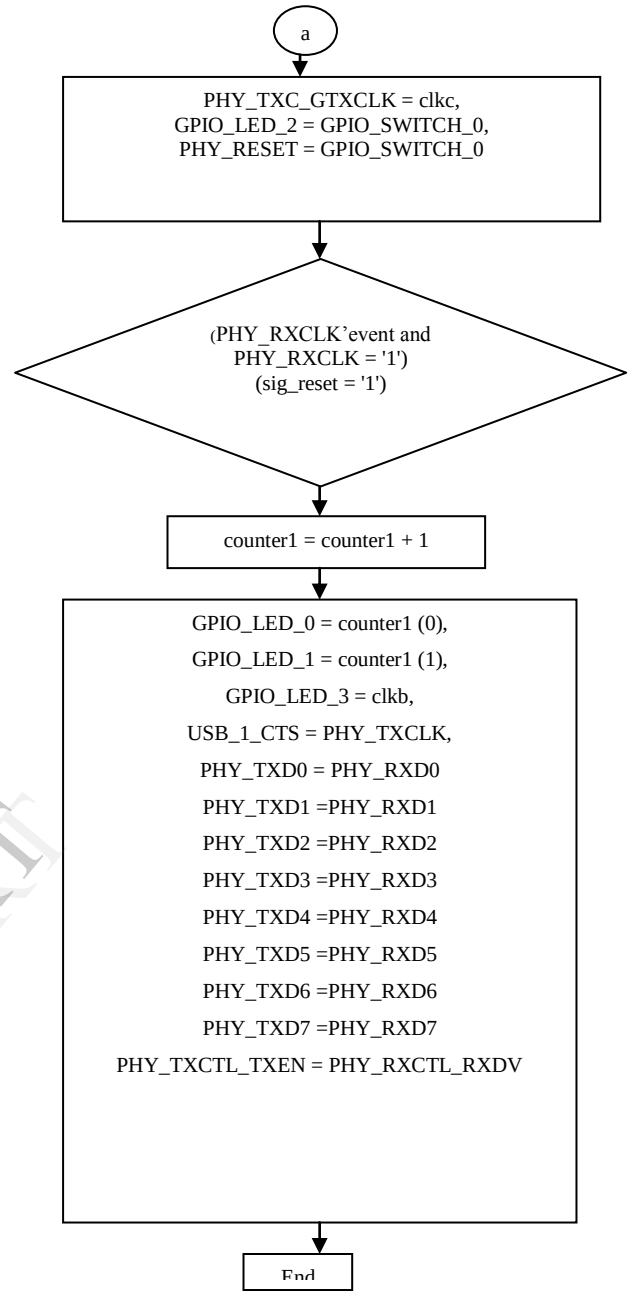

Fig 4: Ethernet Frame Generation

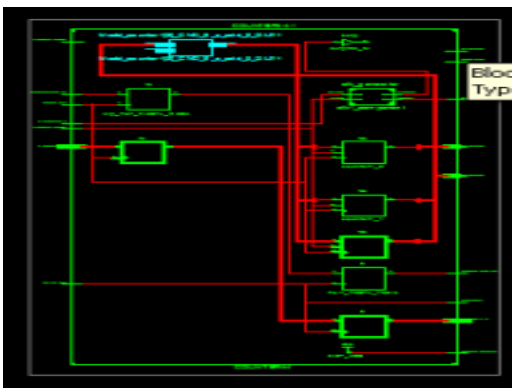

Fig 5: RTL schematic of Ethernet Frame Generation

Fig 6 and 7 shows the simulation result of Ethernet frame and frame captured in Wireshark

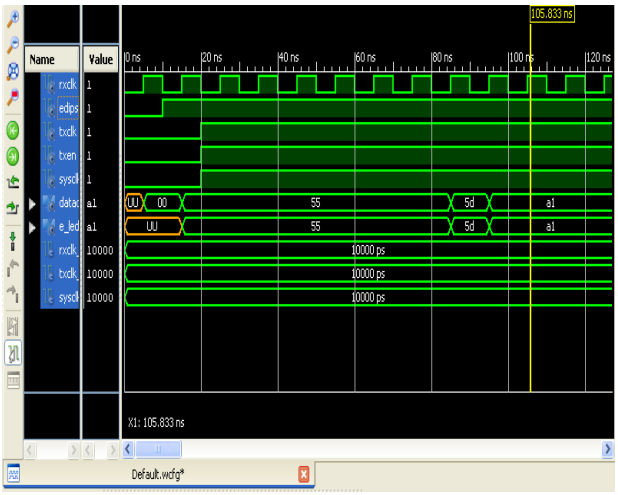

Fig 6: Ethernet frame

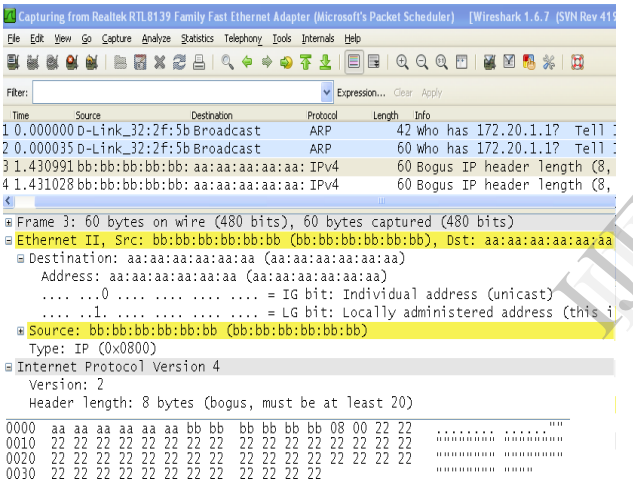

Fig 7: Wireshark Result

III. ADVANTAGES

- with more number of EPPs wire speed can be achieved
- EPP designed can be considered as an application of IP core. This in other words increases the flexibilty of the system.
- since ready IP core is available designing network related systems becomes faster.
- EPPs consume less power and cost is also reduced.
- EPPs are used to verify the systems effectiveness

IV. APPLICATIONS

- Designing Lan switch using Ethernet Packet Processor:
  Ethernet switch connects multiple Ethernet LAN ports. Each port on the switch can be connected to a different LAN port; this topology forms a larger Ethernet network. Ethernet switch is used to interconnect a number of Ethernet local area networks (LANs) to form a large Ethernet network [3].
- High capacity LAN Switch Architecture designing.
- High performance and high speed router design.
- Designing packet analyzers.

V. CONCLUSION

A novel method to design an IP core based packet generator has been presented and a hardware based packets generation, processing packets which can be transmitted at high speed 1/10/20/40/100 Gigabits per second is shown. Transmitting the packets into to pipelined and parallel architecture for further processing to yield high throughput and which can be used routers and switch designs. Therefore using this methodology compact SoC based Ethernet packet processors can be designed which can be used in LAN switch and routers design to increase the speed of the design .since the packets generated are tested in different devices, it can be concluded that, the packets are generated can be used for analyzers

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