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FPGA-based Implementation of Novel Dual-Slope Method for QRS Complex Detection

Yasina S
Dept. of Electronics and Communication Engineering
Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Bangalore, India

S Ravishankar
Dept. of Electronics and Communication Engineering
Amrita School of Engineering, Amrita Vishwa Vidyapeetham, Bangalore, India

***Abstract*— There is a dire need for providing low power, highly compact computing system with scalable hardware solution for remote health monitoring applications. Integrated Circuit Technology in the form of high density FPGAs provide a better solution for implementing Body Sensor Nodes for remote health monitoring. This paper presents a low power hardware implementation for QRS complex detection algorithm using FPGA technology which can be embedded as a sensor in wearable Body Sensor Network. The obtained results were compared with the low power FPGA implementation of existing QRS complex detection algorithms based on Balda and Pan Tompkins QRS detection procedures respectively and found that the proposed implementation resulted in better power dissipation with low hardware complexity. The proposed design is implemented using Xilinx Spartan 3E xc3s500.**

Keywords - ***QRS complex detection, ECG, Xilinx FPGA, BSN.***

I. INTRODUCTION

There is rising trend for personalized healthcare adoption in many countries in which each person is equipped with a wearable or implantable sensor which is wireless, light weight and of small size. These electronic medical devices are used for continuous monitoring of physiological vital signs which provide a prevention oriented healthcare. This interest originates from the need of monitoring a patient continuously for certain disease diagnosis. The wearable sensors temporarily store the vital signs and periodically upload the data to a remote database server where further data analysis can be done. For cardiac patients, these wearable sensors have already become a life-saving intervention. The most attractive feature of these devices is the portability. They are running on battery and the limited battery life of wearable sensors greatly affects the recording time. Therefore, an efficient QRS detection algorithm with less computational complexity is indispensible for low power operation. So there is a great demand for implementing a computationally efficient low power, high speed QRS detector for wearable sensor applications.

Nowadays FPGA chips are becoming attractive choice for designing electronic medical equipments compared to ASIC and Microcontrollers. This is due to its low cost, high degree of parallelism, low time-to-market, on-the-fly reprogrammable and rapid prototyping. The FPGA chips also have fast and efficient testing option which makes it a right choice for implementing and exploring new algorithms. There is an increasing demand of using FPGA chips in various biomedical applications like multichannel physiological signal processing, medical imaging, RF identification, etc.

ECG signal is a representative signal that contains information of each individual's heart. Typical ECG wave consists of P wave, QRS complex and T wave as shown in Figure 1. The main task in ECG signal analysis is the extraction and detection of the QRS complex. For a normal ECG signal the duration of QRS complex is in the range of 0.06-0.1 seconds. Heart rate is determined by detecting QRS complex. Easiest way to detect QRS complex is to find the R peak.

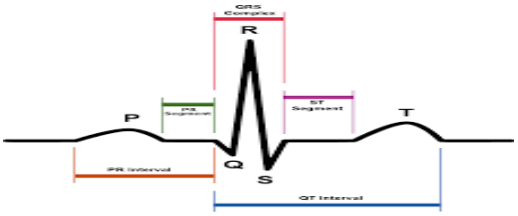

Figure 1 Typical ECG wave

There are several literatures that deal with real time QRS detection of ECG signal [1]-[6]. QRS detection have been regarded as a matured topic until the BSN (Body Sensor Network) is introduced. Wearable sensor is one of the important physiological sensor nodes in BSN. Analysis of ECG signal is important in the diagnosis of Arrhythmia. Basically there are two approaches for analyzing the ECG signal (1) time domain approach (2) frequency domain approach. Qi Haibang et.al, have used Wavelet Transform for position detectionof QRS complex wave which can be used to classify ECG signals for diagnosis [1]. However, constructing mother wavelet is quite challenging resulting in poor recognition rate in this approach. Baseline wandering and background noise are the key issues to be addressed in the detection of QRS complex from the original ECG signal. Chris F. Zhang et.al, employed mathematical morphological methods for removing baseline wandering and background noise from the original ECG signal. They further enhanced the obtained results by using low pass filter. High detection rate of QRS complex is reported in this method. Though mathematical morphological approach appears to be very effective in the detection of QRS complex the selection of proper structural element is difficult task [2].

El Hassan El Mimouni et.al implemented Pan and Tompkins QRS detection algorithm on FPGA. The threshold value for detecting QRS peak is updated for the next peak detection. The design utilizes the parallelism of FPGA in an effective manner [3]. Jovan Kovacevic et.al implemented QRS detection in FPGA technology based on Balda and Pan Tompkins algorithms. The low power implementation of the algorithms are achieved employing hardware optimization methods. Balda algorithm uses derivatives for detecting the slope of QRS complex [4]. The papers [5] and [6] present two different dual slope based methods for QRS detection. Compared to other algorithms the dual slope methods require very low hardware complexity which makes them suitable for wearable ECG sensor applications. Y. Wang et.al used dual slope algorithm for calculating slopes on both sides of a peak in ECG signal. Steepness, shape and height of the signal are used to locate the QRS complex and resulting in very high detection rate [5].
M. Riadh Arefin et.al presents a novel Dual Slope Method for QRS detection analysis which is computationally efficient [6].

This paper presents a low power FPGA implementation of the novel Dual Slope Method used for QRS complex detection[6]. The implementation results of the proposed FPGA architecture when compared with the implementation results of two popularly used QRS detection algorithms (Balda and Pan-Tompkins algorithms) show better results in terms of speed, power dissipation and LEs (Logic Elements).

The remainder of the paper is organized as follows. Section II discusses the Dual-Slope method used for QRS detection and Section III presents the proposed FPGA architecture. In section IV design and synthesis done in Verilog HDL is discussed. Section V presents the evaluation and comparison of the proposed architecture with existing QRS detection algorithms. Conclusion remarks are drawn in section VI.

II. DUAL-SLOPE QRS DETECTION ALGORITHM

In this algorithm, slope of straight line between two samples which are half the QRS width away is calculated[6]. The largest value of slope is found in the peak of the QRS complex. The algorithm focuses on a single sample on both sides of the current sample which is 0.027 sec away. The slopes of straight line on left side and right side of the current sample are calculated. The obtained slopes are multiplied so that higher values which correspond to steep slopes indicate R peaks. The flowchart of the Dual-Slope algorithm is illustrated in Figure 2. The slope equations used in the Dual-Slope algorithm as follows:-

$$S_{left} = \left(\frac{z^{-a} - z^{-(a-k)}}{k}\right) \quad (1)$$

$$S_{right} = \left(\frac{z^{-a} - z^{-(a+k)}}{-k}\right) \quad (2)$$

where a is the nearest integer of 0.027fs where fs is the sampling frequency and z^n is the n^{th} sample in ECG signal.

Steepness measuring variable S_{mult} is evaluated by multiplying S_{left} and S_{right} for each sample according to the following equation:-

$$S_{mult} = S_{left} \times S_{right} \quad (3)$$

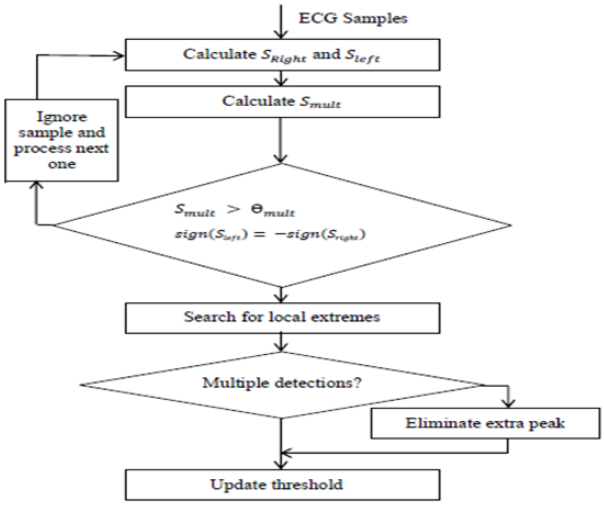

Figure 2 Flowchart of Dual -Slope Algorithm

To ensure that a signal section is R peak, two criteria should be satisfied. The criteria checking has been performed using equations (4) and (5).

$$sgn(S_{left}) = -sgn(S_{right}) \quad (4)$$

$$S_{mult} > \theta_{mult} \quad (5)$$

Where S_{mult} is the steepness measuring variable of the novel Dual –Slope method and θ_{mult} is the preset threshold value.

The equation (4) checks whether the slopes are of opposite signs and equation (5) checks whether the value of S_{mult} is greater than a preset threshold value. If both the conditions are satisfied, local extremes are searched so that multiple detections can be eliminated.

III. HARDWARE IMPLEMENTATION

An FPGA architecture which is area and power efficient is desirable for this novel Dual Slope Algorithm. The FPGA implementation and simulation are done in Xilinx Spartan 3E. The input ECG signal is loaded to MATLAB as text file from MIT-BIH database. The collected signal has 3600 samples taken at 10 sec duration and sampled at a sampling frequency of 360 Hz. The proposed FPGA architecture is as shown in Figure 3.

Three single port ROMs of size 1Kx8 are generated in Xilinx ISE 13.1 IP core generator as shown in Figure 3. The ROM1 stores the input ECG data which is represented by 8 bits. A delay D1 equivalent to 0.027*fs is introduced to the input data and is stored in ROM2 where fs is the sampling frequency. Similarly a delay D2 equivalent to 0.054*fs is introduced to the input signal and is stored in ROM3. The data stored in ROM2 is considered as the present sample whereas data stored in ROM1 and ROM3 are considered as past and future samples respectively.

The proposed architecture consists of the following modules:-

A) Slope Calculation Module: This module plays an important role in the QRS peak detection. The data stored in the ROMs are utilized for slope estimation. Two slopes SL and SR which correspond to left side and right side slopes of the current sample are calculated. The operating speed can be increased by designing two such modules that run parallel. Slope SL is obtained by subtracting the past sample from the present sample using an 8 bit subtractor. Similarly, slope SR is calculated from present and future sample.

B) Multiplier Module: This module multiplies the corresponding slopes of each current sample. This module outputs high value only at peak positions. The multiplier output is fed to the threshold checking module

C) Threshold Module: A comparator block which functions as the threshold module checks whether the multiplier output exceeds the preset threshold value.

D) Polarity Checking Module: This module checks whether the sign of both slopes are opposite. Two input XOR gate will act as the polarity checking module where the most significant bit of both the slopes are fed as inputs. The output from this module is given as control signal to the Decision Making module.

E) Decision Making Module: A demultiplexer unit will function as a decision making module. Whenever the control signal and the threshold module output are high then this module outputs a pulse through the port De1 indicating that an R peak is detected.

IV. DESIGN AND SYNTHESIS IN VERILOG

The novel dual-slope algorithm [6] exhibits better accuracy when simulated in Matlab environment. This paper presents a hardware implementation of the dual-slope algorithm using Verilog HDL. Each module were compiled and simulated in Modelsim and the code has been simulated, synthesized and verified on Xilinx FPGA. In the design to reduce hardware resources serial structures were used. The data stored in each ROM are addressed through counters to estimate the required calculations sample by sample.

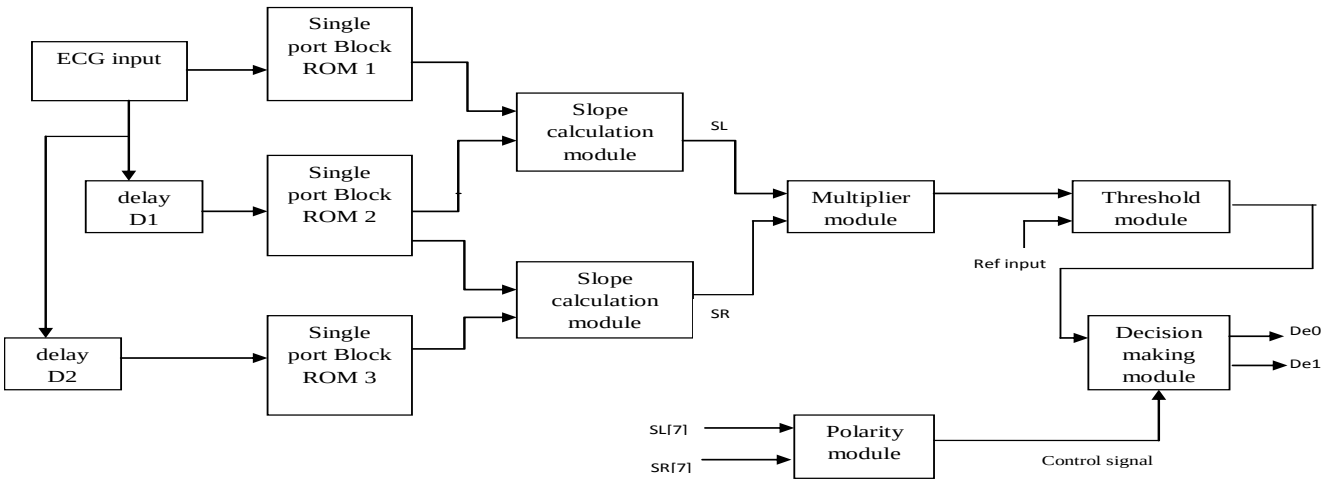

Figure 3 FPGA architecture of Dual Slope Algorithm

The RTL schematic obtained after the successful compilation of each step involved in the Xilinx is shown in Figure 4.The system is designed in such a way that once a peak is detected it shows a pulse. This output when connected to a counter will increment so that the number of peaks detected and thereby the heart rate can be calculated. The simulation result in Xilinx is shown in Figure 5.

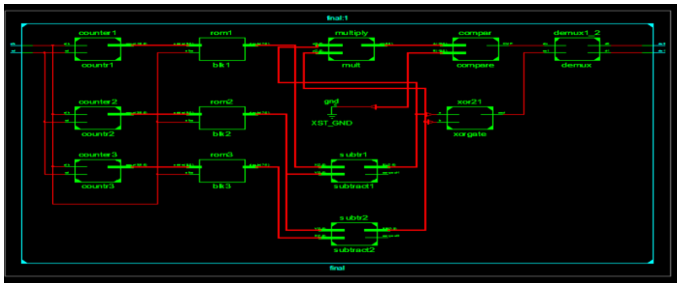

Figure 4 RTL schematic

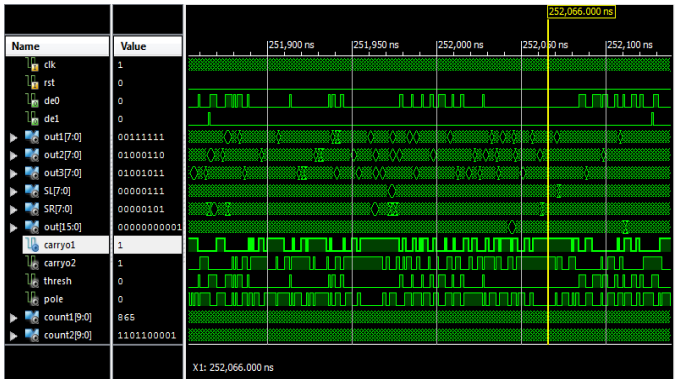

Figure 5 Simulation result of the proposed system

V. EVALUATION

The performance of the proposed architecture with respect to resource utilization and total power dissipation has been investigated. This is done by implementing the system on a reconfigurable platform that is, FPGA which is developed in Xilinx. The memory blocks required for the implementation are generated using Xilinx IP Core Generator. Spartan 3E xc3s500e is the FPGA used and the Table 1 shows the resources estimation. It is clear from the Device Utilization Summary that there is enough space for additional functionalities.

The total power dissipation of the proposed architecture is tested using Xilinx Power Analyzer tool. The total power dissipation at different frequency ranges (50MHz, 25 MHz and 1 MHz) are calculated using this tool. Figure 6 shows the power report of the proposed system at a frequency of 50 MHz is 89 milli Watts.

The total Power dissipation results of the Proposed Dual Slope approach is as illustrated in Figure 7. In the figure, y axis represents the power dissipation and x axis represents the operating frequency. The proposed algorithm exhibits slightly better total power dissipation at different operating frequencies when compared with the optimized implementations in [4]. Table 2 shows the implementation results in terms of LUTs, IOBs and power dissipation.

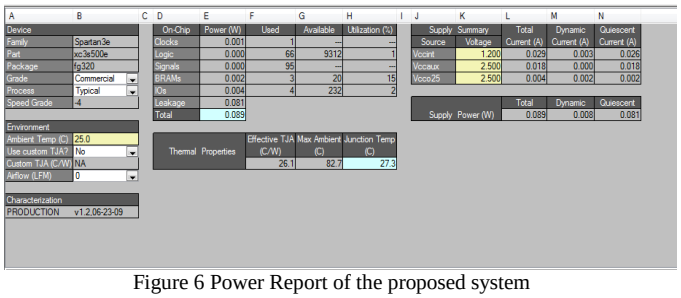

Figure 6 Power Report of the proposed system

Logic Utilization	Used	Available	Utilization (%)
Number of Slices	34	4656	0%
Number of Slice Flip Flops	30	9312	0%
Number of 4 input LUTs	66	9312	0%
Number of bonded IOBs	4	232	1%
Number of BRAMs	3	20	15%
Number of GCLKs	1	24	4%

Table 1 Device Utilization Summary

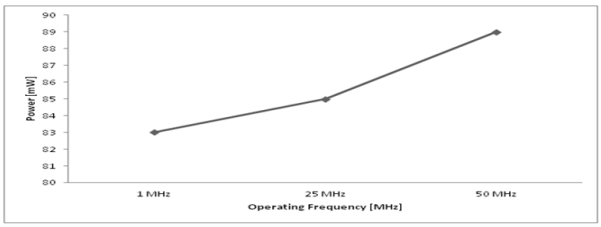

Figure 7 Total power dissipation of Proposed Approach

The resource utilization of the implementation of Pan Tompkins algorithm in literature [3] and [7] done using Spartan 3E xc3s500e FPGA are analysed. The novel implementation of the notorious Pan and Tompkins algorithm occupies only 28% of the used FPGA device [7]. The implementations in literatures [3] and [7] required only 3443 and 1964 4-input LUTs respectively.

The resource utilization of the implementations of the two popularly used QRS detection algorithms – Balda and Pan Tompkins algorithm done in Altera integrated circuit EP4CE115F29C7 FPGA device in literature [4] shows that the implementations require only 419 and 4057 Les respectively. The respective lowest power dissipations were 131.5 milli Watts and 150 milli Watts. The power dissipation of the implementations with respect to different operating frequencies were investigated. The power dissipation testing is done using Power Play analysis tool.

Algorithm	#LEs	#IOBs	Power dissipation at 1 MHz (milli Watts)	Power dissipation at 25 MHz (milli Watts)	Power dissipation at 50 MHz (milli Watts)
Proposed Dual-Slope algorithm implementation	66	4	83	85	89

Table 2 Resource Utilization and Power dissipation of the proposed Architecture

The performance results clearly exhibits that the proposed architecture consumes very low power when implemented in FPGA with less resources which makes it a right candidate for wearable ECG sensor applications.

VI. CONCLUSION

In the area of telemedicine and continuous monitoring of cardiac patients, QRS complex detection plays a key role. So it is important to realize an area and power efficient system that automatically calculates heart rate. This paper presents the design and implementation of such a system on a hardware support. The hardware architecture of a QRS peak detector is proposed and implemented in Spartan 3E. The reason that motivated to end up with this Dual-Slope based QRS peak detection is its low hardware complexity with very low power dissipation.

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