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FPGA based Embedded Central Unit for Active Phased Primary Radar

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***Abstract*--- The Paper presents design, development and realization of a Field Programmable Gate Array (FPGA) based Embedded Central Unit (CU) Controller for Active Phased Primary Radar. The CU Controller performs the in-system Configuration, calibration and Controlling of the T/R modules integrated in the array. The Central Unit of Active phased Array Radar is consists of 5 major Subsystems viz., Low Noise Exciter, Mono-pulse Comparator and BITE / CAL Control Circuit, Receiver Down Converter, CU Controller and Power Supply Unit. There are three Xilinx FPGAs are used to realize the functionality of Central Unit. The Digital Pulse Compression block is also implemented in FPGA along with the Digital Down Converter.**

The I and Q outputs from the CAL channel of digital Down Converter block is interfaced to Front End Processor (FEP) and Array Calibrator Unit located in CU through Low Voltage Differential Signalling (LVDS) interface without any pulse compression. An option is provided to route either the Digital down Converter output or Digital Pulse Compression outputs of any of the quad channel to a Dual Channel DAC for monitoring the I and Q videos from the Receiver Down Conversion under FPGA control.

The CU drives and receives required data to Beam Steering Controller (BSC) for the Active Array. The BSC generates the required beam steering and array configuration signals to control the T/R Modules integrated in the Array Structure.

Suitable Graphical User Interface has been developed in VC++, Each of the Constituent Subsystems of the Active Aperture Array has been Designed and Developed with unique features and has been integrated, tested successfully in the System Level.

***Keywords: Active Phased Array, Transmit/Receive Modules, FPGA, Central Unit and Front End Processor*.**

I. INTRODUCTION

Active Phased Arrays or Active Aperture Arrays, have now become practical propositions for modern day Radar Systems. Active Phased Arrays use individual solid-state Transmit / Receive (T/R) Microwave Module element at each of its radiating element. For the same radiated power, Active Phased Array Systems have been found to be significantly efficient, smaller and lighter than the conventional Passive Array Systems, providing a large power aperture product for long-range surveillance and tracking Radar Systems. The paper describes the Suitable Graphical User Interface has been developed in VC++, Each of the Constituent Subsystems of the Active Aperture Array has been Designed.

The Beam steering controller for the Active Phased array radar is realized through distributed processor architecture in 3 levels of hierarchy similar to RF manifold distribution in the array architecture. A Front-End Processor (FEP) at the top hierarchical level, a Group Level Controller next to the FEP and 320 Nos. of TRM Controllers to control the T/R Modules of TRU forms the Distributed Beam Steering Controller Unit. FEP is realized as a part of the Central Unit applications in the present day new class of Active Phased Array Radar Systems.

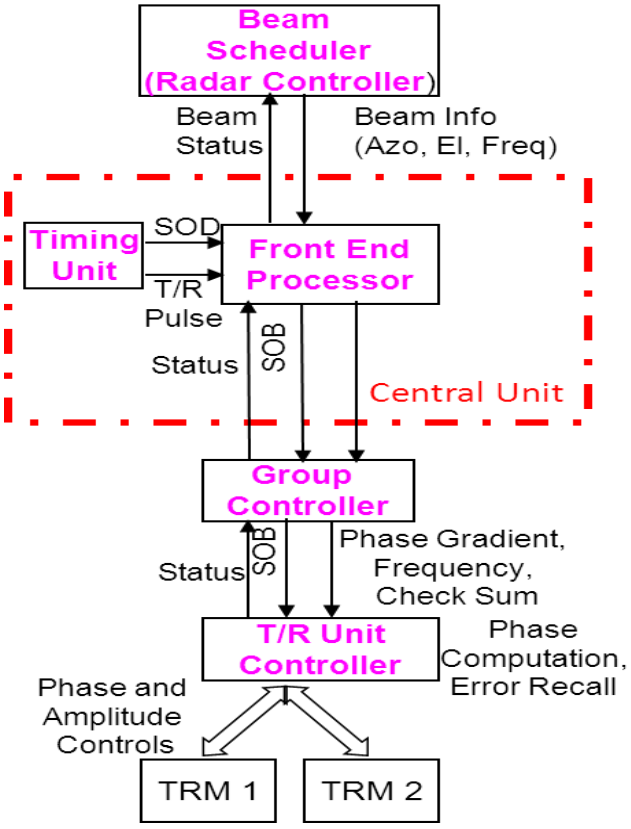


Figure 1.1 Beam switching Data flow via CU

The Radar Controller sends the new Beam Position Data to the FEP and schedules the Beams based on the FIFO (First In First Out) Basis. Since the Beam Switching Time of the BSU is < 200 µSec. as described above, the new Beam Position Data should be available to FEP before 200 µSec. After receiving Beam ready signal from TRU Controllers, the FEP issues Beam Switch Control to the TRU Controllers to load the new Beam Data. It takes a maximum of 1-10 µSec. to

load the Phase Shifters with appropriate Phase Values. The Data Flow Diagram of the Beam Switching is shown in Figure 1.1

II. HARDWARE DEVELOPMENT OF CENTRAL UNIT

The Development of Central Unit consists of two major blocks such as Timing Unit and Front End Processors. It also consists of 1:16 Power divider, 20 channels Analog and Digital Receiver. All these are based on the High end Xilinx FPGAs and Housed as a Central Unit. The Figure 2.1 shows signal flow diagram from T/R Module to the Central Unit Processor.

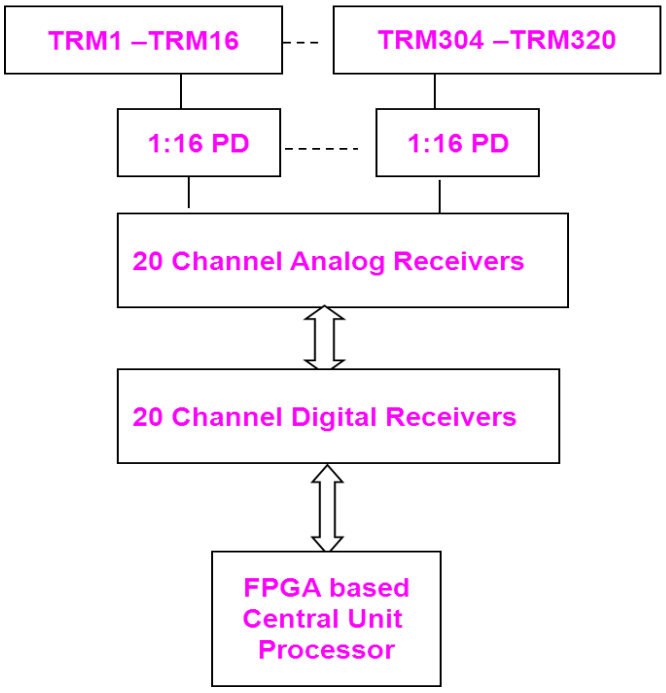
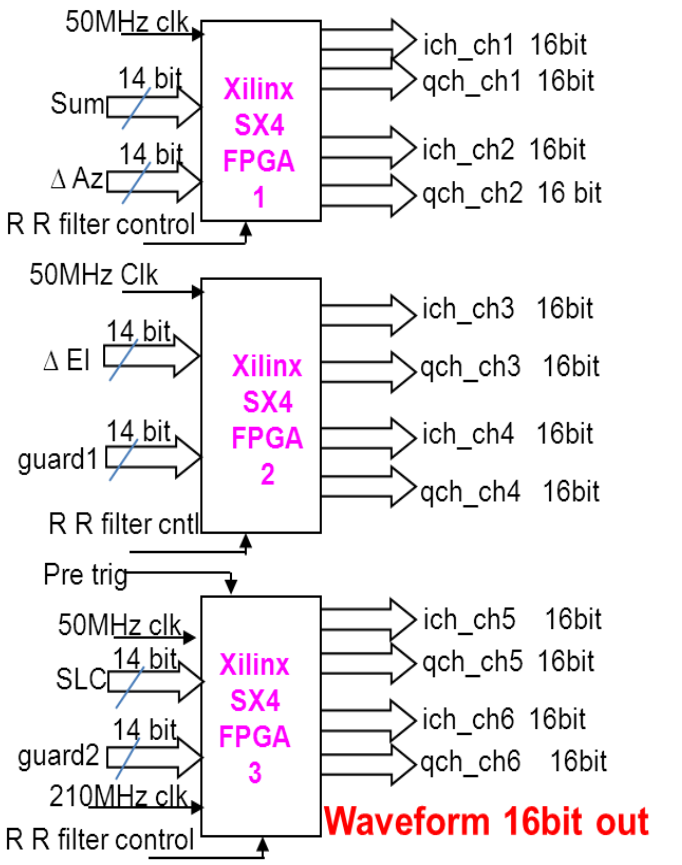


Figure 2.1 Block Diagram of Signal flow

III. DESIGN OF TIMING UNIT

The timing unit is held responsible for generating different timing signals required for the Exciter, Receiver Down Converter Unit and Signal Processing Unit of Active Array Radar. It receives the dwell commands from the Radar Controller through a LAN link and generates the required radar timing signals like T/R Pulse, RF Pulse, Waveform selection, Channel selection control signals, Start of Beam (SOB), Start Of Dwell (SOD), Start of Burst (SOBu), ESM Blanking signal, Norma/Cal Control, Range clock and Pre-trigger etc,. The Timing signals are generated by FPGA using COHO as reference Clock. It also time synchronizes the Central unit and Radar Processor subsystems through a 1PPS (Pulse Per Sec) timing signal of GPS unit received via MSC and with the help of Network Timing Protocol (NTP) messages through LAN interface. The Block Diagram and realized hardware of the Timing Unit is as shown in the Figure 3.1 and Figure 3.2 respectively.



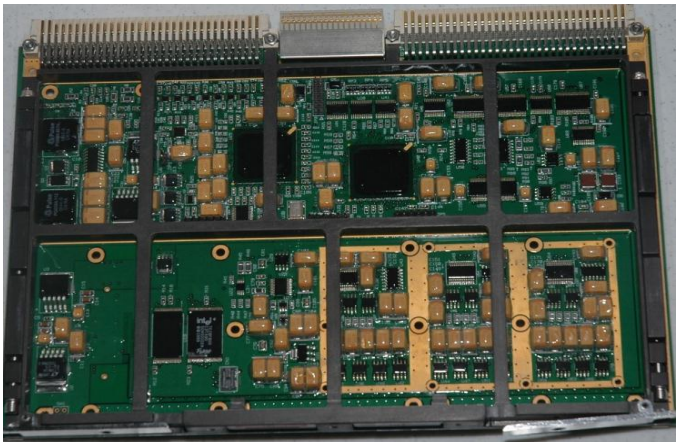


Figure 3.1 Block Diagram of Timing Unit

Figure 3.2 Realized Hardware of Timing Unit

IV. DESIGN FRONT END PROCESSOR

The Front End Processor (FEP) and Array Calibrator Unit of Beam Steering Unit controls and configures the Active Array Antenna Unit, computes the Beam Steering commands and performs the in-system calibration and BITE of the T/R Modules integrated in the array. The FEP is the Central Controller in the Distributed Architecture, which provides interface to the Beam Scheduler of Radar Processor (RP) through a dedicated Ethernet link and Group Unit Level Controllers of the Active Array Antenna Unit through high speed serial link. The Calibration Unit receives the digital I and Q outputs of the CAL Channel and computes the Amplitude and Phase errors.

The detailed functional block diagram and description of this Front End Processor is given in Figure 4.1.

V. CONCLUSION

The FPGA based embedded Central Unit of Active Phased Array Radar provides redundant and efficient interface between the Active Array Antenna Unit (AAAU) along with Radar Processor Controller, performs the following functions

1. Generates the low level Transmit drive signal for AAAU.
2. Receives the 3 Mono pulse RF signals and 3 Guard / Side Lobe Canceller signal from the Active Array
3. Antenna Unit and translates to digital baseband data as an input to signal processor unit of Radar Controller.

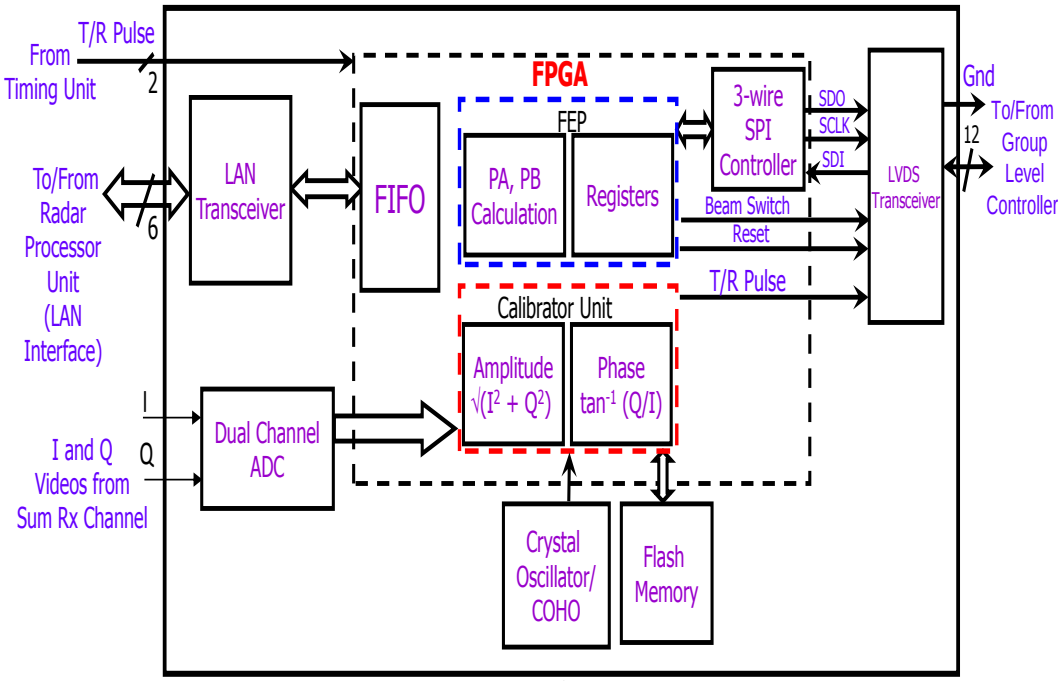


Figure 4.1 Block Diagram of Front End Processor

4. Antenna Unit and translates to digital baseband data as an input to signal processor unit of Radar Controller.
5. Controls BITE/CAL signal to the AAAU
6. Generates necessary beam steering and array configuration control signals to AAAU.
7. Generates the different timing and control signals required for Radar operation based on dwell and configuration commands received from Radar Controller unit.

Suitable GUI has been developed and Constituent Subsystems of the Active Aperture Array has been realized with unique features. The Images of these have shown in the Figure 5.1 and Figure 5.2 respectively. The system integrated, tested successfully in the System Level.

VI. REFERENCES

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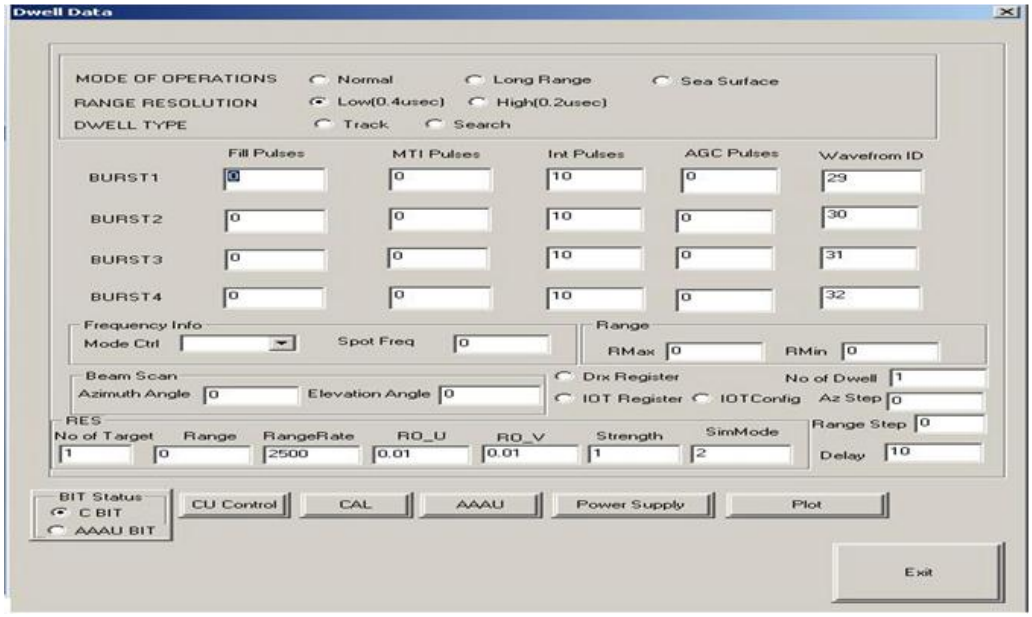

Figure 5.1 GUI for Central Unit and Array Controller

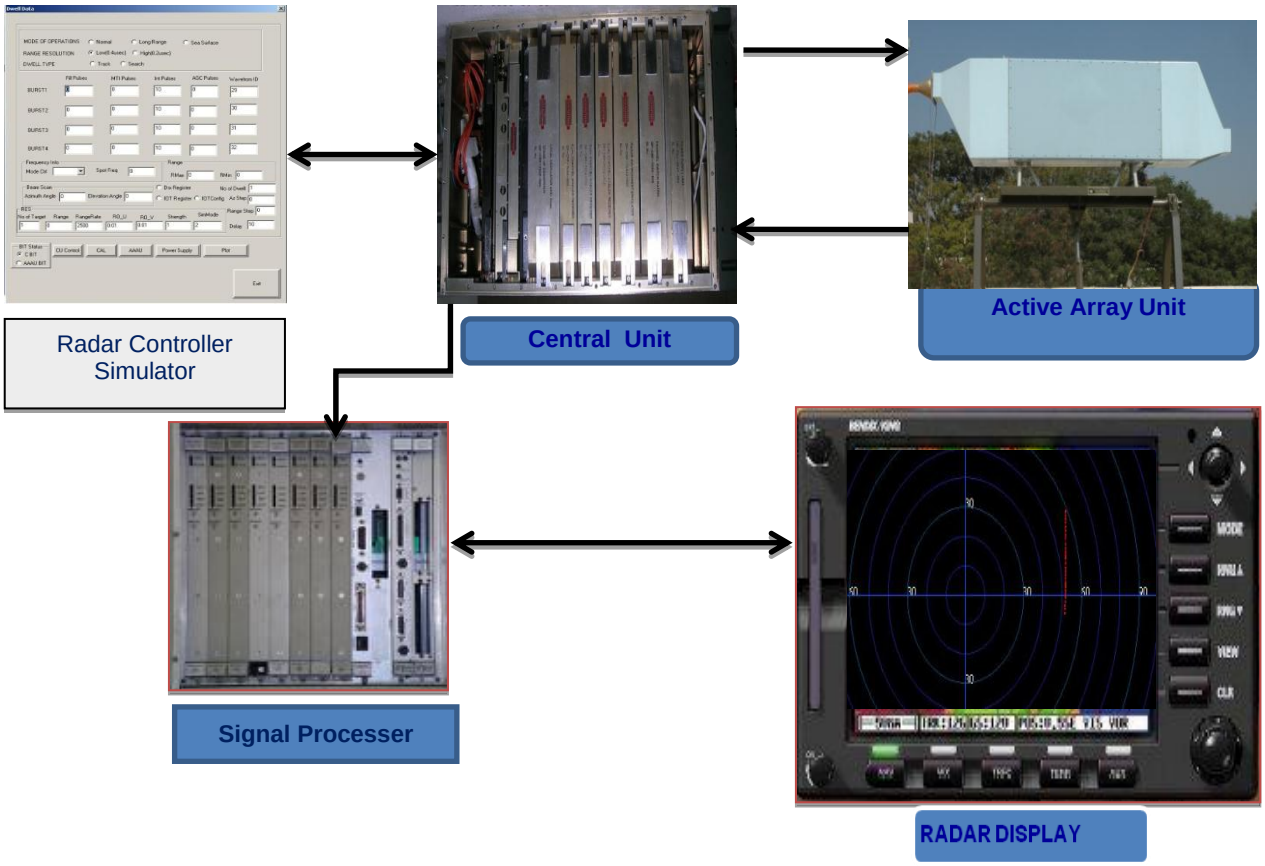

Figure 5.1 Integrated view of Array Unit for Active Phased Array Radar.

BIO DATA OF AUTHOR

Vishakh.L, has been awarded a Proficiency Certificate from Microsoft Research Comp, conducted a technical workshop on advanced Robotics programming in a reputed engineering university[NIT] which is located in our neighbor state, awarded a certificate of achievement from Technophilia (US based org). His one of project named Green Synthesis of rare earth(Re)doped forsterite for WLED's using plant latex _ is approved by the VGST University (Recog. By Govt. of Karnataka) and have been awarded the excellence certificate. Has been awarded an open badge from Mozilla Foundation. His area of interest Android Programming Technology, Robotics with C, Cloud Computing & Virtualization.