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FinFET Based Ultra Low Power SRAM

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***Abstract*— CMOS technology scaling is essential for higher integration density and better performances. Due to scaling the static power consumption increases and becomes a major concern. For SRAM cells, which retain its data only when power supply is provided, the sub-threshold current is a major source of power consumption. Therefore, it is necessary to reduce the sub-threshold current of SRAM cells to use it in low-power applications. FinFETs can be used instead of CMOS as they are good candidates for low supply voltage because of their low power consumption and sub-threshold leakage. These devices provide better control on the channel when compared to CMOS transistors and thus reduces the Short Channel Effect (SCE). Therefore a new technique is proposed to design an ultra-low leakage SRAM cell which improves cell characteristics in read, write and hold modes in FinFET technology.**

Keywords*— *FinFET, sub-threshold leakage, short channel effect, SRAM

I. INTRODUCTION

Static Random Access Memory (SRAM) plays a main role in providing low-power and high-performance for very large scale integration (VLSI) applications. SRAM has high performance with low power consumption during standby mode when compared to other memories. Due to Moore's law, the scaling of CMOS technology well is changed into the nanoscale regime. This shrinking causes many challenges and increases the reliability issues in the design which leads to short channel effects (SCEs) leakage currents and change in process variations.. By using thinner gate oxide SCEs can be decreased but this increase the gate leakage current because of tunneling [2]. This increases the power consumption and thus reliability is reduced. Therefore FinFET transistors are used as a solution as it is a suitable replacement for CMOS. FinFET is a tri-gate transistor has a thin silicon fin that acts as the channel and thus conducts the electrons between the drain and source. In FinFET the short-channel length effect can be controlled by reducing the off-state leakage [1]. FinFET are used to suppress the short channel effects, gate-dielectric leakage currents etc. Therefore a new technique is proposed to design an ultra-low leakage SRAM cell which improves cell characteristics in hold, write and in read mode using FinFET technology.

A conventional SRAM using FinFET is shown in Fig. 1. It contains two inverters which are connected back to back (M1, M2, M3and M4) and two access transistors (M5 and M6) that are connected to the bit lines (Bitline(BL) and bitline bar (BLB). The access transistors provides access to internal nodes and the cross coupled inverters are used to store the two stable states i.e. zero and one. In standby mode, a low voltage is provided to the word line (i.e. WL=0) and the access transistors M6 and M5 are in off condition and therefore the access transistors and the bitlines remains disconnected. In this mode the two inverters provide feedback as long as supply is provided and thus the data continues to remain in the latch condition. In read mode, the bitlines are precharged to a high voltage level (i.e. V_{DD}) and the word line is also enabled (i.e. WL=1) and thus the access transistors are connected to the bitlines and this allows transfer of values in the nodes (QB and Q) to bitlines [5]. If the value at node Q is 1 then the bitline BLB gets discharged through the transistor M2 while the bitline BL remains at logical 1. For the write '0' operation the bitline BL is provided with a 0V while bitline BLB is pulled high to V_{DD} and the word line is enabled [5].

The paper is arranged as follows. Section 2 describes about the related works and section 3 gives the description of proposed work. Section 4 shows the result and its analysis and section 5 concludes the paper.

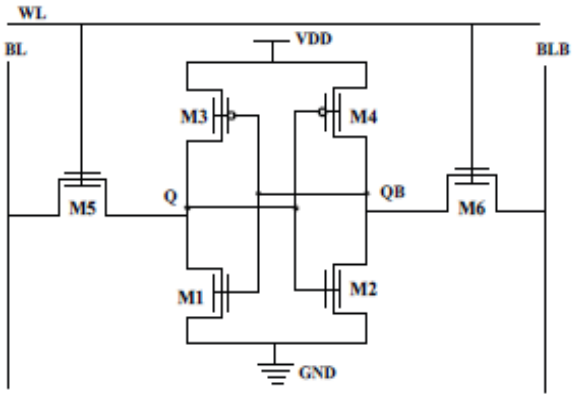

Fig. 1. 6T FinFET SRAM

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II. RELATED WORKS

A. SRAM with Power Gating Technique

The technique is implemented using different states of the WL, BL, and BLB. Other than for read operation, one of the signals is always at low voltage level. This observation is used to design a topology to reduce static and dynamic power. The technique is used to break the leakage path through ground for any low voltage level signals. Word line, bit line and a complementary bit line are set to a high voltage level for the read operation and depending upon the data in the cell the bitlines get discharged or remain charge. During the write operation, word line and one of the bit lines are at high voltage and no need to discharge the bit lines. In hold state, both bit lines are at high voltage level but word line is at a lower voltage level and breaks the path between storage nodes and bit lines [3] - [5]. This technique saves more static power dissipation. The reason for decrement in leakage current during write operation is supply voltage and no path to ground. Either of bit line (BLB or BL) is at low logic during write operation or gives output =’1’, the connected PMOS is off which breaks the path to ground. During read operation all the signal are at logic high and gives output=’0’, PMOS is ON and provide the path to discharge the one of the bit lines.

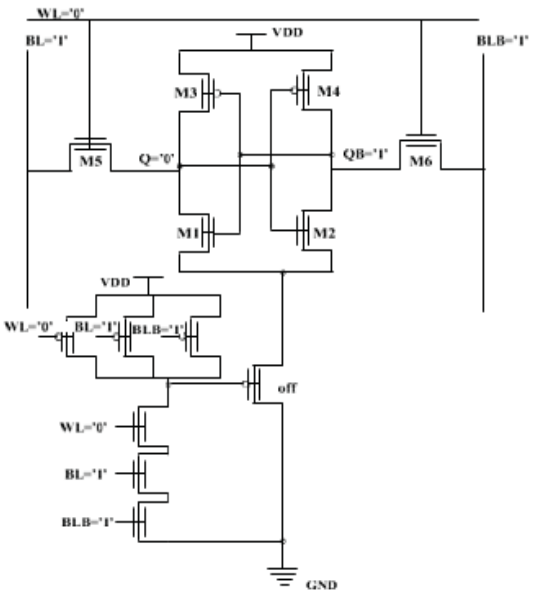

Fig. 2. SRAM with Power Gating Technique

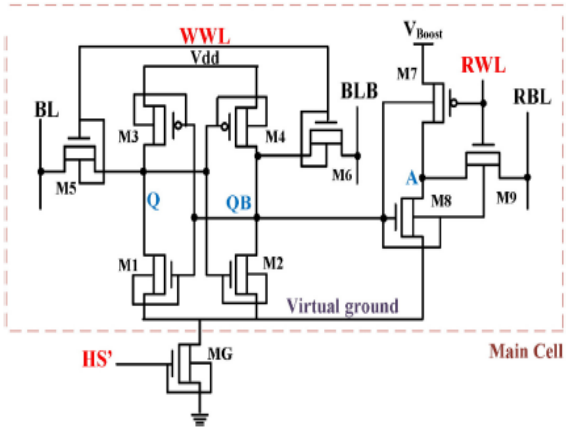

Fig. 3. SRAM with Current Sharing Concept

B. SRAM with Current Sharing Concept

The SRAM cell shown in Fig. 3 consists of ten transistors with six main body transistors, similar to a conventional cell. The additional transistors are used to provide a reduction in the read path leakage and to power-gate the cell when it is in hold mode. The cell stability can be improved by using separate paths for write and read operations. The proposed cell operates in three modes: hold, write and read mode.

The power gate transistor (MG) at the bottom of the main body is used to switch the cell between the active (i.e. read and write modes) and hold modes by adjusting the virtual ground voltage (VG). The HS signal controls the transistor MG. During active mode, V_{DD} is applied to HS inorder to turn ON the transistor MG. Activating WWL or RWL signals enables the write and read operations respectively [12]-[14].

The power gate transistor in the tail of the storage cell and sharing of current and read path are used to reduce the hold power, reshapes the butterfly diagram (higher read SNM stability) and acts as internal feedback to adaptively suppress the changes in the cell. In addition, this decreases the cell voltage drop in write and hold modes, improving write ability and significantly reducing the static power of cell.

III. PROPOSED WORK

The 6T SRAM cell has the advantage of low static power consumption and very less area [5]. But the main problem with the 6T SRAM cell is the stability problem that occurs during the read operation due to the vulnerability of the cell towards noise and thus the cell stability is affected. Therefore proper design of SRAM cell is essential for the proper operation of SRAM. Therefore a new technique as shown in Fig. 4 is proposed to have a SRAM cell with low leakage

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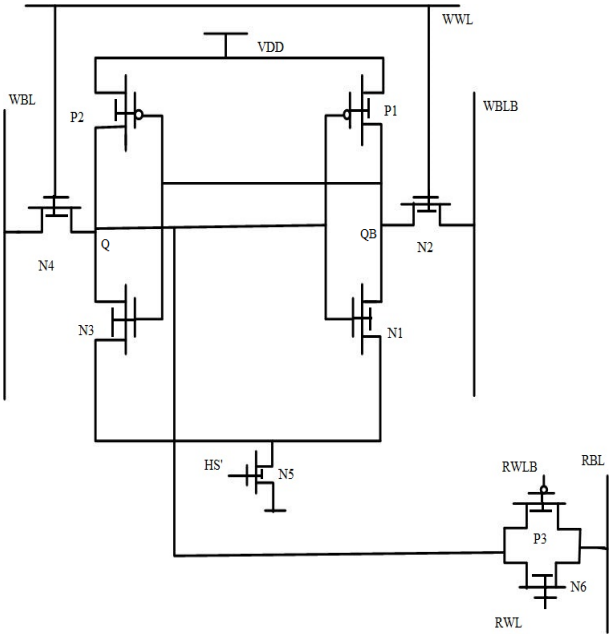

Fig. 4. Proposed Technique

power and improved cell characteristics like write, read and hold noise margin using FinFET technology [8]-[10].

The proposed structure consists of nine transistors with six main body transistors, similar to a conventional 6T cell. The additional three transistors reduce the leakage and the use of separate paths for read and write operations improve the cell. The proposed cell operates in three modes: write, read and hold modes.

During the read operation the write word line (WWL) is disabled and the read word line (RWL) is enabled and the read operation occurs through the read bit line RBL with the help of transistors P3 and N6. The hold and write mode operation of the proposed technique is similar to that of 6T SRAM.

IV. RESULT AND DISCUSSION

The proposed technique is simulated using HSPICE simulator at 22 nm in FinFET technology with 0.9V supply voltage. The parameters that affects performance of a SRAM includes static noise margin (SNM), delay and power. The cell stability of a SRAM is characterized by the SNM value. The cell stability is affected by three types of noise margins : Read noise margin, write noise margin and hold noise margin. The SNM is obtained by drawing the VTC curve of an inverter and mirroring it and finding the maximum possible square between them. The read SNM thus obtained is shown in Fig. 5. The read SNM of proposed technique is obtained as 320mV. Similarly the write and hold SNM of proposed technique is obtained as 600mV and 740mV respectively. The power and delay obtained for the proposed technique is shown in Table1.

TABLE1. POWER AND DELAY OF PROPOSED TECHNIQUE

	Read	Write	Hold
Power (uW)	244.44	30.5	29.59
Delay(ps)	265.9	255.3	266.3

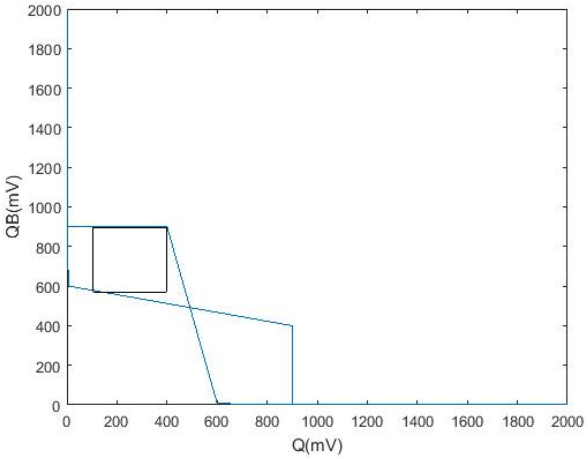

Fig. 5. Butterfly curve for Read SNM

Comparison of power of the proposed technique with 6T SRAM is shown in Table 2 and in Fig. 6 and it is observed that the read power is reduced by 39% and the write and hold power is reduced by 81% & 62% respectively when compared to conventional 6T FinFET SRAM.

TABLE2. COMPARISON OF POWER

	Read Power (uW)	Write Power (uW)	Hold Power (uW)
6T SRAM	399.81	161.03	79.25
Proposed Technique	244.44	30.5	29.59

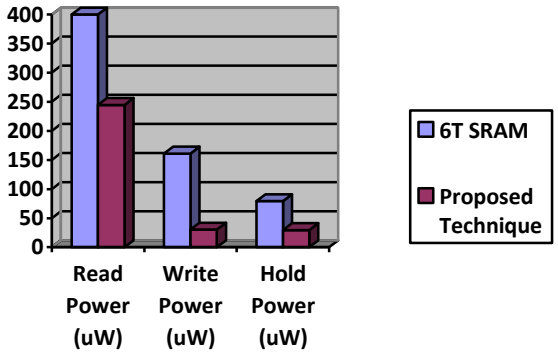

Fig. 6. Comparison of Power

Variation of power with temperature is shown in Table 3 and it is seen that as temperature increases the power also increases.

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TABLE 3. VARIATION OF POWER WITH TEMPERATURE

Temp	Pwrite(uW)	Pread(uW)	Phold(uW)
50ºC	32.96	202.223	31.26
100ºC	34.035	218.480	32.73
150ºC	35.437	235.683	33.40

Variation of power with threshold voltage is shown in Table 4 and it is seen that asthreshold voltage increases the power decreases.

TABLE 4. VARIATION OF POWER WITH THRESHOLD VOLTAGE

V_{TH}	Pread(uW)	Pwrite(uW)	Phold(uW)
0.2	247.51	32.51	60.788
0.3	244.44	30.56	29.59
0.4	238.11	27.32	24.41
0.5	234.589	26.14	23.41

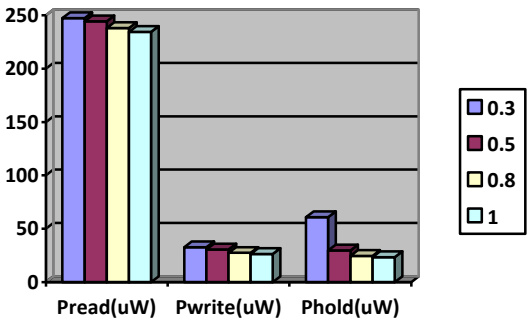

Fig. 7. Variation of Power with Threshold Voltage

V. CONCLUSION

FinFET SRAM cell with reduction technique has been simulated using Hspice software and a reduction in power is obtained. Compared to conventional 6T SRAM cell, the design provides negligible static power dissipation, saves up to 39% of power in read operation and up to 81% of power in write operation and 62% of power in hold operation. The proposed technique reduces the read, write and holds power of the SRAM and also improves the stability of the cell

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