A high speed 64-point FFT processor based on FPGA is implemented using modified Cooley-Tooley algorithm. The architecture is implemented using an 8 point FFT in two stages along with pre-calculated twiddle factors, which also employs complex multiplier and bit-parallel multipliers to achieve an FFT processor that consumes considerable low power and is almost 8 times faster than the existing architectures.

Keywords—64-point FFT processor; FPGA; Cooley-Tooley algorithm

INTRODUCTION

Fast Fourier Transformation is a popular algorithm in modern Digital Signal Processing, Telecommunications, radar and reconnaissance applications etc. Efficient FFT processors are required for applications in orthogonal frequency division multiplexing (OFDM) systems such as IEEE 802.11a/g, WiMAX, Digital video Broadcasting etc. FFT implementations on FPGA have been performed by using Distributed arithmetic, complex multipliers, CORDIC algorithm and Global Pipeline architecture. The above techniques do not support high speed applications.

The most commonly used FFT Processors based on FPGA uses single butterfly architecture. The DFT computations have a time complexity of $N^2$ so the proposed modified COOLEY TUKEY algorithm efficiently reduces the time complexity to $N\log_2 N$, where $N$ is the FFT size.

There are various methods of implementations of FFT which can be mainly classified into memory based and pipeline architecture styles. The memory based architecture is widely known as single processing element (PE) approach which consists of a main PE. This PE acts as single stage 8pt FFT. The Pipelined architecture can overcome the problems of long latency, lower throughput at the cost of marginal hardware overhead by reducing number of stages, compared to 64pt FFT. The pipeline FFT processor uses two design types of which one uses a single path delay feedback (SDF) architecture and the other uses a multiple path delay commutator (MDC). SDF uses less memory space and the computations involved in multiplications are reduced. So the SDF pipeline architecture FFT is employed in this work which is advantageous for implementation of low-power designs. The complex multipliers used in the processor are realized with shift-and-add operations.

In order to improve the power consumption and chip area, an architecture that uses a radix-2 pipeline architecture which consumes low power is proposed for the FFT processor.

Complex multipliers and bit-parallel multipliers are used to store the twiddle factors.

I. MODIFIED COOLEY-TUKEY ALGORITHM

The discrete Fourier transform (DFT) $X_k$ of an N-point discrete-time signal $x_n$ is defined as:

$$X_k = \sum_{n=0}^{N-1} x_n w^{-nk}_N, \quad 0 \leq k \leq N-1,$$

Where the twiddle factor $w^{-nk}_N = e^{j2\pi nk/N}$ is the N-point primitive root of unity. Usually, FFT analyzes an input signal sequence by using Decimation in Frequency (DIF) or a Decimation in time (DIT) Decomposition for the construction of signal flow graph.

If $N$ is the product of two factors with $N=N_1*N_2$, the indices $n$ and $k$ are given as $n=N_1*n_1+n_2$, $0 \leq n_2 \leq N_2-1$ and $0 \leq n_1 \leq N_1-1$, $k=N_1*k_1+k_2$, $0 \leq k_2 \leq N_2-1$ and $0 \leq k_1 \leq N_1-1$.

$w^{-nk}_N$ can be split as

$$w^{-nk}_N = e^{j2\pi nk/N} = e^{j2\pi [n_1N_1+n_2N_2]/N_1N_2}$$

$$= W^{-nk}_N = W^{nk}_N = W^{n_1k_1}_{N_1} W^{n_2k_2}_{N_2} \quad 0 \leq n_1 \leq N_1-1, 0 \leq n_2 \leq N_2-1, 0 \leq k_1 \leq N_1-1, 0 \leq k_2 \leq N_2-1$$

The radix-2 DIF-FFT described here requires less number of complex multipliers.

II. PROPOSED ARCHITECTURE

The PE approach has long latency, low throughput and cannot be parallelized. This problem can be overcome by Parallel pipelined architecture which implements only a single 8-point FFT. A 64-point FFT can be implemented with eight 8-point FFTs. Hence, a single 8-point FFT is first implemented and it is reused wherever required, thus reducing the design complexity. This design style reduces latency at the cost of a marginal hardware overhead. This is because an additional unit is required for the pre-calculated twiddle factors that are stored in the form of LUTs.
A DEMUX operation is used to de-series the input data into 8 parallel channels. A pipeline 8-point FFT is employed to this parallel data. Then the outputs of the pipeline FFT are multiplied with 8 complex coefficients from the LUT’s. Lastly another pipeline 8-point FFT processor is employed to the outputs of the 8 complex multiplies. Later a MUX operation is performed to make a serial output from FPGA.

The pipelined architecture is illustrated in the form of a signal flow graph. The basic operation is a 2-point DFT butterfly having the following form.

\[
X_{m+1}(p) = X_m(p) + X_m(q) \cdot W_N^p \\
X_{m+1}(q) = X_m(p) - X_m(q) \cdot W_N^p
\]  

(2)  

(3) 

The pipeline architecture is illustrated in the form of a signal flow graph. The basic operation is a 2-point DFT butterfly having the following form.

The latency is very less compared to the existing architectures and in turn operates at higher speeds. The gate counts and power consumption are reduced. Especially, the proposed design consumes considerably less active power. The functional simulation is verified using Verilog HDL. The design is also implemented on FPGA chip acknowledging that the architecture is working well.

IV. CONCLUSION

A 64-point FFT processor for low power and high speed applications is designed. A single 8-point FFT is reused for the operations thereby greatly reducing the design and hardware complexity. Also, this design is a time-efficient approach as the parallel pipeline structure gives up to 8 times the operational frequency than the existing designs. This shows that the design is done with minimal hardware cost and reduced power consumption.

REFERENCES


A Sreeharsha received the B.Tech degree in Electronics and communication engineering from JNTUH in 2008. Currently pursuing M.Tech degree from Kaushik college of engineering (JNTUK). She has a teaching experience of 3 years in affiliated engineering colleges of JNTUK as Assistant professor. Her area of interest is in the field of VLSI design.

B Rambabu received the M.Tech degree in VLSI and Embedded System. He is currently working as an Assistant Professor in Kaushik college of engineering (JNTUK) and has a teaching experience of 6 years in JNTUK affiliated colleges. His areas of interest include VLSI and Embedded systems.

SOLOMON JV GOTHAM is the Professor and HOD, Electronics and communication in Kaushik college of engineering, Visakhapatnam. He has a teaching experience of 22 years in various colleges.

A VENKATA KRISHNA is an Assistant Professor in GVP college of Engineering for Women, Visakhapatnam. He has 2 years of Industry experience in VLSI Design and 8 years of teaching experience. His areas of interest include Digital and Analog IC design, Low power VLSI.