Fault Tolerant Reversible Logic D-Flip Flop Based Shift Registers In 32nm CMOS Technology

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Abstract

In Fault tolerant reversible logic gate circuit, the parity of the input vector must equals the parity of the output vector. It renders to find the fault in the circuit. Thus the parity preserving reversible logic will be beneficial to the development of fault tolerant systems in nanotechnology. Fault tolerant reversible logic and reversible logic gates are widely known to be compatible with revolutionary computing paradigms such as optical and quantum computing. This paper presents an efficient realization of DFF, D-LATCH, SHIFT REGISTER using RR- Fault tolerant parity preserving reversible gates. The minimum power, delay, power delay product and hardware complexity to synthesize a fault tolerant reversible Dff, D-Latch, Shift Register circuit has also been given. Finally, this paper presents a novel fault tolerant reversible Dff, D-Latch, Shift Register circuit and demonstrates its superiority with the existing.

1. Introduction

Power dissipation is one of the important parameters in the digital circuit design. Power dissipation plays an important role in VLSI circuit designing. The logic elements are normally irreversible in nature and according to Landauer's principle irreversible logic computation results in energy dissipation due to power loss. This is because of each bit of information dissipates at least KTln2 Joules of energy where K is Boltzamann's constant and T is the absolute temperature at which the operation is performed. By 2020 reversible logic will become a substantial part of energy dissipation, Moore's law states that every 18 months the device package gets doubled and doubling in chip performance. This particular problem of VLSI designing was realized by Feynman and Bennet in 1970s. In 1973 Bennet had shown that energy dissipation problem of VLSI circuits can be overcome by using reversible logic. This is due to the fact that in reversible computation there no loss of information or bits and consequently it does not dissipate any energy for computation. Reversible computation requires circuits with reversible logic and synthesis of such circuits differs significantly from its irreversible counter part because of different factors.[1]A reversible logic gate must have the same number of inputs and outputs, and for each input pattern there must be a unique output pattern. Thus, Reversible logic circuits avoid energy loss by uncomputing the computed information by recycling the energy in the system [3]. In the design of reversible circuits two restrictions should be considered [4]; firstly, Fan-out is not permitted and secondly, Feedback from gate outputs to inputs is not permitted. Due to these restrictions, synthesis of reversible circuits can be carried out from the inputs towards the outputs and vice versa [5]. So, there should be one-to-one mapping between input vector and output vector. In an n-output reversible gate, the input number is equal to the no of output. A logic synthesis technique using a reversible gate should have the features like minimum gate count along with less use of constants and garbage generation. Reduction of these parameters is the main design focus.[6]

Fault tolerance is the property that enables a system to continue operating properly in the event of the failure of some its components. If the system is fault tolerant in nature, then the detection and correction of faults become easier and simple. In communication and many other systems, fault tolerance system can be achieved by having parity. Therefore, parity preserving reversible circuits will be the future design trends for the development of fault tolerant reversible systems in nanotechnology. A gating network will be parity preserving if its individual gate is parity preserving[2]

2. Reversible Logic Gates

A logic gate is reversible if the mapping of inputs to outputs is bijective, that is, every distinct input pattern a distinct output pattern will be produced, and equal no of input and output are avalible. If it has inputs

K*k(and outputs), we call it a reversible gate.[7]Realization of reversible function using gates with smaller width increases the gate count and garbage outputs. Therefore, there must be a tradeoff of using a family of reversible gates. There are many reversible gates in the literature. Among them are 2*2 Feynman Gate (FG) [3], 3*3 Peres Gate (PG) [11], 3*3 Toffoli Gate (TG) [14], 3*3 Fredkin Gate (FRG) [4], 3*3 Khan Gate (NG) [8], 3*3 double Gate (F2G) [10], and 3*3 NFT [5]. Any realization techniques should keep both the number of constants and garbages as low as possible[8]. Garbage Outputs, Constant Inputs, Gate Count, Hardware Complexity, Area Consumption, Path Delay should be made minimum

3. Fault Tolerant Reversible Logic

Fault tolerance enables a system to continue its operations correctly when an error occurs in some parts of it. Parity checking is one of the widely used mechanisms for detecting single level fault in Communication and many other systems. It is believed that if the parity of the input data is maintained throughout the computation, no intermediate checking would be required [11,12]. Therefore, parity preserving reversible circuits will be the future design trends towards the development of fault tolerant reversible systems in nanotechnology. A gating network will be parity preserving if its individual gates are parity preserving [11]. Thus, we need parity preserving reversible logic gates to construct parity preserving reversible circuits [9][10]. Agrawal [13] has shown that fault-detection probability gets maximum when the output information of a circuit is maximized. thus we find that the fault detection would be much easier in the reversible logic, where the information loss is less, than in irreversible ones. Under the multiple fault the full pattern has to be checked in order to find the fault in the circuits for growing number of inputs and the number of gates. This provides additional motivation for studying reversible circuits, namely they may be much easier to test than their irreversible counterparts. A reversible logic circuit design should be optimized for following criteria:

- minimum number of reversible gates
- minimum number of garbage outputs
- minimum number of constant inputs
- The minimum quantum cost of circuit

We first note that of the gates depicted, only the Fredkin gate is parity-preserving. This is readily verified by comparing the input parity A ⊕ B ⊕ C (or A ⊕ B for the Feynman gate) to the output parity P ⊕ Q ⊕ R (or P ⊕ Q). The Feynman gate is quite useful, but, unfortunately, it is inadequate for the synthesis of efficient reversible circuits. Given that synthesis methods with the Toffoli gate, using Fredkin gates to assist in optimizing cost or performance, are quite advanced, we are motivated to look for additional reversible gates that would lead to similarly efficient designs. In this search, the following impossibility result rules out a fundamental role for 2-input, 2-output gates. No 2-input, 2-output reversible gate can be parity preserving. we next look into 3-input, 3-output gates. We have already observed that the Fredkin gate is parity-preserving. Well known fault tolerant gates are [8] New Fault Tolerant Gate, Fredkin gate, Feynman double gate, Islam gate.

4. Previous Work

In [16] Fredkin gate have been constructed the reversible gates. It uses less no of transistors than conventional CMOS based reversible gates. This reduces the area and as well as to operate the circuit with low power consumption and the speed is increased with the reduction in delay The source of energy supplied to the system is only through the input signals only which will greatly favours for the future designs. A fundamental conservative reversible logic gate is the Fredkin gate have been designed using 22,14,10 transistor as shown in fig 1 respectively in [15],[16],[14].

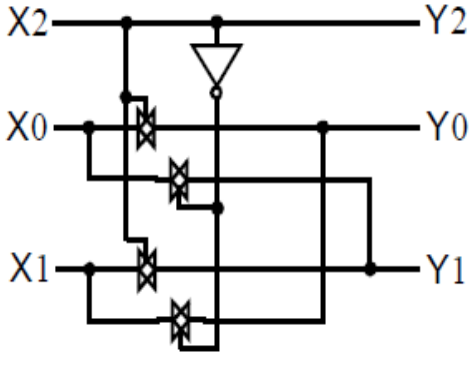

Fig. 1. 10 Transistor FREDKIN gate.

5. Design of New RR Parity Preserving Fault Tolerant Reversible Gate

This paper presents a new 4*4 parity preserving reversible gate, RR Gate (RR), depicted in Figure 2. it has four input and four output wires and it can also be said as parity preserving fault tolerant reversible gate. The gate is one through, which means one of the input variables is also output. The truth table of the RR- gate is shown in Table 1. It can be readily verified from the truth table that the input pattern corresponding to particular output pattern can be uniquely determined.

The proposed reversible RR gate is parity preserving. This is readily verified by comparing the input parity A⊕B⊕C⊕D to the output parity P⊕Q⊕R⊕S.

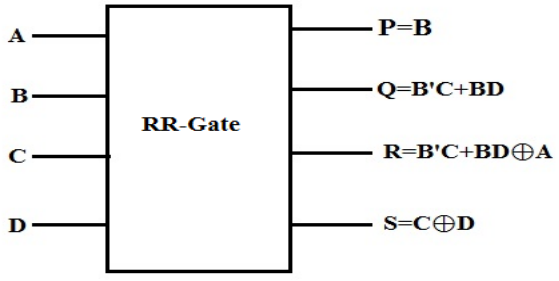

Fig.2 Proposed RR 4*4 Fault Tolerant gate.

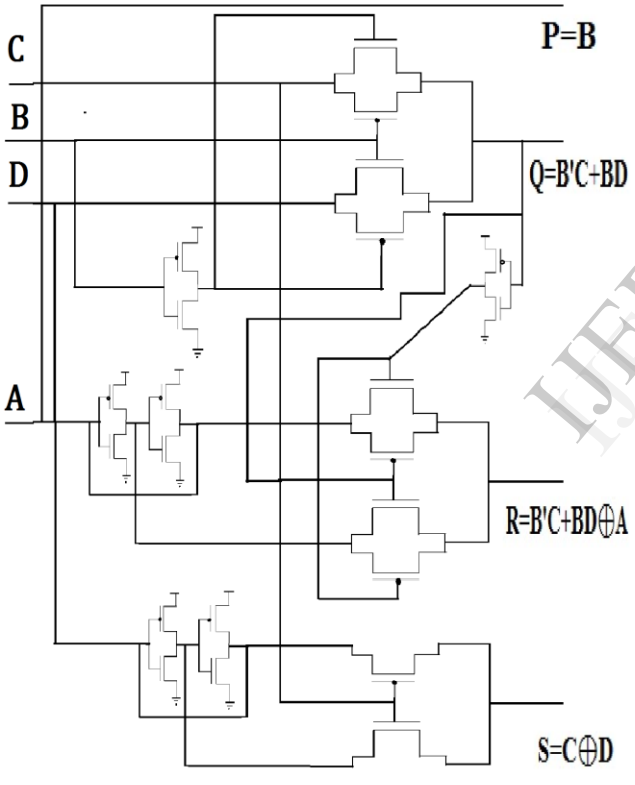

Fig.3 Transistor Design of RR 4*4 Fault Tolerant gate.

There are other two 4*4 reversible gates in the literature, namely TSG and MKG. Though these two gates are reversible but not parity-preserving and therefore do not allow detection of circuit's faults[18].

TABLE1.TRUTH TABLE FOR PROPOSED RR 4*4 FAULT TOLERANT GATE.

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	1	1	1
0	0	1	1	0	1	1	0
0	1	0	0	1	0	0	0
0	1	0	1	1	1	1	1
0	1	1	0	1	0	0	1
0	1	1	1	1	1	1	0
1	0	0	0	0	0	1	0
1	0	0	1	0	0	1	1
1	0	1	0	0	1	0	1
1	0	1	1	0	1	0	0
1	1	0	0	1	0	1	0
1	1	0	1	1	1	0	1
1	1	1	0	1	0	1	1
1	1	1	1	1	1	0	0

6. Synthesis of Fault Tolerant Reversible DFF

Flip-flops and latches are the one bit storage element. such circuits which store the data or the state is defined as the sequential circuit. The D Flipflop make the transaction when it is enabled by the clock. Flipflops are edge triggered. It can be classified into single edge triggered and double edge triggered. This paper we are going to see about single edge triggered.

when the clock is high then the data will be transmitted to the output making the master to work. when clock is low the storage or the feedback condition take at this time slave will be in the active state and the master will be off condition and vice verse. D Flip-flop is defined as the delay flipflop because it can't make any necessary transmission unless until it is enabled by the clock. This paper provides the design of D-latch, D-Flip-flop, using the proposed 4*4 Fault tolerant gate in Fig.4.the advantage of this design is that the designs using this RR fault tolerant gate will preserve parity. Such that the fault or error detection will be simple

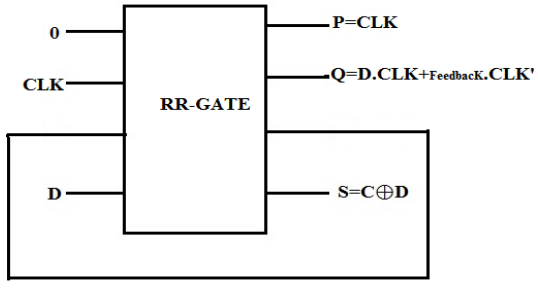

Fig.4.a. D-Latch using RR Gate.

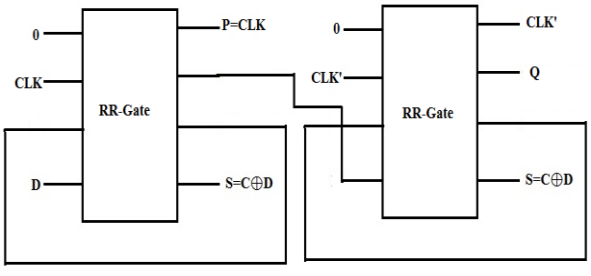

Fig.4 b. D flipflop using RR Gate.

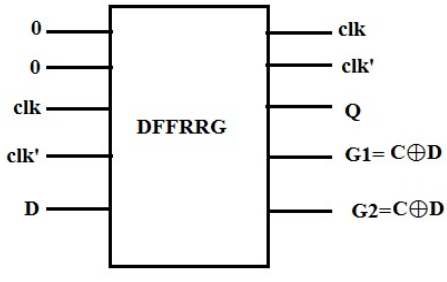

Fig.5. MASTER-SLAVE D-FLIPFLOP USING RR GATE.

7. SHIFT REGISTER

The flip flops are cascaded to form the shift register which shares the same clock, the output of each flip-flop is given as the "data" input to the next flip-flop due to which bit shifting take place. More generally, A shift register may be multidimensional, where data in and data out are in the form of bit array. Several shift register of same length are connected to form this bit array. Shift registers can have both parallel and serial inputs and outputs. These are often configured as serial-in, parallel-out (SIPO) or as parallel-in, serial-out (PISO). There are also types that have both serial and parallel input and types with serial and parallel output. Shift registers are a type of sequential logic circuit, mainly ment for storage of digital data. As the flipflops are cascaded the output of one flipflop is provided as the input for other. All flip-flop is driven by a global clock. The available basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out, and bidirectional shift registers. In few lectures, the basic types of shift registers are studied, such as Serial In - Serial Out, Serial In - Parallel Out, Parallel In – Serial Out, Parallel In - Parallel Out. The storage capacity of a register is the total number of bits (1 or 0) of digital data it can retain. Each stage (flip flop) in a shift register represents one bit of storage capacity. Therefore the number of stages in a register determines its storage capacity.

Serial In - Serial Out Shift Registers: The serial in/serial out shift register shown in Fig.6 accepts data serially – that is, one bit at a time on a single line. It produces the stored information on its output also in serial form. The input data is then applied sequentially to the D input of the first flip-flop on the left .During each clock pulse, one bit is transmitted from left to right. The least significant bit of the data has to be shifted through the register from DFF-RRG0 to DFF-RRG3.In order to get the data out of the register, they must be shifted out serially. This can be done destructively or non-destructively. All flip-flops are reset to zero such state is called destructive state. A basic four-bit shift register can be constructed using four D flip-flops. The operation of the circuit is as follows. depending on the clock the bit shifts from left to right at every clock transaction.

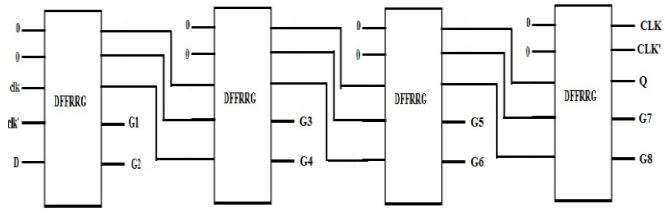

Fig.6. SERIAL IN SERIAL OUT.

Serial In - Parallel Out Shift Registers: Data input are provided serially only at the first flipflop and output is driven parallel .the output of the frist flip-flop is provided as the input for the next flip-flop. The difference is the way in which the data bits are taken out of the register. Once the data are stored, each bit appears on its respective output line, and all bits are available simultaneously. the design of a four-bit serial in - parallel out register is shown in Fig.7.

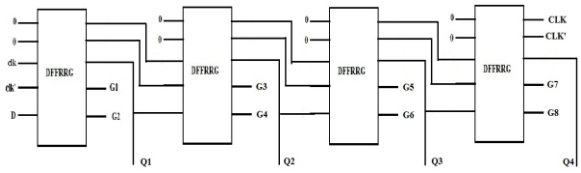

Fig.7. SERIAL IN PARALLEL OUT.

Parallel In Parallel Out: The fig.8 represents the conventional PIPO. The D flip-flop tries to follow the input d but cannot make the required transitions unless it is enabled by the clock. For parallel in - parallel out shift registers the data are provide parallel and the output also taken out parallel. D-flipflop are the main component in the design of the shift register which is the storage register. the application of the shift register is to convert between serial and parallel interfaces in communication system. This is useful as many circuits work on groups of bits in parallel. Serial interfaces can be constructed simply compared to the parallel ones. Shift registers can be used as simple delay circuits.

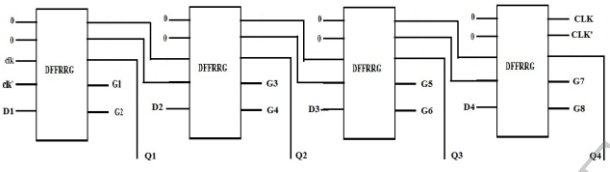

Fig.8. PARALLEL IN PARALLEL OUT.

Parallel In Serial Out: This configuration has the data input on lines D1 through D4 in parallel format. the read and write process take place depending on the selection lines. when sel is low read process which is nothing but the parallel loading takes place. During sel is at high the serial shifting takes place and the registers are clocked. read process is pipo, write process the operation of siso takes place.Here the multiplexer is designed using the Fredkin gate which is also a fault tolerant reversible gate so that the parity may be preserved such that the single level fault occurrences will be less.

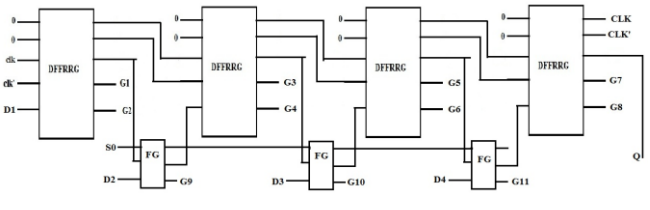

Fig.9.PARALLEL IN SERIAL OUT.

8. Results and Discussion

The proposed parity preserving reversible RR and DFF circuits are more efficient than the existing circuits presented in [10,19,9]. The proposed circuits can be easily compared with the help of the comparative results given in Tables 2,3.

Hardware Complexity: Hardware complexity is found using

a = A two input EX-OR gate calculation
b = A two input AND gate calculation
c = A two input OR gate calculation
d = A NOT calculation

T = Total logical calculation So, for : T = a+b+c+d The hardware complexity for the D-LATCH, D-FLIPFLOP, SISO, SIPO, PIPO, PISO using the Fredkin gate is T=4a+8b+4d, T=8a+16b+8d, T=32a+64b+32d, T=32a+64b+32d, T=32a+64b+32d, T=44a+88b+44d respectively. The hardware complexity for the D-LATCH, D-FLIPFLOP using the proposed RR gate is T= 2a+4b+2c+2d,T=4a+8b+4c+4d,T=16a+32b+16c+16d, T=16a+32b+16c+16d, T=16a+32b+16c+16d, T=28a+56b+16c+28d, respectively, Thus, the proposed parity-preserving reversible circuit requires less logical Calculations. So, Our proposed circuit is better than the circuit presented in in all the terms[10,9,19].

Table2.Comparation of power, delay with existing and proposed gate for 1ghz

Using Fredkin Gate	**Average Power(µW)**	**Delay (ns)**	**Power Delay Product (fJ)**
D-FF	109.9	0.0299	3.28601
SIPO	339.8	0.055227	18.7661346
		1.057504	359.3398
		2.057454	699.122869
		3.057454	1038.9228
SISO	339.8	3.057454	1038.9228
PISO	367.2	3.041331	1116.77674
PIPO	441.5	0.033055	14.5937825
		0.033055	14.5937825
		0.033947	14.9876005
		0.033947	14.9876005

Table3.Comparison of power, delay with existing and proposed gate design1ghz.

Using RR Gate	**Average Power(µw)**	**Delay (ns)**	**Power Delay Product (fJ)**

D-FF	67.59	0.017547	1.1860017
SIPO	325.5	0.053505	17.415877
		1.050157	341.82610
		2.054239	668.65479
		3.011294	980.17619
SISO	325.5	3.011294	980.17619
PISO	200.6	3.0084344	603.49194
PIPO	274.7	0.010122	2.7805134
		0.010122	2.7805134
		0.010691	2.9368177
		0.010691	2.9368177

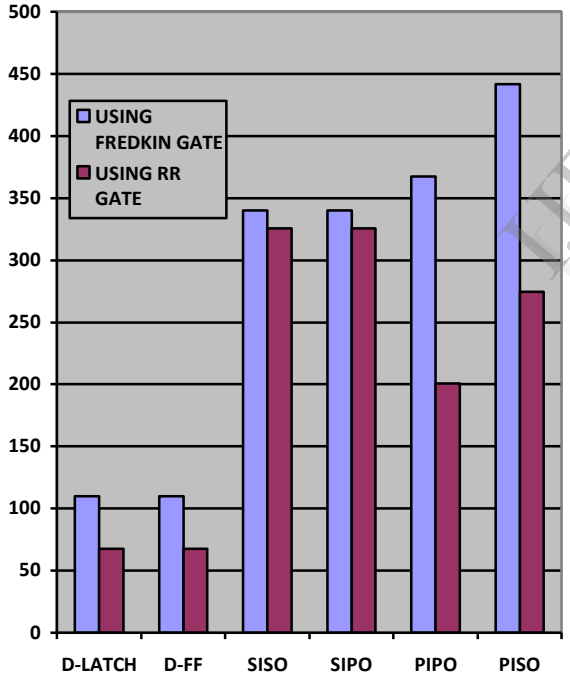

Chart1.power comparison for D-LATCH,DFF,SHIFT REGISTER.

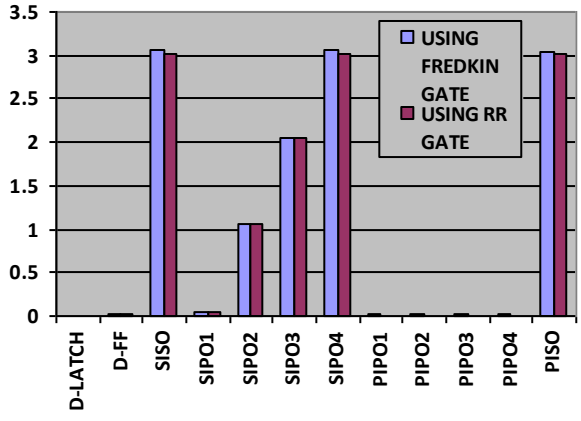

Chart2. Delay comparison for D-LATCH,DFF,SHIFT REGISTER.

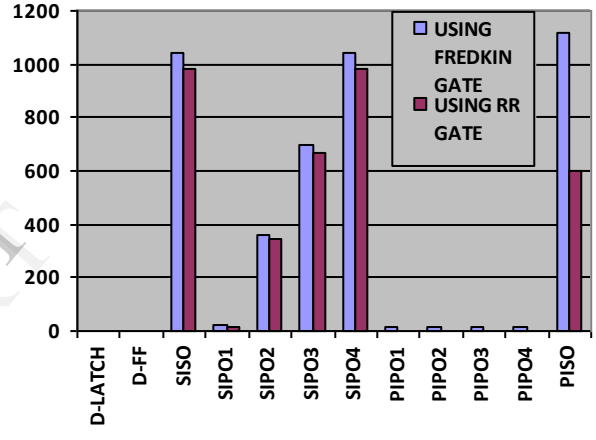

Chart3.Power Delay Product comparison for D-LATCH,DFF,SHIFT REGISTER.

9.Conclusion.

we have given an overview of the k*k parity preserving reversible gates. An efficient Fault tolerant reversible logic RR-gate circuit has been presented. this paper presents a novel realization of fault tolerant reversible D-LATCH, D-FLIPFLOP, SHIFT REGISTER using HSPICE tool in 32nm technology at different frequencies of 1Ghz. The power, delay, power delay product and the hardware complexity is compared with the existing and the proposed design.

10.References

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