Fault Elimination of PWM Modulator to Increase Reliability using Triple Modular Redundancy with Spare Arrangement

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Abstract:- **The proposed work describes the designing of PWM Modulator with increase reliability by triple modular redundancy with spare arrangement. The design, the synthesis, and the implementation of pulse width modulation (PWM) with increase reliability in Xilinx Field Programmable Gate Array (FPGA). The contribution of this proposed work will be the development of PWM Modulator in Xilinx Integrated System Environment (ISE) CAD tools and the VHDL modeling is used in the design process of PWM.**

The project develops high frequency PWM generator with increase reliability architecture on FPGA. The resulting FPGA frequency depends on the target FPGA speed grade and the duty cycle resolution requirements. In most industrial application due to the need of design integration in control systems, FPGA based PWM controller is advantageous over the other controller systems like microprocessor, microcontroller and so on. As geometries shrink and device counts multiply, opportunities abound to do incredible things within the confines of a single chip i.e. FPGA.

Keywords: PWM Modulator, triple modular redundancy with spare arrangement, FPGA, increase reliability.

1. INTRODUCTION

As semiconductors increase in density, growing trend toward moving complete systems from the board level to the chip level such as FPGA . Nowadays, the trends in production of integrated circuits, is to fit the greatest number of devices into small chip area, which leads into high power density. Thus, the manufacturers get into situations where for example, transistor structure is only a few atoms wide. Reduction in size of devices and isolation gaps leads to undesirable phenomena of transient fault. Therefore, increasing of the reliability of devices is necessary, whether with the appropriate hardware or software modification. In Department of mechatronics and electronics, are this new trends implemented in our applications.

Using pulse width modulation (PWM) in telecommunication is not new, there are different approaches for developing pulse width modulation. Many digital circuits can generate PWM signals, but what is interesting is, to generate pulse width modulation using Hardware Description Language (VHDL) and implementing it in FPGA with increase reliability using TMR with spare arrangement[1][2]. FPGA implementation of PWM is selected because FPGA can process information faster, controller architecture can be optimized for space or speed, available in radiation tolerant package, implementation in VHDL allows the targeting of a variety of commercially available device, FPGA allows for implementation of parallel processing.

A field programmable Gate Array (FPGA) is a large Programmable logic device (PLD) that can be used to implement large logic equations as well as arbitrary combinational and sequential logic circuits. Thus, an FPGA can also be used to implement the control- logic design. FPGA can be programmed to the desired application or functionality requirements.

In this project, VHDL modeling is used to generate the PWM signal and XILINX Web Pack ISE Design Software is used for the design of PWM[3][4]. And also XILINX FPGA Spartan 3E family is used for the process, the VHDL language is exhaustively used for PWM generation and the language's capability is explored [5].

2. PWM MODULATOR

The design is based on a simplified block diagram, shown in the fig.1, which consists of generator of triangle signal, the receiver of reference signal and the comparator, which compares the reference signal and signal from triangle wave generator. Pulse width modulation (PWM) is a technique to provide a logic "1" and logic "0" for a controlled period of time. It is a signal source involves the modulation of its duty cycle to control the amount of power sent to a load .Its main use is to allow the control of the power supplied to electrical devices, especially to inertial loads such as motors.

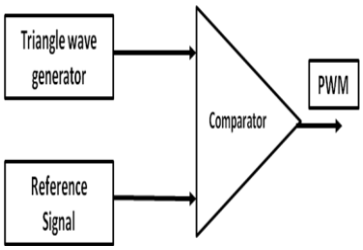

Fig.1. Block scheme of PWM modulator

3. PROPOSED SYSTEM

The proposed project will increase the reliability of the PWM Modulator by using triple modular redundancy and standby spare arrangement.

Methods Used:1) Triple Modular Redundancy Arrangement

2) A Standby Spare Arrangement

3.1 Triple Modular Redundancy

Triple Modular Redundancy (TMR) [2] is a well-known mechanism based on static redundancy. The general principle is to triplicate a system module and introduce the majority voting to obtain a single result of the module, as shown in Figure 1. Such an arrangement allows us to mask failures of a single module.

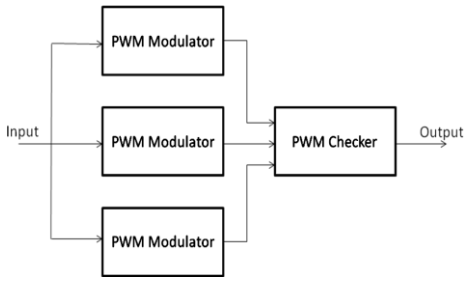

Figure-1 Triple Modular Redundancy

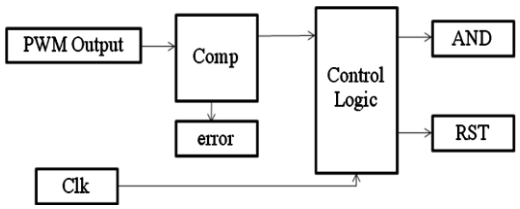

Figure-2 PWM Checker

Block diagram of PWM Checker is shown in fig.2. For each block forming the modulator enters the control block value from the basic comparator PWM modulator. These values are then compared with values from other comparators. The results from comparison of all the blocks evaluate control logic block. In case of difference in data comparison, is fault modulator marked as unreliable. However, the PWM Checker controls the output of fault module for 3 clock pulses and if the difference persists, modulator is permanently removed. In the case of transient fault, modulator is again integrated into service. All error messages are stored in error block for further analysis.

3.2 Standby Spare Arrangement

In Standby Spare Arrangement mechanism, every result produced by an active (main) module is checked by a fault detector. If an error is detected then the result produced by the failed module is ignored and the system switches to accepting the results produced by the spare. The spare can be hot meaning that the main module and spare work in parallel. In this case the switch to spare happens almost instantly. The spare also can be cold, i.e., the spare is in the standby mode and is activated only after the main module fails.

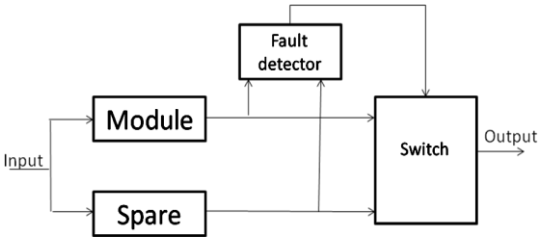

Figure-3 Standby Spare Arrangement

3.3 Triple Modular Redundancy with Spare Arrangement

In this project we propose a hybrid method i.e., Triple Modular Redundancy with spare arrangement shown in fig-4, which is a combination of both the methods, i.e., Triple Modular Redundancy and standby spare arrangement to increase reliability to a greater extent.

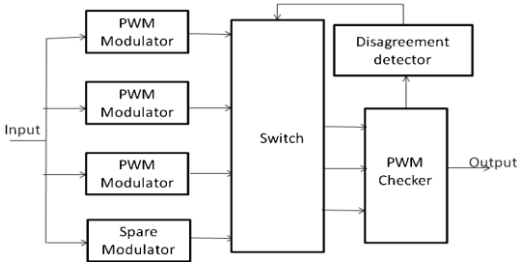

Figure 4 – Block diagram of proposed system

The system works as TMR until a failure of a module occurs. Then the system activates the spare to ”replace” the failed module. The system is using the advantages of both the techniques and combining it to one to increase the reliability.

3.4 Objective of the project:

1. Design of Triple Modular Redundancy with spare Arrangement
2. Synthesis of the proposed design

3. Hardware implementation of proposed system i.e. Triple Modular redundancy with spare Arrangement on FPGA.
4. Comparative study of proposed method with previous methods.

4. CONCLUSION

Improvement of reliability of electronic devices has its own importance. In environments with high frequency electromagnetic radiation, is chance of transient fault more often, which results in unreliable operation of devices, which are not adapted to eliminate transient faults. PWM modulator can reduce the impact of transient failures and thus increase the reliability of the control system.

5. REFERENCES

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