Fast Search Algorithm Based Anti-collision Technique For RFID Passive Tag's

C.Karunakara, M.Tech Student, and Dr.K.Soundara rajan, Professor
Department of Electronics & Communication Engineering
Jawaharlal Nehru Technological University
Anantapur, India

Abstract: -This paper presents a proposed Fast search Algorithm based Anti-collision technique for Radio Frequency Identification passive tag's. The Anti-collision technique architecture consists of two main subsystems; First subsystem and Second subsystem. The First subsystem is to detect any error in the incoming messages. Then the identification bit of the no error packet will be fed to the next subsystem. The Second subsystem is to identify the tag by using the proposed Fast-search Lookup Table. The proposed system is designed using Verilog HDL. The system is simulated using Modelsim and synthesized using Xilinx Synthesis Technology. Finally the Anti-collision technique architecture is resynthesized using from the hardware verification results, it shows that the proposed Anti-collision technique system enables to identify the tags without error at the maximum operating frequency of 261 MHz and the average connection delay is 1.15 ns. Maximum pin delay is 4.177ns.

1. Introduction

The main role of the Data link layer is to convert the unreliable physical link between reader and tag into a reliable link. Therefore, the RFID system employs the *Cyclic Redundancy Check* (CRC) as an error detection scheme. The CRC calculation consists of an iterative process involving Exclusive-ORs and shift register, which is executed much faster in hardware compare in software. Whenever Reader communicates with the multiple tags, an anti -collision technique is required. The technique is to coordinate the communication between the reader and the tags. The common deterministic anti-collision techniques are based on the Tree algorithm such as the Binary Tree.

2. Methodology

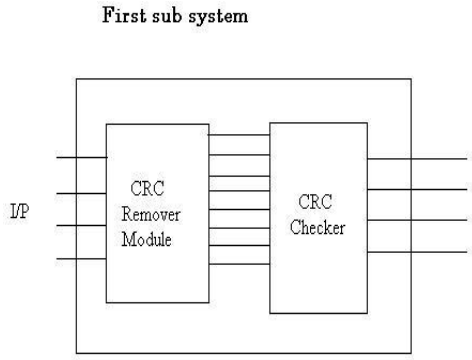
In our proposed Anti-collision technique the frame consists of slots and each slot is divided into four mini-slots. Therefore in each slot, four tags are allowed for contending the mini slots. The Anti-collision technique will identify these four tags using the proposed Lookup table. The uniqueness of this proposed technique is reducing the tag identification time in the Binary Tree. The existing tags are divided into four in each Read cycle to reduce the required iterations and thus faster the tag identification. In Anti-collision technique, bidirectional communications are involved, from the reader to the tag (Downlink) and from the tag to the reader (Uplink). When the reader detects there are tags exist in its interrogation zone, it will power these tags. The selected tags group will move to the Ready state. Next the Reader transmits Reset signals and its frame. After that the frame is transmitted back to the reader, column by column starting with the first column. This compensates the time required for transmitting the packet to the reader. Therefore for every Read cycle, there are always available packets at the reader waiting for identification. At the reader, the incoming packets for each link sequentially enter the Anti-collision technique system. To avoid the four incoming packets from colliding with each other, these packets (IDs) are identified using the Binary Tree based technique with maximum four leaves.

The reader selects these IDs using the proposed Fast-search Lookup table; the four IDs will be identified from the smallest value to the largest one in one Read cycle. Then the tag that has successfully identified will be acknowledged by sending the kill tag.

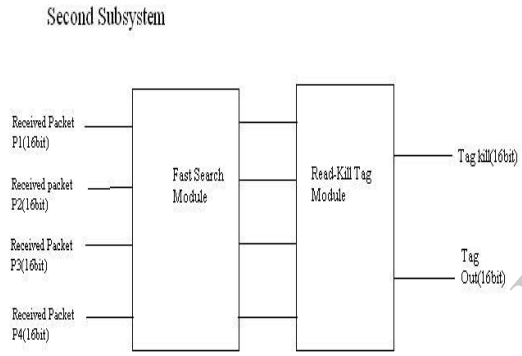
3. Architecture

The Anti-collision technique architecture consists of two subsystem; First subsystem and Second subsystem (Fig. 4). In the First subsystem, the received messages are fed into the CRC-remover module. These received messages will be separated into two; the received packet and the received CRC. These packet and CRC are sent to the CRC-checker module for verification process. The CRC-checker module recalculated the CRC of the received packet. Then, this calculated CRC is compared with the received CRC. If the values are same, means no error, the status-bit is set to its original value i.e. zero. After that, this updated status-bit is appended to its respective packet. Finally, the packet with the updated status-bit is fed to the Status-checker module. The Status-checker module will check any errors in the incoming packets. If there are errors, then reset the slot of the respective packet to zero value. Otherwise, fill the slot of the packet with its respective ID. The status-bit is removed from its packet and only. The tag's ID will be output to the Second subsystem In the Second subsystem, the active tags are divided into a group of four for every Read cycle in order to reduce the number of iterations in the identification process. The Second subsystem reads all the ID bits at once regardless of its length. Using the word-by- word multiplexing performs this. During the identification process, the Fast-search module identifies the four tags IDs simultaneously in one Read cycle which equal to a Tag clock cycle

The module firstly identifies the smallest ID bits until the largest one follows the Binary Tree with a maximum number of four leaves.



(a) First subsystem block diagram



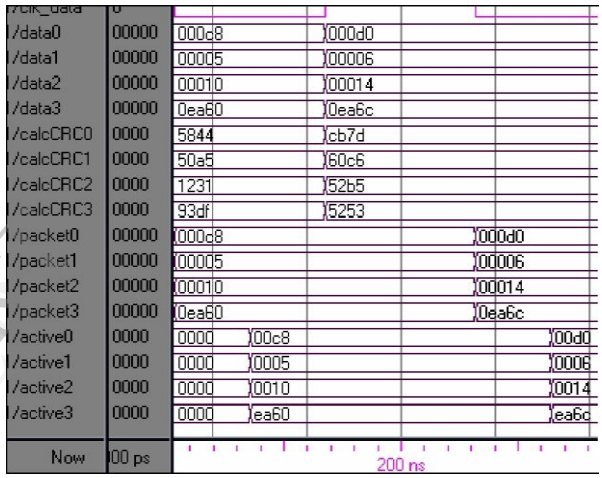
(b) Second subsystem block diagram

4.Simulation results

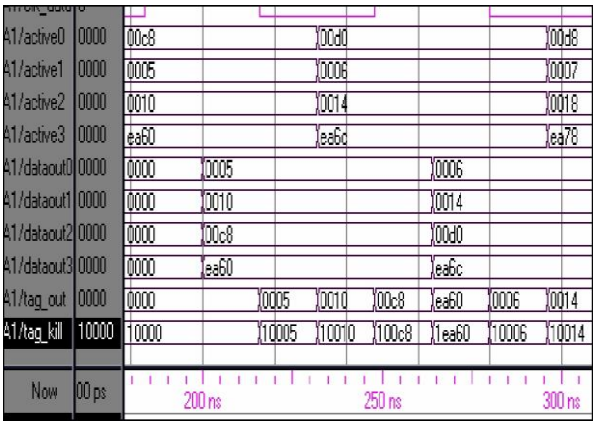
Verilog HDL codes for the Anti-collision technique architecture have been successfully simulated and verified using the ModelSim XE II. The following will discuss the Behavioral simulation waveforms for the selected ports in the Anti-collision technique system as shown in Fig. 2. At the first Read cycle, for the received messages of $000C85844_{16}$, $0000550A5_{16}$, 000101231_{16}, and $0EA6093DF_{16}$, the recalculated CRC of these messages are 5844_{16}, $50A5_{16}$, 1231_{16}, and $93DF_{16}$ respectively.

As a result, the calculated CRCs are equal to the received CRCs, which are represented by the four bit of the least significant bit (LSB) of the messages. Since there are no errors in the received messages, the Status-bit of the packets are set to zero, which are represented by the MSB of the packets; $000C8_{16}$, 00005_{16}, 00010_{16} and $0EA60_{16}$ respectively. Finally, the ID of these packets will be fed simultaneously to the Second subsystem. In the Second subsystem, the Fast-search module will identify the four active tags simultaneously starting from the smallest value to the largest one. For examples, for the four input tag's ID of $00C8_{16}$, 0005_{16}, 0010_{16} and EA60 $_{16}$ will be identified as 0005 $_{16}$, 0010_{16}, $00C8_{16}$ and $EA60_{16}$ respectively.

Then these identified tags will be fed to the Read-kill tag module simultaneously at the negative edge of the Tag clock. Finally, the Read-kill tag Module will output the four identified tags serially, one tag at every cycle of the system clock starting from the smallest tag's ID to the largest one. Moreover, at the same clock cycle, the identified tag will be killed.



(a) First subsystem modules output



(b) Second subsystem modules output

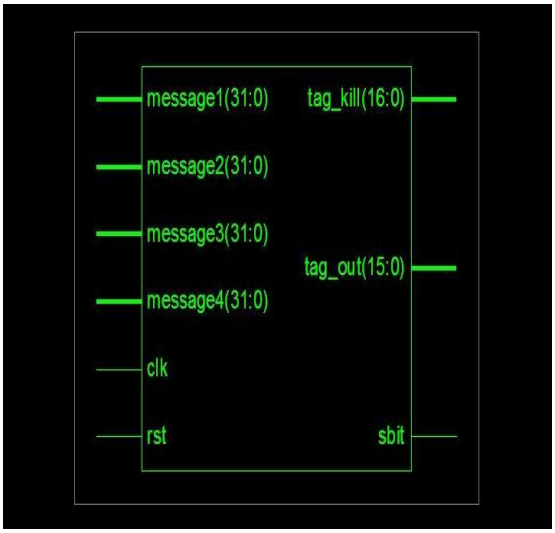


Fig: RTL schematic of top module

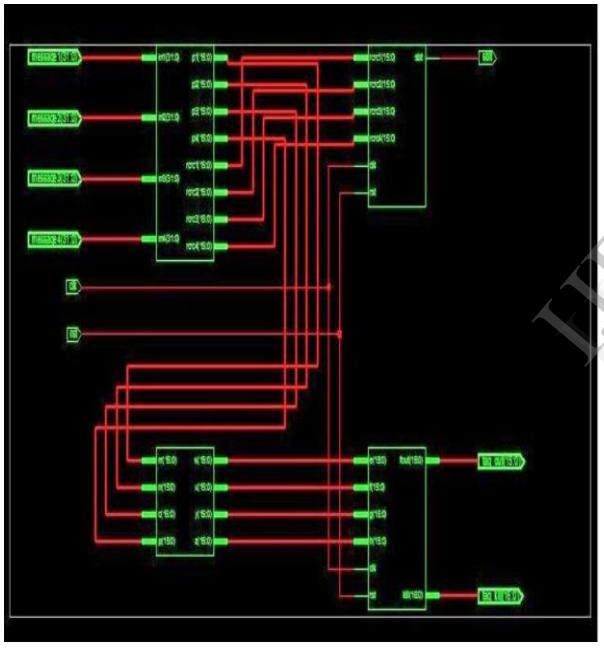


Fig: RTL schematic of sub module

5. Synthesis Results

From the synthesis results, it shows the Anti-collision technique architecture has the maximum operating frequency of 261 MHz .The average connection delay is 1.15 ns and the maximum pin delay is 4.177 ns.

Design Summary of Target device: xc3s500e-4-fg320

Logic Utilization	Used	Available	Utilization
Number of slice	28	9312	0.3%
Number of 4i/p LUTs	339	9312	3%
Number of bonded IOBs	100	232	43%
Total equivalent gate count for design	2597		

Xilinx Synthesis result parameters

Xilinx Parameters
Maximum frequency = 261 MHz
Connection Delay = 1.15ns
Maximum pin Delay =4.177 ns
Total equivalent gate count for design =2597

6. Conclusions

A proposed Anti-collision technique is designed to achieve a reliable and cost effective identification technique of the tag. The Anti-collision technique architecture consists of two main subsystems; first sub system checks error in the incoming packets using the CRC scheme. Second sub system identifies the error free packets using Binary Tree based technique. The architecture has been synthesized using Xilinx Synthesis Technology. The result shows that the architecture has smaller area and number of gates. Therefore minimize the implementation and operating costs

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