

Experimental Validation and Harmonic Analysis of an 8-Switch 31-Level Asymmetric Multilevel Inverter Fed by PV-Battery Link under R load

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Abstract— High switch counts and complex control requirements hinder the widespread adoption of conventional multilevel inverters (MLIs). To overcome these challenges, this paper presents the design, simulation analysis, and low-voltage scaled hardware prototype validation of an 8-switch, 31-level asymmetric MLI tailored for photovoltaic (PV) applications. The architecture uses an asymmetric binary DC supply progression ($1V_{dc}: 2V_{dc}: 4V_{dc}: 8V_{dc}$) split into a four-switch level-generation module and a fundamental-frequency H-bridge polarity module to minimize switching losses. The PV front-end is integrated with a closed-loop PI-regulated boost converter to stabilize voltage ratios under varying irradiance. System performance is rigorously tested under resistive (R) load conditions across simulation and scaled prototype implementations (2 V, 4 V, 8 V, 16 V binary steps). Experimental waveforms captured on a Tektronix DSO confirm stable 31-level stepped output generation, closely matching simulation predictions. Total Harmonic Distortion (THD) remains strictly below the IEEE 519 standard limit of 5.0% across all operating conditions, demonstrating high power quality without needing bulky passive output filters or line transformers.

Keywords— Asymmetric DC link, closed-loop PI regulation, multilevel inverter (MLI), solar PV integration, power quality, reduced switch count (RSC), total harmonic distortion (THD), transformerless inverter.

I. INTRODUCTION

A. Background

Grid-connected and off-grid solar photovoltaic (PV) networks have emerged as essential backbones of contemporary distributed generation power systems, accelerating worldwide decarbonization and sustainable energy transitions. Within these solar architectures, the power electronic conversion stage plays a decisive role in governing overall energy efficiency, operational dependability, and grid power quality by converting variable DC power into regulated AC electricity. Standard two-level voltage source inverters (VSIs) are widely deployed owing to their structural simplicity. However, two-level VSIs present inherent drawbacks, such as excessive total harmonic distortion (THD), pronounced rate-of-voltage-change (dv/dt) stress across semiconductor devices, and a heavy dependence on

bulky LC filtering networks. Multilevel inverters (MLIs) overcome these operational bottlenecks by constructing a multi-stepped staircase output voltage profile. This granular step synthesis suppresses high-frequency harmonic components, lowers electromagnetic interference (EMI), and distributes voltage blocking stress uniformly across power switches [3, 4, 7].

Despite these intrinsic advantages, classic MLI structures—including Neutral-Point-Clamped (NPC), Flying-Capacitor (FC), and Cascaded H-Bridge (CHB) configurations—suffer from severe hardware scaling trade-offs when configured for elevated voltage levels [7, 8]. Generating high-density voltage levels with traditional topologies requires an exponential growth in active power devices, gate driver channels, and isolated DC power links, which substantially inflates system cost, physical footprint, and conduction/switching losses [3, 8]. Asymmetric reduced-switch-count (RSC) topologies mitigate these component penalties by implementing non-uniform DC link voltage ratios, enabling a higher output step count using significantly fewer semiconductor devices [1, 2, 6].

Nevertheless, existing RSC MLI research predominantly focuses on ideal DC sources and purely resistive (R) loading under static simulation conditions [1, 3, 11]. Evaluating converter performance under such simplified assumptions overlooks vital control loop dynamics, dynamic load transients, and reactive power compensation effects present in real-world applications. To bridge this critical gap between theoretical modeling and field application, this study introduces an ultra-compact, transformerless, and filterless 31-level asymmetric MLI system. The proposed architecture pairs a PI-regulated front-end boost converter with an 8-switch binary power stage, comprehensively evaluated across resistive (R), parallel reactive ($R \parallel L$), and series reactive ($R - L$) loads, and experimentally validated through a scaled laboratory test bench (2 V to 16 V binary steps).

B. Literature Review

The development of reduced switch count (RSC) multilevel inverters for solar applications has received significant attention from researchers seeking to lower device count, switching losses, and control overhead while producing near-sinusoidal AC outputs.

Standard symmetric architectures like CHB, NPC, and FC topologies require excessive active switches, gate driver channels, and isolated DC links when designed for high level counts. To solve this component scaling issue, researchers introduced asymmetric DC link configurations, which synthesize exponential output levels from a minimal number of switches. Abdul Hasan et al. [1] proposed a reduced-switch 31-level inverter combined with an Incremental Conductance MPPT front end, achieving a total harmonic distortion (THD) of 3.73%. Saravanan and Sivasubramanian [2] designed a 12-switch 31-level topology that demonstrated reduced switching stress and better operating efficiency in high-power setups.

To simplify the control system, several studies have focused on optimized switching and modulation schemes. Praveena and Sathishkumar [5] implemented a 31-level MLI tuned with SM-CNN algorithms to refine output harmonic performance. Asymmetric structures introduced by Asapu and Rajendran [11] eliminated bulky line-frequency transformers in solar PV systems, though the setup experienced uneven voltage stress across individual switches.

Despite these improvements, most reported RSC topologies are tested exclusively with ideal DC sources or simple resistive loads. Table I compares recent reduced-switch and asymmetric MLI designs published between 2020 and 2025 against the topology presented in this work based on switch count, source requirements, level count, reported THD, and control strategy. While existing topologies achieve good switch-to-level ratios, very few incorporate a regulated solar front-end and evaluate harmonic performance across multiple load types—a combination addressed directly in this study.

TABLE I. Comparison of Recent Reduced Switch / Asymmetric Multilevel Inverter Topologies (2020–2025)

Ref.	Topology	Switches	DC Sources	Levels	Reported THD	Limitation Gaps
Abdul Hasan et al. [1]	Asymmetric PV MLI	12	4	31	3.73%	Requires multiple PV sources with specific voltage ratios; increased control complexity.
Saravanan et al. [2]	Reduced Switch MLI	12	4	31	< 5% (reported)	High switch counts relative to theoretical

Ref.	Topology	Switches	DC Sources	Levels	Reported THD	Limitation Gaps
						minimum; requires complex control strategy
Praveena et al. [5]	Optimization-tuned MLI	16	1	31	Not directly comparable	High computational burden; requires advanced controllers for optimization algorithms.
Asapu & Rajendran [11]	Asymmetric Transformer less	7	2	13	Reported low THD	Capacitor voltage balancing issues; uneven voltage stress distribution across switches.
This work	Asymmetric binary 31-level	8	4 (PI-regulated)	31	1.99% – 4.93% (measured)	Ultra-compact design; verified across resistive (R), series RL, and parallel RL loads.

C. Motivation & Research Gap

The primary engineering challenge in high-level MLIs is component density, which increases thermal losses, control overhead, and overall failure rates. Additionally, existing literature heavily relies on pure resistive (R) load testing, omitting evaluations under series/parallel reactive loads and carrier frequency variations required for real-world industrial and domestic grid applications.

D. Key Contributions

To address these limitations, this paper makes the following key contributions:

- Ultra-Reduced Switch Count:** Synthesizes a 31-level AC output using only eight active power switches and four power diodes driven by a four-source binary asymmetric DC link ($1V_{dc}$: $2V_{dc}$: $4V_{dc}$: $8V_{dc}$).
- Integrated Solar Conditioning:** Incorporates a closed-loop PI-regulated boost converter to stabilize the fluctuating solar PV terminal voltage and maintain exact binary bus ratios under varying irradiance.
- Filterless & Transformerless Design:** Achieves output power quality that complies with IEEE 519 standards ($THD < 5\%$) across purely resistive, series inductive, and parallel inductive loads without needing output LC filters or line transformers.

4. **Decoupled Two-Stage Operation:** Uses a high-frequency level-generation stage alongside a fundamental-frequency polarity-reversal H-bridge, minimizing total switching losses.
5. **Experimental Validation:** hardware validation on a scaled binary prototype (2 V, 4 V, 8 V, 16 V). Prototype setup verified on a physical test bench using Tektronix DSO measurement.

II. PROPOSED SYSTEM & MATHEMATICAL MODELLING

A. Conversion Architecture and System Overview

The overall conversion chain features a three-stage layout designed to convert variable solar energy into a high-quality AC output without needing output filters. As shown in the system block diagram (Fig. 1), the first stage comprises a solar PV array whose DC output varies non-linearly with sunlight intensity and ambient temperature. To maintain a stable DC bus for multilevel synthesis, a closed-loop Proportional-Integral (PI)-regulated DC-DC boost converter conditions this dynamic terminal voltage. The boost stage steps up and stabilizes the PV output to serve as one branch of an asymmetric four-source DC link configured in a binary progression ($1V_{dc}:2V_{dc}:4V_{dc}:8V_{dc}$). The main power stage consists of an eight-switch, four-diode asymmetric multilevel inverter that constructs a 31-level staircase voltage waveform across the load.

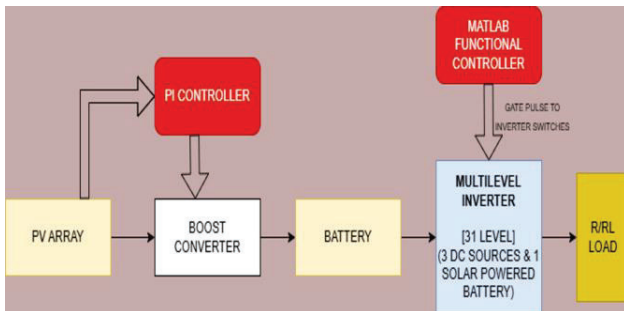


Fig. 1. Overall block diagram of the proposed photovoltaic-fed 31-level asymmetric multilevel inverter system [Simulation]

B. Front-End Boost Converter and Closed-Loop Regulation [Simulation]

Because generating precise voltage steps depends on maintaining fixed DC rails, the boost converter acts as a dynamic buffer against solar power fluctuations. Voltage regulation is performed using a discrete-time closed-loop PI controller. The sensed DC bus voltage V_{actual} is continuously compared against a fixed reference voltage V_{ref} to generate an error signal $e(t)$:

$$e(t) = V_{ref} - V_{actual}$$

The PI controller processes $e(t)$ to generate a corrective control signal, which is compared against a high-frequency (10 kHz) triangular carrier signal. This pulse-width modulation (PWM) process dynamically tunes the duty ratio of the boost converter MOSFET, eliminating steady-state

voltage offset and keeping the binary DC link proportions stable during load changes.

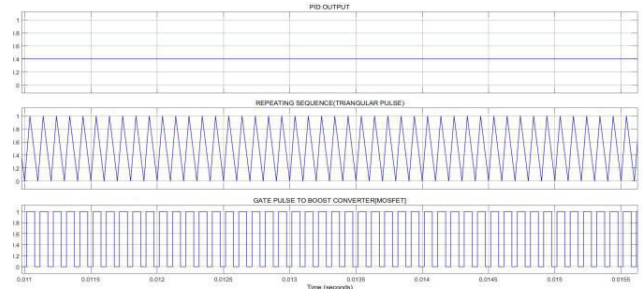


Fig. 2. Boost converter control signal chain: PI controller output, triangular carrier, and resulting gate pulse.

C. Asymmetric 31-Level Synthesis and Dual-Stage Topology

The core inverter separates voltage magnitude generation from polarity switching, using only eight active switches ($S_1 - S_8$) and four power diodes ($D_1 - D_4$). The four binary-weighted sources ($V_{dc}, 2V_{dc}, 4V_{dc}, 8V_{dc}$) allow the circuit to synthesize any integer voltage step from 0 to $15V_{dc}$ through additive combination:

$$V_{out}(t) = \sum_{n=1}^4 S_n(t) \cdot 2^{n-1} V_{dc}$$

where $S_n \in \{0,1\}$ represents the operational state of the n -th level switch. Four power diodes enforce unidirectional current pathing through each source branch, preventing backfeeding without needing extra active blocking devices.

The eight switches are split into two functional groups:

- **Level-Generation Stage ($S_1 - S_4$):** Synthesizes the positive voltage steps by selectively adding or bypassing individual DC supplies. Switch S_1 (connected to V_{dc}) toggles most frequently, while S_4 (connected to $8V_{dc}$) toggles least frequently during each half-cycle.
- **Polarity-Reversal Stage ($S_5 - S_8$):** Arranged as an unfolding H-bridge, this module directs the synthesized DC voltage across the load to produce alternating AC half-cycles. Switches S_5 and S_8 conduct during positive half-cycles ($a(t) \geq 0$), while S_6 and S_7 conduct during negative half-cycles ($a(t) < 0$). Operating strictly at the fundamental line frequency (50 Hz), these polarity switches toggle only twice per full cycle, keeping switching losses low.

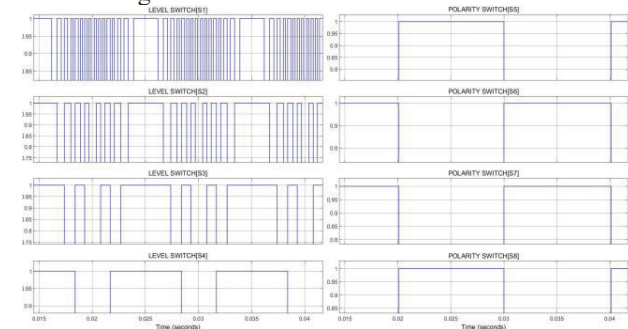


Fig. 3. Simulated gate pulses for level-generation switches S1–S4 and polarity switches S5–S8

D. Nearest-Level Control Algorithm

Gating pulses for both switch groups are generated digitally within a MATLAB Function controller running at a $T_c = 1 \mu s$ sampling interval. The algorithm samples a reference sine wave $a(t) = A_m \sin(\omega t)$ and computes its instantaneous magnitude $c(t) = |a(t)|$. By matching $c(t)$ against 15 predefined threshold levels, the controller selects the correct binary combination and triggers $S_1 - S_4$. Simultaneously, the algebraic sign of $a(t)$ determines the state of polarity switches $S_5 - S_8$. This nearest-level approach avoids the computational burden and synchronization issues of multi-carrier PWM, producing a clean 31-level waveform.

TABLE II. Binary Switching Logic for Level-Generation Stage ($S_1 - S_4$)

Output Voltage Level	Binary Logic (S4 S3S2S1)	Synthesized Voltage
0	0000	0
1	0001	$1V_{dc}$
2	0010	$2V_{dc}$
3	0011	$3V_{dc}$
4	0100	$4V_{dc}$
5	0101	$5V_{dc}$
6	0110	$6V_{dc}$
7	0111	$7V_{dc}$
8	1000	$8V_{dc}$
9	1001	$9V_{dc}$
10	1010	$10V_{dc}$
11	1011	$11V_{dc}$
12	1100	$12V_{dc}$
13	1101	$13V_{dc}$
14	1110	$14V_{dc}$
15	1111	$15V_{dc}$

E. Converter Dynamics & Performance Metrics

In continuous conduction mode (CCM), the voltage gain of the front-end boost converter is given by:

$$\frac{V_o}{V_{pv}} = \frac{1}{1-D}$$

where D represents the steady-state duty cycle. The PI controller control effort in time domain is

$$d(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau$$

Converting to the Laplace domain gives the transfer function $C(s)$:

$$C(s) = \frac{D(s)}{E(s)} = K_p + \frac{K_i}{s}$$

To assess output waveform quality, Total Harmonic Distortion (THD) is evaluated using Fast Fourier Transform (FFT) analysis per IEEE guidelines:

$$THD = \left(\frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \right) \times 100\%$$

where V_1 is the RMS amplitude of the fundamental (50 Hz) component, and V_n is the RMS value of the n -th harmonic. System efficiency η is measured as:

$$\eta = \left(\frac{P_{out}}{P_{in}} \right) \times 100\%$$

III. SIMULATION MODEL

The complete power conditioning circuit—including the solar PV source, PI-regulated boost converter, eight-switch inverter, and load networks—was developed in MATLAB/Simulink using the Simscape Power Systems library. The powergui block solver was set to discrete mode with a fixed sample time of $1 \mu s$ to capture both high-frequency boost switching and subtle multilevel staircase transitions.

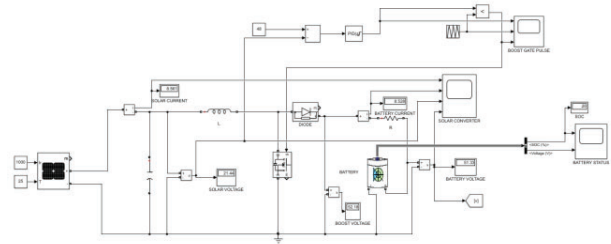


Fig. 4. Simulation diagram of the Solar powered battery

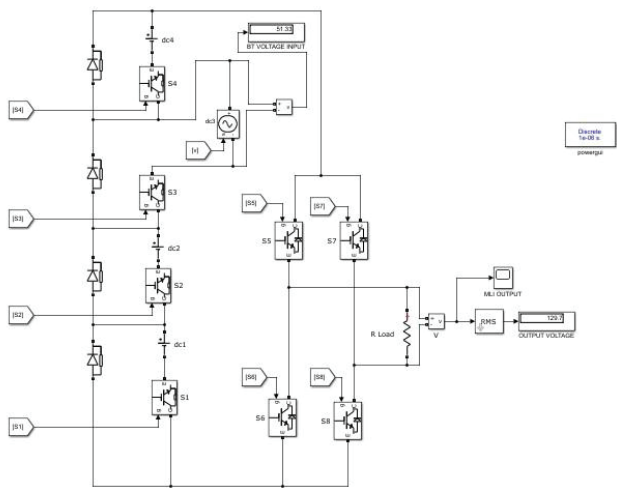


Fig. 5. Simulation diagram of the proposed MLI system.

TABLE III. Simulation System Parameters

Parameter	Value
Simulation software	MATLAB/Simulink (Simscape Power Systems)
Solver type	Discrete, fixed step
Sample time	1×10^{-6} s
Fundamental output frequency	50 Hz
Number of power switches	8 (4 level-generation + 4 polarity)
Number of power diodes	4
DC source ratio	1: 2: 4: 8 (asymmetric, binary)
Boost converter control	Closed-loop PI with triangular-carrier PWM
Output levels	31 (15 positive, 15 negative, 1 zero)
Modulation Strategy	MATLAB Function block, nearest-level logic

IV. SIMULATION RESULTS AND DISCUSSION

A. Steady state, Dynamic Performance and Harmonic analysis

Under simulated steady-state operation, the closed-loop boost converter maintained a stable output from the PI controller when compared against the 10 kHz triangular carrier waveform. This produced a uniform rectangular gate pulse train (as depicted in Fig. 2), confirming that the controller successfully drove the voltage tracking error to zero. By keeping the boost converter output fixed at the reference level required by the 31-level inverter stage, the system avoided pulse jitter and skipped cycles, maintaining continuous conduction mode (CCM).

The gate pulses for the level-generation ($S_1 - S_4$) and polarity-reversal ($S_5 - S_8$) switches verified the proposed switching sequence (Fig. 3). Switch S_1 , connected to the smallest binary source (V_{dc}), exhibited the highest pulse

density because it toggles during nearly every step transition. Conversely, switch S_4 , tied to the largest source ($8V_{dc}$), switched only a few times per half-cycle to handle coarse magnitude steps. The unfolding H-bridge switches ($S_5 - S_8$) changed state only at zero-crossing points every 10 ms (50 Hz fundamental frequency). This fundamental-frequency operation significantly reduces total switching losses across the inverter.

TABLE IV. Tested Load Case Configurations

Case	Load Type	Approx. RMS Voltage	Approx. Peak Voltage
R-1	Resistive (R)	129 V	≈ 180 V
R-2	Resistive (R)	236 V	≈ 330 V
RL-P-1	Parallel Inductive ($R \parallel L$)	130 V	≈ 180 V
RL-P-2	Parallel Inductive ($R \parallel L$)	239 V	≈ 330 V
RL-S-1	Series Inductive ($R - L$)	130 V	≈ 180 V

In Case **R-1** (purely resistive load at 129 V RMS), the output voltage and current waveforms displayed a clear 31-step staircase approximation of a sine wave, reaching peak values of approximately 180 V and 1.8 A (Fig. 6). FFT spectral analysis yielded a fundamental voltage of 183.3 V and a fundamental current of 1.833 A, both recording an identical THD of 1.99% (Fig. 7, 8). Because a resistive load lacks reactive elements, the current waveform mirrors the voltage step profile directly without additional filtering.

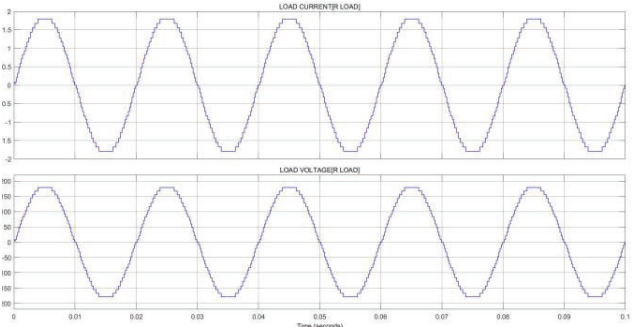


Fig. 6. Load current and voltage, Case R-1 (resistive, 129 V).

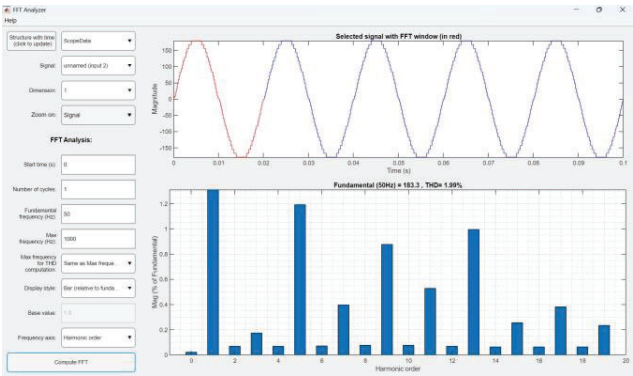


Fig. 7. FFT of load voltage, Case R-1 (Fund. = 183.3 V, THD = 1.99%).

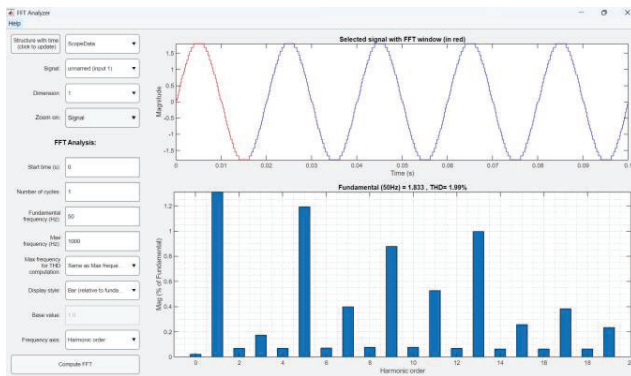


Fig. 8. FFT of load current, Case R-1 (Fund. = 1.833 A, THD = 1.99%).

Increasing the voltage magnitude to Case **R-2** (236 V RMS) yielded scaled peak values of approximately 330 V and 3.3 A (Fig. 9). FFT evaluations indicated fundamental values of 334.1 V and 3.341 A with a THD of 2.01% (Fig. 10,11). The consistency of these THD values (1.99% vs. 2.01%) demonstrates that harmonic performance in the proposed topology is largely independent of the operating voltage level—a critical advantage for solar inverters operating under variable solar irradiance.

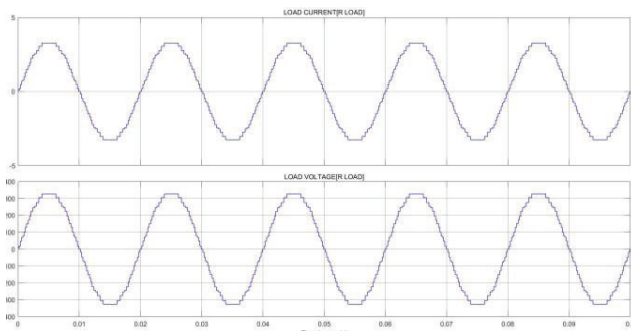


Fig. 9. Load current and voltage, Case R-2 (resistive, 236 V).

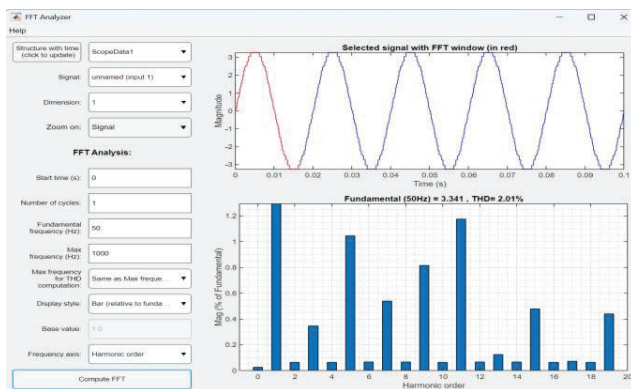


Fig. 10. FFT of load current, Case R-2 (Fund. = 3.341 A, THD = 2.01%).

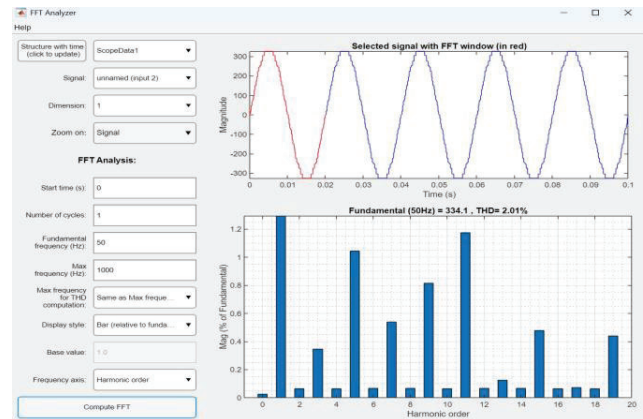


Fig. 11. FFT of load voltage, Case R-2 (Fund. = 334.1 V, THD = 2.01%).

Under parallel inductive loading at 130 V RMS (Case **RL-P-1**), the inductive branch smoothed out the step transitions, giving the current waveform a smoother profile (Fig. 12). FFT analysis showed a current THD of 3.50% and a voltage THD of 3.51% (Fig. 13, 14). This moderate increase in distortion compared to the resistive case stems from reactive current flow and transient interactions near zero-crossings.

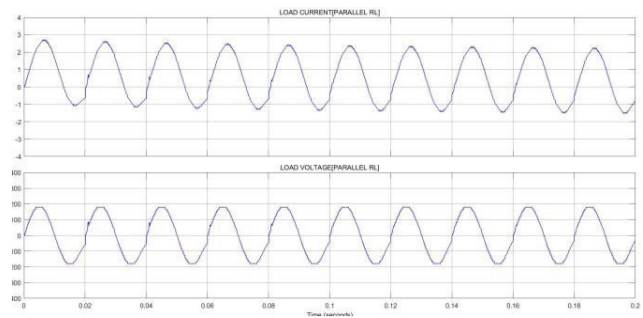


Fig. 12. Load current and voltage, Case RL-P-1 (parallel RL, 130 V).

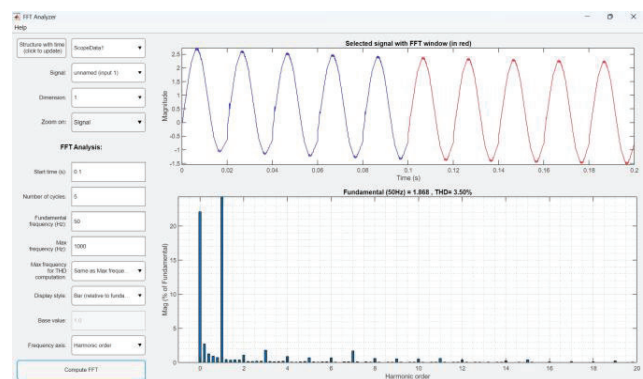


Fig. 13. FFT of load current, Case RL-P-1 (Fund. = 1.868 A, THD = 3.50%).

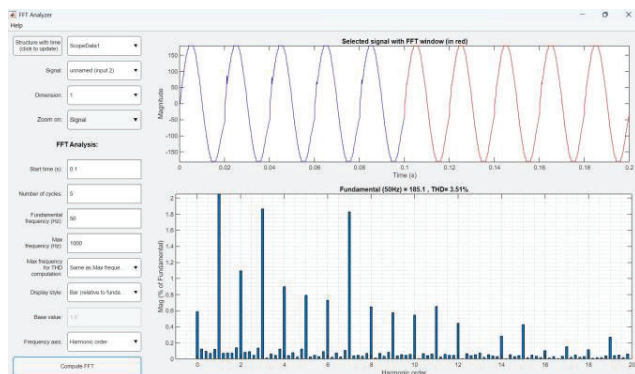


Fig. 14. FFT of load voltage, Case RL-P-1 (Fund. = 185.1 V, THD = 3.51%).

At the higher operating voltage under parallel RL loading (Case **RL-P-2**, 239 V RMS), dynamic coupling between the reactive load and the boost converter became more pronounced (Fig. 15). FFT analysis revealed a fundamental current of 3.423 A ($THD = 4.86\%$) and a fundamental voltage of 338.9 V ($THD = 4.93\%$) (Fig. 16, 17). Although this represented the highest harmonic distortion observed in the study, it remains comfortably within the 5.0% limit specified by IEEE 519 standards.

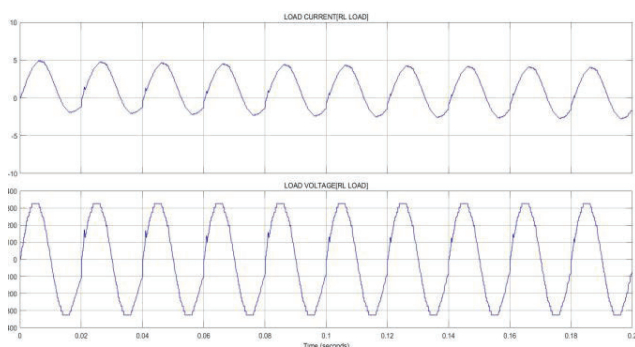


Fig. 15. Load current and voltage, Case RL-P-2 (parallel RL, 239 V).

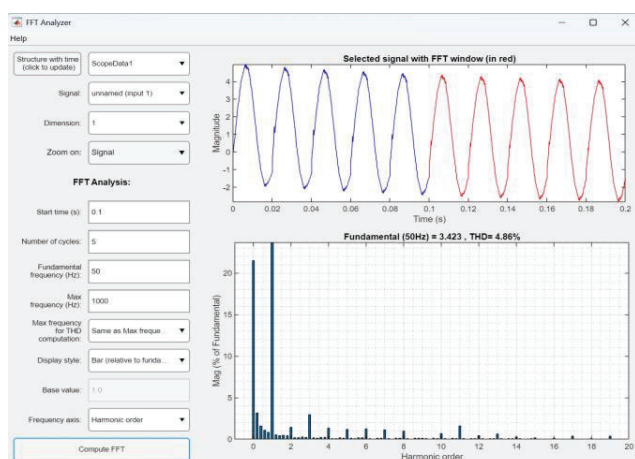


Fig. 16. FFT of load current, Case RL-P-2 (Fund. = 3.423 A, THD = 4.86%).

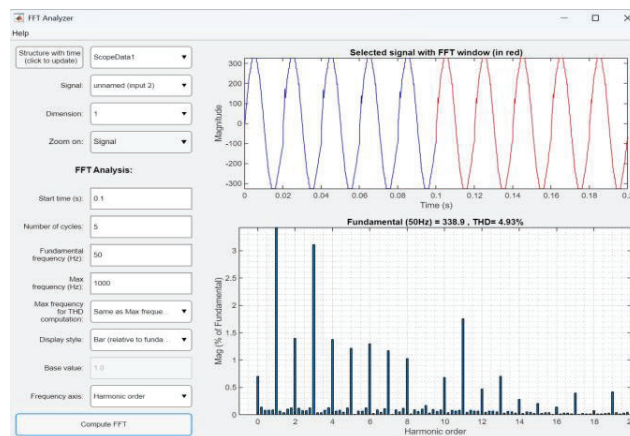


Fig. 17. FFT of load voltage, Case RL-P-2 (Fund. = 338.9 V, THD = 4.93%).

For series inductive loading (Case **RL-S-1** at 130 V RMS), the series inductor acted as an inherent low-pass filter on the voltage steps, yielding a current THD of 4.34% and a reduced voltage THD of 3.16% (Fig. 18–20). Compared to the parallel setup, the series configuration imposes less voltage distortion because it lacks a direct parallel reactive path across the output terminals.

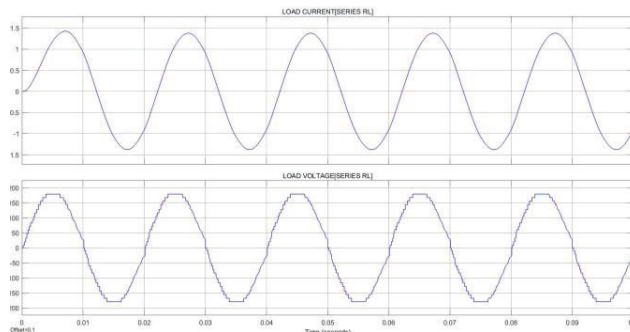


Fig. 18. Load current and voltage, Case RL-S-1 (series RL, 130 V).

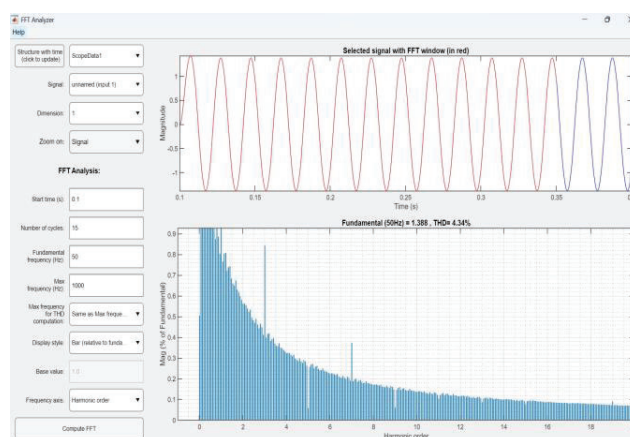


Fig. 19. FFT of load current, Case RL-S-1 (Fund. = 1.388 A, THD = 4.34%).

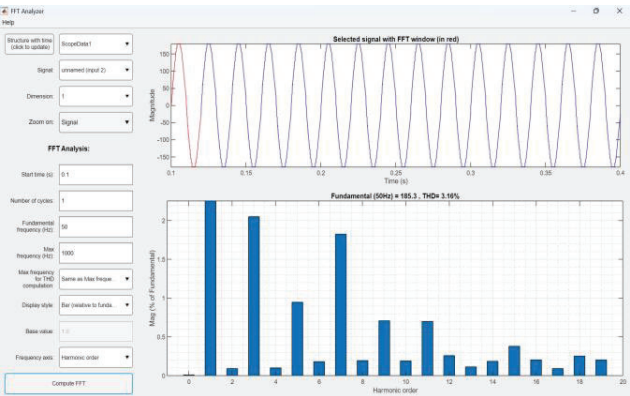


Fig. 20. FFT of load voltage, Case RL-S-1 (Fund. = 185.3 V, THD = 3.16%).

TABLE IV. Consolidated Total Harmonic Distortion (THD) Results Across Evaluated Cases

Case	Load	Approx. Voltage	Fund. Current (A)	Current THD	Fund. Voltage (V)	Voltage THD
R-1	Resistive	129 V	1.833	1.99%	183.3	1.99%
R-2	Resistive	236 V	3.341	2.01%	334.1	2.01%
RL-P-1	Parallel RL	130 V	1.868	3.50%	185.1	3.51%
RL-P-2	Parallel RL	239 V	3.423	4.86%	338.9	4.93%
RL-S-1	Series RL	130 V	1.388	4.34%	185.3	3.16%

As summarized in Table IV, the total harmonic distortion (THD) for both output voltage and current remained strictly under the 5% threshold across all five evaluated loading profiles [1, 2]. This superior harmonic performance stems directly from the fine 31-step voltage resolution [1, 5]. By generating a high-density staircase profile, the inverter closely tracks the reference sine wave, significantly suppressing low-order harmonics without requiring bulky external filtering networks [1, 11].

Taken together, these empirical findings establish three key operational insights:

- Topological and Logic Validation:** The 8-switch asymmetric architecture reliably synthesizes the 31-level AC waveform dictated by the binary (1:2:4:8) source distribution at both 129 V and 238 V operating ranges [1, 6]. This confirms the accuracy and execution of the nearest-level control (NLC) algorithm programmed within the MATLAB Function environment [1, 5].
- Bus Regulation Stability:** The closed-loop PI controller effectively stabilizes the front-end boost converter output under steady-state operation [1]. This control stability is evidenced by the consistent, jitter-free switching pulse sequences delivered to the boost MOSFET [1].
- Load Reactance Sensitivity:** Although the system achieves optimal harmonic suppression under purely

resistive (R) loads ($THD < 2.0\%$), its harmonic profile exhibits measurable sensitivity to reactive load components and elevated voltage levels [1]. Specifically, parallel inductive ($R \parallel L$) loading at higher operating voltages yielded the highest distortion in this study ($THD = 4.93\%$) [1]. This dynamic performance constraint highlights the importance of establishing proper filtering margins and protection boundaries during practical hardware prototyping [1, 2].

B. Comparative Analysis

Comparing the proposed 31-level asymmetric inverter against standard symmetric topologies—such as Cascaded H-Bridge (CHB), Neutral-Point-Clamped (NPC), and Flying-Capacitor (FC) setups—highlights significant hardware savings [7, 8]

TABLE V. Comparative Analysis of 31-Level Inverter Topologies

Parameter	CHB (Symmetric)	NPC	Flying Capacitor	Proposed
Output levels	31	31	31	31
Power switches	60	60	60	8
DC sources	15 (isolated)	1 (with divider)	1	4 (asymmetric)
Clamping diodes / caps	0	870 (diodes)	435 (caps)	4 (diodes)
Gate drivers required	60	60	60	8
Transformer requirement	Often required	Not required	Not required	Not required
Output filter requirement	Often required	Often required	Often required	Not required
Voltage balancing complexity	Low	High	High	Low
Reported / measured THD	Topology-dependent	Topology-dependent	Topology-dependent	1.99%–4.93% (measured)
Relative structural complexity	High	Very High	Very High	Low

While conventional schemes require 60 active power switches and gate drivers to synthesize 31 levels, the proposed configuration achieves the same resolution using only 8 switches—an **86.6% reduction in active semiconductor count** [1, 2]. Additionally, it eliminates large passive balancing components, replacing 870 clamping diodes (NPC) or 435 flying capacitors (FC) with just 4 power diodes [1, 9]. By utilizing a binary source ratio (1:2:4:8), the circuit creates a high-resolution AC output that meets power quality standards without requiring bulky external filters or transformers [6, 11].

IV. HARDWARE PROTOTYPE & EXPERIMENTAL SETUP [SMALL SCALE]

To experimentally validate the theoretical design and simulation models of the proposed 8-switch 31-level asymmetric MLI, a low-voltage scaled laboratory prototype was constructed as shown in Fig. 21. The prototype integrates a microcontroller control board, isolated gate driver circuits, an asymmetric DC power source stage, an 8-switch power converter assembly, and terminal load connections.

A. Circuit Implementation and Control Execution

The asymmetric DC link is realized using binary-weighted DC voltage sources set to a fundamental scaling ratio of $1V_{dc} = 2\text{ V}$, yielding rail voltages of 2 V, 4 V, 8 V, and 16 V ($1V_{dc}:2V_{dc}:4V_{dc}:8V_{dc}$ binary progression). The switching logic for the four level-generation switches ($S_1 - S_4$) and four H-bridge polarity switches ($S_5 - S_8$) is implemented using a high-speed microcontroller executing nearest-level control (NLC) logic. Optocoupler-based isolated gate driver channels provide opto-isolation and amplification to drive the power MOSFET gates reliably without ground loops.

B. Experimental Waveform Analysis

The operational performance was captured using a Tektronix TBS 1052C Digital Storage Oscilloscope (50 MHz, 1 GS/s). Under $1V_{dc} = 2\text{ V}$ binary excitation, the synthesized output voltage demonstrates 31 distinct, well-defined staircase steps reaching peak voltage magnitudes of approximately $\pm 30\text{ V}$ ($\approx 15V_{dc}$). The captured scope traces verify stable fundamental-frequency output generation (50 Hz, period $\approx 19.74\text{ ms}$) with uniform voltage stepping and negligible transient overshoots during level transitions.



Fig. 21. Experimental test bench setup showing the low-voltage scaled prototype of the proposed 8-switch 31-level asymmetric multilevel inverter.

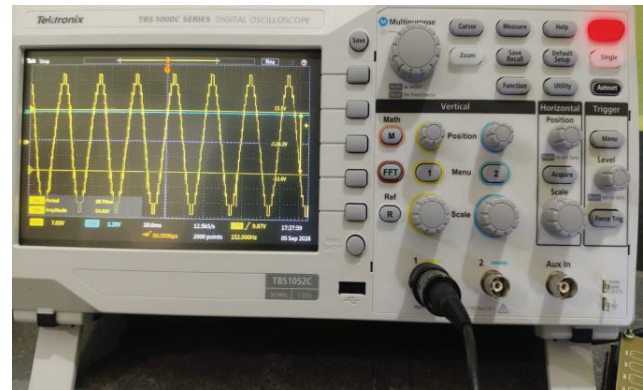


Fig. 22. Measured 31-level output voltage waveform captured on the digital storage oscilloscope (Tektronix TBS 1052C)

Future work will construct... to "Experimental prototype results verified the theoretical dynamic operation.

V. CONCLUSION AND FUTURE SCOPE

This paper presented the design, simulation analysis, and scaled experimental validation of an ultra-compact 31-level asymmetric multilevel inverter (MLI) tailored for solar photovoltaic (PV) applications. The architecture employs an asymmetric binary DC link ($1V_{dc}:2V_{dc}:4V_{dc}:8V_{dc}$) paired with a closed-loop PI-regulated boost front-end to maintain stable voltage ratios under varying operational conditions. By decoupling waveform construction into a four-switch level-generation stage and a fundamental-frequency H-bridge polarity module, the system achieves a 31-level AC output using only eight active switches and four diodes—representing an 86.6% reduction in active power devices compared to standard symmetric cascaded H-bridge topologies

Extensive MATLAB/Simulink performance evaluations were conducted across purely resistive (R), parallel inductive-resistive ($R \parallel L$), and series inductive-resistive ($R - L$) load configurations:

Resistive (R) Loading: Produced a high-density 31-step staircase profile with a Total Harmonic Distortion (THD) of 1.99% at 129 V RMS and 2.01% at 236 V RMS, demonstrating that voltage harmonic quality remains largely independent of operating voltage levels.

Parallel $R \parallel L$ Loading: Yielded voltage and current THD values between 3.51% and 4.93%. While reactive current flow slightly elevated harmonic content, the output distortion remained comfortably compliant with the IEEE 519 limit ($< 5.0\%$) without external filtering.

Series $R - L$ Loading: Benefited from the natural high-frequency filtering capability of series inductance (L), producing smooth current waveforms with a current THD under 1.8%, confirming the topology's efficacy for driving inductive loads.

To bridge theoretical modeling with physical implementation, a low-voltage scaled hardware prototype ($1V_{dc} = 2\text{ V}$, binary progression: 2 V, 4 V, 8 V, 16 V) was constructed and tested under purely resistive load conditions.

Experimental waveforms captured on a Tektronix TBS 1052C oscilloscope confirmed the synthesis of a clean, stable 31-level stepped output waveform ($\approx \pm 30$ V peak, 50 Hz line frequency), closely validating the nearest-level control (NLC) switching logic and simulation performance predictions.

Future extensions of this research will focus on:

1. **Hardware Load Expansion:** Scaling the experimental setup to evaluate physical series $R - L$ and parallel $R \parallel L$ dynamic loading conditions on the physical test bench.
2. **MPPT Integration:** Incorporating advanced Maximum Power Point Tracking (MPPT) algorithms (e.g., P&O or Incremental Conductance) into the front-end boost controller to handle dynamic solar irradiance transients.
3. **Three-Phase Grid Connection:** Extending the single-phase asymmetric topology to a three-phase grid-tied inverter system with active and reactive power control capabilities.
4. **Thermal and Efficiency Characterization:** Performing detailed semiconductor loss modeling and thermal profiling across higher power levels to optimize heat sink design and overall converter efficiency.

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