ETI Inversion Techniques in Memory Architecture

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***Abstract*- The power dissipated in bus level is more complex in VLSI circuits. So switching activity provides savings on the overall power budget. It presents new method of encoding techniques suitable for minimizing the switching activity of system-level address buses. In particular, the schemes such as full inversion, even inversion and odd inversion target the reduction of the average number of bus line transitions that occur in one clock cycle. Experimental results, conducted on address streams generated by a real FPGA, demonstrates the effectiveness of the proposed method. It can reduce the power consumption and improvement in performance level.**

***Keywords- Area, power, marginal noise, performance, cost, ETI inversion*.**

I. INTRODUCTION

Many number of non-volatile flip flops and registers are used in the system .Using more flip-flops area and power consumption is increased in existing process. PaCC compression scheme requires more power due to run length encoding techniques. Previous compression ratio is analysed in compress and compare scheme and is found to be less when compared to in parallel compare and compress scheme. It requires some problem in transmission of data. I transmission of large number of data into the circuit level, collision and congestion problem occurs. The problem is rectified in collision avoidance scheme. Here the technique of run length encoder is used to reduce redundancy of the bit level. This system require an Embedded Transition Inversion (ETI) encoder and decoder. For reducing area and power consumption flip-flop is avoided instead of that microchip is used. Because of using microchip the area is reduced. In existing system the transmission in system level leads to collision. It occurs due to transmission of large number of data per clock cycle. So delay occurs. To avoid delay and glitches from the circuit, the inversion techniques are used. This techniques can minimize the switching activity and latency problem. By this network number of data transmission, the marginal noise is produced, it can overcome by collision aware techniques and inversion scheme. It leads to reduction in data bit level. This inversion take place in fours way to reduce the data level from high to low from that conversion voltage can be reduces so power consumed in the network is low. Therefore power consumption is achieved. During inversion techniques three condition requires to change the data bit level and also the data can be inverted based on selection line. Based on the selection line only given data can be inverted.in this inversion the input have same number of zeros and one means architecture provides comparison in input data whether the input is high in odd term then odd inversion is occurs or the input is high in even terminal means even inversion is occurs. After the data is inverted run length coding encoder is held to compress the data bit level. It reduces data from 16 bit to 2 bit level.

II. LITERATURE REVIEW

This section can reduce the latency and redundancy problem. ETI compression scheme reduce the refresh time per data bit in system level. From existing system only the run length encoder is used for data compression, the data bit level not reduces because more flip-flop and register is required. To avoid collision and compress data bit level inversion techniques is used and also reduce the area and power consumption in the network level.

III. PROPOSED SYSTEM

From ETI encoder four inversion techniques are involved to compress the data bit.

1. Full inversion
2. Odd inversion
3. Even inversion
4. Zero inversion

Inversion techniques are take place due to compress of data length. For example full inversion requires inverting all one as zero and zero as one.

From this inversion techniques, three condition requires to convert the binary bit level and after the compression scheme can be achieved.

Three condition for inversion are

1>0 full inversion
0>1 no inversion
1=0 odd or even inversion

If number of 1's is high means full inversion can be occurs. Following this condition and selection bit level this inversion scheme can be achieved.

Full inversion - All the value can be changed that means all the eight bit valve can be converted

1 1 1 1 1 1 1 1

0 0 0 0 0 0 0 0

The data bit level can be compressed as 00 .So area and power consumption level reduces.

In irregular data bit level also processed in this scheme if more number of zeroes in zigzag form then it can be considered as low .So no need to apply inversion scheme. If it is high then apply inversion scheme to reduce the data bit level power consumption.

From fig.1 it is observed that first binary input is given to the system and the parallel to serial converter is used to convert the binary bit. If the bit is in parallel form then by using this converter it is converted to serial form as they same vice versa is taken where the data bit can be converted from serial to parallel form. After converting the data form binary input can be given to detector ,detector is detect how many ones and zeroes in the binary input and after it can be given to ETI encoder, where this encoder can be used to convert the bit by using four inversion condition

The condition can be requires to conversion of data bit according to its selection line

If the selection line is

00 – full inversion

11 – No inversion

01 – Even inversion

10 – Odd inversion

If number of ones can be high means glitches can be occurred during marginal noise occurs in the circuit. If one have voltage level of 3.3V it can be reduce to 2.5 by this conversion scheme. After inversion of binary data it can be given to input of run length encoder, where the run length encoder can be used to compress the data bit level and produce the size of data from 8 bit to 2 bit level. If the decoder can be used to retain the data from its original, and output can be seen either octal or binary form. This inversion scheme helps to reduce marginal noise, power and output without glitches.

A.BLOCK DIAGRAM

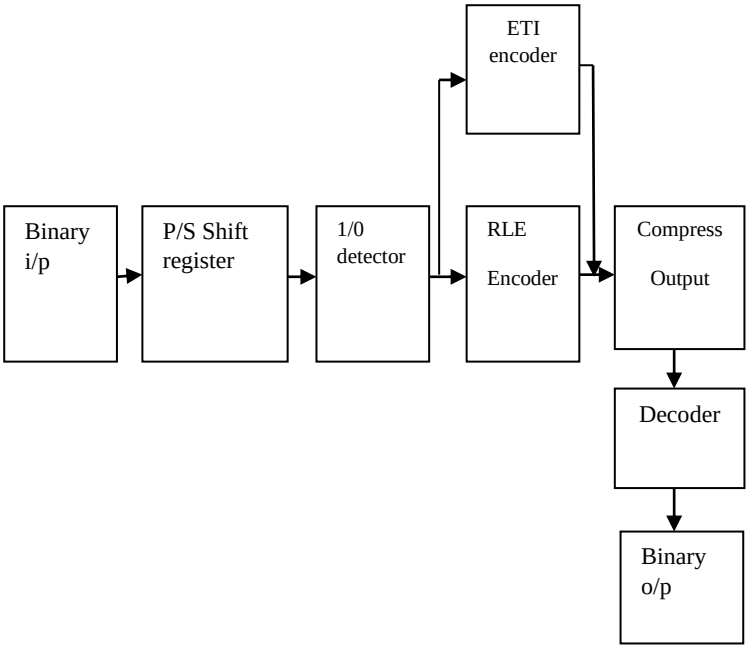

Fig 1: Proposed block diagram

In ETI encoder have inversion techniques. This technique can be used to compress the data bit level. The graphical chart involved to reduce the area and power consumption. From that over all area can be reduced due to reduction of register and flip flops. From that ETI encoder block architecture comparator and controller can be requires .if the comparator can be used which type of inversion can be occur for this binary data bit. Only comparator can be held for this condition 1=0, whether this is odd inversion or even inversion. According to the binary data the condition checks and inversion scheme is applied. If ones can placed the position high in odd term means odd inversion occur and reduce the binary bit level because of that checking process the comparator requires.

Controller requires to control the voltage level from the inversion scheme. If the input level zeroes can be placed in high in the data level then no inversion occurs because already the input level is low by inversion scheme applied means it should be high and power consumption should be high. So the controller is used to reduce the power level during the binary bit transmission. After the compressed binary output is achieved by using the inversion techniques.

IV. EVALUATION RESULTS

In the evaluation PACC can leads to compression of the data bit level. It can be implemented in real time system for more memory space and less power consumption. This scheme reduces the latency and delay in the circuit. IPhone/tablet have system-on-chip integration increasing number of components to offer more functionality. Capacity and effective of data communication between memory and other hardware blocks have become a major concern in the system on chip design. To address this concern, proposed to use Network-on-chip architectures, to meet high bandwidth, and low power and area demands.

A. Area reduction in ETI

From PACC method area is compressed by using design compiler. Based on reduction only 25% to 30% is reduced .By using an inversion techniques scheme, area is reduced up to 33% to 40%. It is efficient and collision problem also be reduced. Area reduction is high less in this scheme, where the binary data level is reduced, size also reduces from 8 bit to 2 bit size can be reduces.

B. Codec performance level

The run length encoder and decoder plays role in PACC method but it is not efficient when reduction of data bit level .So inversion scheme exhibits better performance in reduction of bit level. By this inversion scheme zigzag data is compressed. From that run length encoder requires to compress the binary data bit level from higher order bit to lower bit. From DRAM processor design state diagram representation and state table also exhibits to calculate the analysis report. So area is reduced and power is saved up to 40%. Algorithm state machine design is used to design the memory system. In this representation the memory system achieves smaller size .It saves the power and area compared to design of algorithm level. From the power and area analysis chart area can be minimized up to 35% and power consumption can be reduced up to 57% due to inversion scheme .The refresh time per bit level can be reduces so power consumption in system level reduce. According to the system level overall binary data bit reduces so the area size also reduces. Each and every binary data bit level of its refreshing time also reduces in DRAM

ETI Encoder simulation result:

Fig 3: Encoder simulation result

From that ETI encoder scheme only the data bit level is reduced due to this inversion algorithm. From this result the binary data is compressed by this scheme, and the input is given the clock and should be always rising edge and reset is set as one in initial condition. After that reset is set as zero and the simulation is run in 8 bit level in 8 times. From fig.4 simulation result diagram, full inversion is applied here. The encoder input is eight bit of data and selection line of sel is indicates which type of inversion should occur, the clock should be always rising edge and reset is initially one. After reset is force to zero to produce the inversion output for full inversion scheme and the value is 00000000.In encoder output ten bit is produced, in ten bit eight bit refers to the output bit and first two bit is a selection line .This line indicates which type of the condition of inversion is applied.

V. CONCLUSION

Non Volatile processor have reduced power consumption due to reduce area size .The cost of chip is also be reduced. From advanced codec level of parallel compare and compress scheme it reduces the number of flip flops .According to this techniques, power consumption and bit level compression is reduced by using congestion aware techniques. It can reduce traffic due to data transmission and glitches can be avoided. Network level data

transmission causes congestion problem. It can be avoided by using congestion aware techniques and inversion is used to reduce that data bit level. Hence power consumption, area size and latency problem is reduced.

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