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Although, in the case of the conventional TFET the observed potential change seems to be slightly less than in the other two cases. Concretely, in the conventional TFET, the value of the potential rise is higher near the channel/drain interface, which corresponds to a narrower tunnel barrier width and a smaller Wmin. This compression is related to increased ambipolar current (Iamb). On the other hand, when thickness was set to 4 nm, the recording of a more extensive potential gradient was a sign of a steeper tunnel barrier. However, decreasing the thickness to 2. By applying 5 nm, there is a concomitant of a larger potential gradient meaning a wider tunnel barrier. Overall, these results underscore the importance of having two drain regions. The low-doped region also helps in effectively depleting the drain region at the channel-drain junction and thus enabling reduced tunneling barrier width and ambipolar current control.

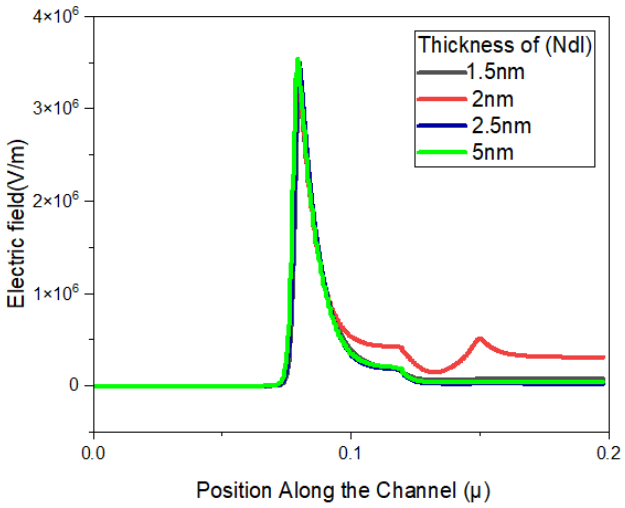

Fig. 7. Electric field of the proposed TFET for different drain doping thickness

Additional electric field analysis was carried out at the varying drain doping thickness, at 1. 5 nm, 2 nm, 2. 5 nm, and 4 nm, as indicated in Figure 7 above. These electric fields are especially useful in high frequency, and their usage cannot be further emphasized. First, there is the high-frequency performance which is most affected by the electric field since it influences the motion of charge carriers. In conditions of high electric field strength, it is easy to make fast and effective transport of these charge carriers. This phenomenon is of much significance in high frequency in the context of radio frequency (RF) as well as microwave communication system. A higher electric field gives the ability to charge carriers to move more rapidly, giving signals a boost. This is a key step in making high data rates and signal frequencies in the RF and microwave communication systems possible. Consequently, electric field intensity determines the span of frequencies that is usable in such applications. Hence, mastering and the proper positioning of electric field strength is a critical aspect of increasing operating frequencies and rates of high-frequency systems, which is one of the overarching goals in modern applications.

1)>Ft=(gm/2)(Cgs+Cgd)

A thorough analysis is carried out on high-frequency operating parameters of FETs, namely transconductance, drain-to-gate capacitance, source-to-gate capacitance, and the most important unit gain cut-off frequency. The results of this analysis are presented in the form of figure 8 which depicts cutoff frequency versus drain doping thickness. When comparing between the source-to-gate and drain-to-gate capacitances capacitance Csg remains invariant at all gate voltage values in both conventional and proposed TFETs. However, it reacts drastically different from the behavior of Cdg. As for the gate voltage below VGS ≈ 1.05 V, in the Cdg of the proposed structure, the upper region thicknesses are observed to be reduced. It is important to note that beyond VGS > 1.05 V, if the upper region thickness is less, then Cdg is slightly less for the thinner thickness regions. The transconductance (gm) has been evaluated in detail based on the thickness of the material at various thicknesses. Evaluating the change of the cutoff frequency with respect to the gate-to-source voltage, contrasting different cases of the proposed method with the conventional TFET. Analyzing the maximum cutoff frequency (fT max) in relation to the values varying from 1 to 10 nm. The understanding from the analysis is clear as crystal based on figure 8. The maximum cutoff frequency (fTmax), which starts with 60 GHz for the conventional structure is improved by a considerable extent when employing two layers of drain doping, beginning the upper layer thickness at 2 nm. The fT max is greatest when th is set at 2; this is an indication that the fT max has reached its optimal frequency. undefined Incredibly, if th is decreased to a dimension of less than 2 nm, fT max suffers a sharp decline. Hence, the choice of th seems to be highly sensitive, and it locates in the vicinity of 2. 5 nm or in its proximity.

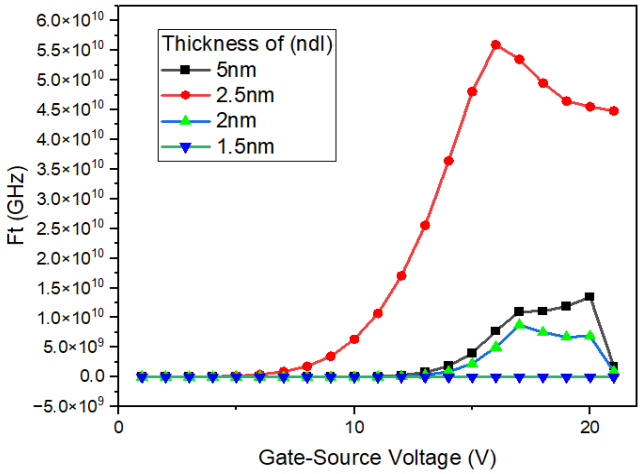

Fig. 8 Frequency of the proposed TFET for different drain doping thickness

In the next step directing focus to the spacer length (Ls) effect on ambipolar current measured at VGS = – 0.8 V and VDS = 1.5 V as well as the maximum cutoff frequency (Ft max). The purpose of this investigation has been performed for two different thickness of upper drain region which is th = 2 nm and th = 3nm. Strikingly, both trends are similar in these two cases. Integrating both the structural engineering with the doping engineering approaches into the device, including attaining a high frequency response greater than prior findings. Engaged in an investigation of important design parameters which substantially affect the performance of the device. From the decreasing ambipolar current (Iamb) at higher spacer length

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(Ls), it is evident that the length of the spacer cannot be increased to freely produce high speed output. This can be accounted for in the fact that the physical separation between the drain contact and the channel–drain interface is considerably longer than in MOSFETs. This results in a well-defined depletion region at the interface and increased distance from the junction. Whenever the spacer length is at 35 nm and above, there is virtually no occurrence of Iamb. But it is crucial to look at the fact that with these increased values of Ls the value of fT max, the maximum cutoff frequency decreases. Hence, it deserves careful thought concerning the selection of the proper value for the "Ls" with the aim of limiting ambipolar current while minimizing the influence used on the HF performance.

Variables	Conventional device	Proposed device
Spacer length (ls)	30nm	28nm
Source Length	80nm	100nm
Drain	80nm	100nm
Channel length	40nm	50nm
Doping thickness	5nm	2.5nm
Frequency	109	10^{10}
Gate work function	4.3ev	4.3ev
Electric field	------	4 x 10^{10}

Table 2: Comparing the Dimensions and Parameters in Simulation: Proposed with Conventional Devices

The effect of heavy doping (Ndh) as well as light doping (Ndl) on both Iamb and fT max must be compared. Figure 5 shows that ambipolar current increases with Ndl. Such behavior is typical for numerous doping of the higher drain region. What makes it much more interesting is that the variation of fT max is also varying as well at the same time. For Ndh of 6×10^18 cm−3 × 7×10^17 cm-3 the fT max shows almost linear dependence on Ndl, but for Ndl above 1×10^18 cm-3, there is a steep fall in the fT max value. For Ndh equal to 5 × 10^18 cm-3 fT max depends on Ndl and with its increase from 0 to 1 × 10^18 cm-3 the value increases and then sharply decreases with addition increase of Ndl. Such results show that there is an optimal method of drain doping that can lead to high frequency performance together with moderate ambipolar current. Sustaining such operation is central to high-frequency operation and thus underlines the precision required for set parameters in a device design.

IV. CONCLUSIONS

In this paper and for further evaluation of the cutoff frequency (fT), we used 2D TCAD simulations coupled with a comprehensive analysis of the structure of the device and drain doping concentrations. We examined four different drain doping thicknesses for the drain doping layers, namely 1. 5nm, 2 nm, 2. The optical band gaps of Composites 1, 2 and 3 were found to be 5 nm, 4 nm respectively. Among them, thickness of 2. Compared with other mob versions, 5 nm displayed the maximum cutoff frequency of response, standing at a record of high-frequency operation. These parameters consisted of the thickness of high doped drain region, spacer length and the dopant concentrations in both the low doped and high doped drain regions. This coverage gave us a better understanding of the influence of these factors on different performance characteristics including ON current, ambipolar current and cutoff frequency among others. Notably, we also observed that the ON-current levels are relatively stagnant irrespective of the design configurations. Furthermore, it was established that capacitance values were significantly boosted, especially up to an initial gate voltage of about 1V. 5 V. More importantly, these results are aligned with the capability to improve high-frequency characteristics based on a rational design strategy, particularly in terms of the changes to the thickness of the upper layer as well as doping levels. Not only does this pitched investigation make high-frequency devices demonstrate their merits, but it also provides us with explicit insights into these merits.

REFERENCES

[1] V. Kilchytska et al., "Influence of device engineering on the analog and RF performances of SOI MOSFETs," IEEE Trans. Electron Devices, vol. 50, no. 3, pp. 577–588, Mar. 2003J. Clerk Maxwell, A Treatise on Electricity and Magnetism, 3rd ed., vol. 2. Oxford: Clarendon, 1892, pp.68-73.

[2] E. Abou-Allam, T. Manku, M. Ting, and M. S. Obrecht, "Impact of technology scaling on CMOS RF devices and circuits," in Proc. IEEE Custom Integr. Circuits Conf., May 2000, pp. 361–364

[3] S. Bangsaruntip, G. M. Cohen, A. Majumdar, and J. W. Sleight, "Universality of short-channel effects in undoped-body silicon nanowire MOSFETs," IEEE Electron Device Lett., vol. 31, no. 9, pp. 903–905, Sep. 2010

[4] J.-P. Colinge, FinFETs Other Multi-Gate Transistors. Berlin, Germany: Springer, 2008.

[5] S. Strangio, P. Palestri, M. Lanuzza, D. Esseni, F. Crupi, and L. Selmi, "Benchmarks of a III–V TFET technology platform against the 10-nm CMOS FinFET technology node considering basic arithmetic circuits," Solid State Electron., vol. 128, pp. 37–42, Feb. 2017.

[6] K. Roy, S. Mukhopadhyay, and H. Mahmoodi-Meimand, "Leakage current mechanisms and leakage reduction techniques in deepsubmicrometer CMOS circuits," Proc. IEEE, vol. 91, no. 2, pp. 305–327, Feb. 2003.

[7] A. M. Ionescu, "New functionality and ultra low power: Key opportunities for post-CMOS era," in Proc. Int. Symp. VLSI Technol., Syst., Appl., Apr. 2008, pp. 72–73.

[8] S. Strangio et al., "Impact of TFET unidirectionality and ambipolarity on the performance of 6T SRAM cells," IEEE J. Electron Devices Soc., vol. 3, no. 3, pp. 223–232, May 2015.

[9] K. Boucart and A. M. Ionescu, "Double-gate tunnel FET with high-κ gate dielectric," IEEE Trans. Electron Devices, vol. 54, no. 7, pp. 1725–1733, Jul. 2007.

[10] A. S. Verhulst, B. Sorée, D. Leonelli, W. G. Vandenberghe, and G. Groeseneken, "Modeling the single-gate, double-gate, and gate-allaround tunnel field-effect transistor," J. Appl. Phys., vol. 107, no. 2, p. 024518, Jan. 2010.

[11] W. Y. Choi, B.-G. Park, J. D. Lee, and T.-J. K. Liu, "Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec," IEEE Electron Device Lett., vol. 28, no. 8, pp. 743–745, Aug. 2007

[12] Semiconductor Industry Association (SIA). (2005). International Technology Roadmap for Semiconductors (ITRS). [Online]. Available: http://www.itrs.net/

[13] S. Agarwal, G. Klimeck, and M. Luisier, "Leakage-reduction design concepts for low-power vertical tunneling field-effect transistors," IEEE Electron Device Lett., vol. 31, no. 6, pp. 621–623, Jun. 2010.

International Journal of Engineering Research & Technology (IJERT)
ISSN: 2278-0181
Vol. 13 Issue 8, August 2024

[14] C. Anghel, P. Chilagani, A. Amara, and A. Vladimirescu, “Tunnel field effect transistor with increased ON current, low-k spacer and high-k dielectric,” Appl. Phys. Lett., vol. 96, no. 12, p. 122104, Mar. 2010.
[15] D. B. Abdi and M. J. Kumar, “In-built N+ pocket p-n-p-n tunnel field-effect transistor,” IEEE Electron Device Lett., vol. 35, no. 12, pp. 1170–1172, Dec. 2014.
[16] W. Cao, C. J. Yao, G. F. Jiao, D. Huang, H. Y. Yu, and M.-F. Li, “Improvement in reliability of tunneling field-effect transistor with p-n-i-n structure,” IEEE Trans. Electron Devices, vol. 58, no. 7, pp. 2122–2126, Jul. 2011.
[17] R. Jhaveri, N. V. Nagavarapu, and J. C. S. Woo, “Effect of pocket doping and annealing schemes on the source-pocket tunnel field-effect transistor,” IEEE Trans. Electron Devices, vol. 58, no. 1, pp. 80–86, Jan. 2011.
[18] H.-Y. Chang, B. Adams, P.-Y. Chien, J. Li, and J. C. S. Woo, “Improved subthreshold and output characteristics of source-pocket Si tunnel FET by the application of laser annealing,” IEEE Trans. Electron Devices, vol. 60, no. 1, pp. 92–96, Jan. 2013.
[19] S. Saurabh and M. J. Kumar, “Impact of strain on drain current and threshold voltage of nanoscale double gate tunnel field effect transistor: Theoretical investigation and analysis,” Jpn. J. Appl. Phys., vol. 48, no. 6R, p. 064503, Jun. 2009.
[20] W. Y. Choi and W. Lee, “Hetero-gate-dielectric tunneling fieldeffect transistors,” IEEE Trans. Electron Devices, vol. 57, no. 9, pp. 2317–2319, Sep. 2010.
[21] M. J. Lee and W. Y. Choi, “Effects of device geometry on hetero-gatedielectric tunneling field-effect transistors,” IEEE Electron Device Lett., vol. 33, no. 10, pp. 1459–1461, Oct. 2012.
[22] B. Raad, K. Nigam, D. Sharma, and P. Kondekar, “Dielectric and work function engineered TFET for ambipolar suppression and RF performance enhancement,” Electron. Lett., vol. 52, no. 9, pp. 770–772, Apr. 2016.
[23] A. S. Verhulst, W. G. Vandenberghe, K. Maex, and G. Groeseneken, “Tunnel field-effect transistor without gate-drain overlap,” Appl. Phys. Lett., vol. 91, no. 5, p. 053102, Jul. 2007.
[24] J. Zhuge et al., “Digital-circuit analysis of short-gate tunnel FETs for low-voltage applications,” Semicond. Sci. Technol., vol. 26, no. 8, p. 085001, Aug. 2011.
[25] J. Madan and R. Chaujar, “Gate drain underlapped-PNIN-GAA-TFET for comprehensively upgraded analog/RF performance,” Superlattices Microstruct., vol. 102, p. 17–26, Feb. 2017.
[26] S. Ahish, D. Sharma, Y. B. N. Kumar, and M. H. Vasantha, “Performance enhancement of novel InAs/Si hetero double-gate tunnel FET using Gaussian doping,” IEEE Trans. Electron Devices, vol. 63, no. 1, pp. 288–295, Jan. 2016.
[27] V. Vijayvargiya and S. K. Vishvakarma, “Effect of drain doping profile on double-gate tunnel field-effect transistor and its influence on device RF performance,” IEEE Trans. Nanotechnol., vol. 13, no. 5, pp. 974–981, Sep. 2014.
[28] B. R. Raad, K. Nigam, D. Sharma, and P. N. Kondekar, “Performance investigation of bandgap, gate material work function and gate dielectric engineered TFET with device reliability improvement,” Superlattices Microstruct., vol. 94, pp. 138–146, Jun. 2016.
[29] S. Saurabh and M. J. Kumar, “Novel attributes of a dual material gate nanoscale tunnel field-effect transistor,” IEEE Trans. Electron Devices, vol. 58, no. 2, pp. 404–410, Feb. 2011.
[30] S. Kumar and B. Raj, “Analysis of ION and Ambipolar Current for Dual-Material Gate-Drain Overlapped DG-TFET,” J. Nanoelectron. Optoelectron., vol. 11, no. 3, pp. 323–333, Jun. 2016.
[31] H. Wang et al., “A novel barrier-controlled tunnel FET,” IEEE Electron Device Lett., vol. 35, no. 7, pp. 798–800, Jul. 2014.
[32] D. B. Abdi and M. J. Kumar, “Controlling ambipolar current in tunneling FETs using overlapping gate-on-drain,” IEEE J. Electron Devices Soc., vol. 2, no. 6, pp. 187–190, Nov. 2014.
[33] S. Sahay and M. J. Kumar, “Controlling the drain side tunneling width to reduce ambipolar current in tunnel FETs using heterodielectric BOX,” IEEE Trans. Electrons Devices, vol. 62, no. 11, pp. 3882–3886, Nov. 2015
[34] E.-H. Toh, G. H. Wang, G. Samudra, and Y.-C. Yeo, “Device physics and design of double-gate tunneling field-effect transistor by silicon film thickness optimization,” Appl. Phys. Lett., vol. 90, p. 263507, Jun. 2007.
[35] S. Mookerjea, R. Krishnan, S. Datta, and V. Narayanan, “On enhanced Miller capacitance effect in interband tunnel transistors,” IEEE Electron Device Lett., vol. 30, no. 10, pp. 1102–1104, Oct. 2009. [36] ATLAS Device Simulation Software, Silvaco Inc., Santa Clara, CA, USA, 2015.
[36] P. M. Solomon et al., “Universal tunneling behavior in technologically relevant p/n junction diodes,” J. Appl. Phys., vol. 95, no. 10, pp. 5800–5812, May 2004.
[37] A. Shaker, M. El Sabbagh and M. M. El-Banna, "Influence of Drain Doping Engineering on the Ambipolar Conduction and High-Frequency Performance of TFETs," in IEEE Transactions Electron Devices, vol. 64, no. 9, pp. 3541-3547, Sept. 2017, doi: 10.1109/TED.2017.2724560.