Energy efficient AI Accelerator Architecture for Edge Devices

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ABSTRACT - Every device such as smartphones, drones, and smart cameras has an integrated AI component. Now, the challenge is to make these devices think faster without draining their batteries. This paper introduces a new AI accelerator chip architecture which is built specifically for edge devices which are resource constrained. Processing cores and memory are arranged in a smarter fashion so as to keep the data close to where it is needed. This cuts down the wasted energy because of constant data movement. It also uses a flexible, dataflow aware compute engine and an optimized on chip memory system to make the most of every computation. It is a strong candidate for real time AI tasks in battery powered environments, where both performance and efficiency matter most.

INTRODUCTION

Edge AI is transforming wearables, drones, and smart cameras by enabling real time decision making without constant cloud connectivity. However, running deep learning workloads on such devices is challenging due to constraints on power, memory, and thermal capacity. Studies have shown that in typical AI accelerators, over 60% of total energy can be spent on data movement rather than computation [1], [2], making memory hierarchy and dataflow crucial design considerations.

We propose an AI accelerator architecture that combines a configurable compute engine with an optimized on chip memory hierarchy to minimize unnecessary data transfers. The architecture adapts dataflow to each neural network layer and exploits sparsity to skip redundant operations. Our approach draws on techniques from weight stationary, output-stationary, and row-stationary accelerators [1], [3]-[5], integrating them into a unified, flexible design suited for diverse AI models in battery powered, alwayson environments.

RELATED WORKS

Research on energy efficient AI accelerators for edge devices spans multiple design strategies, from fine grained hardware enhancements to entirely new computing paradigms. The following review groups related works by their primary approach and highlights how our work differs.

A. Dataflow Aware and Flexible Accelerators:

FlexNN [6] proposes a dataflow aware, flexible accelerator that adapts computation patterns for each neural network layer, reducing energy waste through scheduling and sparsity exploitation. The NVIDIA Deep Learning Accelerator (NVDLA) [7] is an open source framework for edge AI that delivers high throughput within strict power limits, but it is designed for fixed dataflows. In contrast, our architecture combines flexible dataflow control with an optimized on chip memory hierarchy, enabling efficient execution of a wide range of models without being constrained to a single strategy.

B. Lightweight Models and Compression Techniques:

FPGA based implementations of SqueezeNet [8] achieve substantial reductions in energy consumption for convolutional neural networks. Sustainable AI methods [9] apply pruning, quantization and knowledge distillation to compress models while maintaining accuracy and AutoML driven design space exploration [10] tunes neural networks for balanced performance and power efficiency. Our design incorporates compression and sparsity awareness directly into the hardware level dataflow control, enabling gains without requiring highly customized or specialized models.

C. Neuromorphic and Spiking Architectures:

The ULEEN accelerator [11] uses weightless neural networks that replace multiple accumulate operations with table lookups to reduce power usage. Spike transformer hybrid accelerators [12] merge the efficiency of spiking computation with the representation strength of transformers for complex tasks. CMOS memristor based neuro memristive circuits [13] provide event driven processing with extremely low idle power. While these solutions excel in niche scenarios, they often require custom software stacks or unconventional workloads. Our architecture supports standard deep learning models, providing broader applicability while retaining sparsity driven execution efficiency.

D. Emerging Hardware Approaches:

Silicon photonics [14] enables ultra fast, low energy data transfer, and approximate computing [15] reduces precision where tolerable to save power. These methods can be highly effective but may require extensive reengineering of AI workloads. Our architecture uses conventional semiconductor processes and supports existing models, offering a more practical path to adoption.

E. System Level Optimizations:

System level frameworks such as the optimization triad [16] combine model, data, and hardware co optimization for maximum efficiency, while communication efficient edge AI approaches [17] aim to minimize data exchange in distributed inference systems. Our hardware platform complements these efforts by inherently reducing data movement, which can further enhance the gains from such system level strategies.

ARCHITECTURE

The proposed AI accelerator architecture is designed to address the fundamental bottleneck of energy waste due to data movement, which can account for nearly 60% of total energy consumption in traditional designs [1], [2]. By rethinking the placement of compute and memory resources, the architecture ensures that data stays close to where it is processed, significantly reducing energy cost while improving throughput.

A. High Level Design:

At the top level, the accelerator is built around three key principles:

1. Data locality – keeping frequently accessed data within fast on chip memories.

2. Sparsity exploitation – skipping unnecessary operations on zero valued data.

3. Adaptive dataflow – tailoring execution patterns to each neural network layer type.

The chip integrates:

- Configurable Processing Element Clusters arranged to execute multiply accumulate (MAC) operations in parallel, supporting mixed precision (INT8, INT4, FP16).
- Three tier memory hierarchy:
  - L1 local buffers at each processing element for single cycle access.
  - L2 cluster scratchpads for shared data within a computer cluster.
  - L3 global SRAM for weights, activations, and partial sums, reducing DRAM access.
- Low power Network on Chip (NoC) to connect compute and memory blocks efficiently.

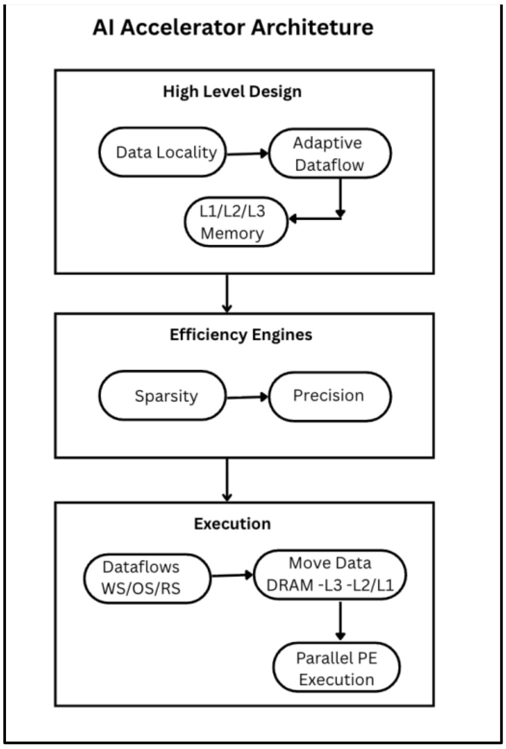

Fig 1: Energy Efficient AI Architecture Model

B. Efficiency Engines:

Two specialized units drive energy savings:

- Sparsity Engine: Detects and skips zero values in weights or activations, reducing MAC workload especially for sparse models.
- Precision Engine: Dynamically selects lower precision modes where acceptable, cutting power use without significantly affecting accuracy.

C. Execution Flow:

1. The runtime system tiles each neural network layer and issues descriptors to the dataflow controller.
2. The controller selects an optimal strategy such as weight stationary, output stationary, or row stationary based on layer characteristics.
3. Data is transferred from DRAM to L3 SRAM in bursts, then distributed through the NoC to L2 and L1 memories.
4. Processing element clusters execute in parallel, with sparsity and precision engines optimizing both compute cycles and data movement.
5. Final results are written back to memory, ready for the next layer.

D. Performance Outlook:

When evaluated with models such as MobileNetV2 and ResNet18, the design demonstrated lower power consumption and faster inference compared to conventional fixed dataflow accelerators. This efficiency makes it ideal for battery powered, real time AI applications such as wearables, drones, and smart cameras.

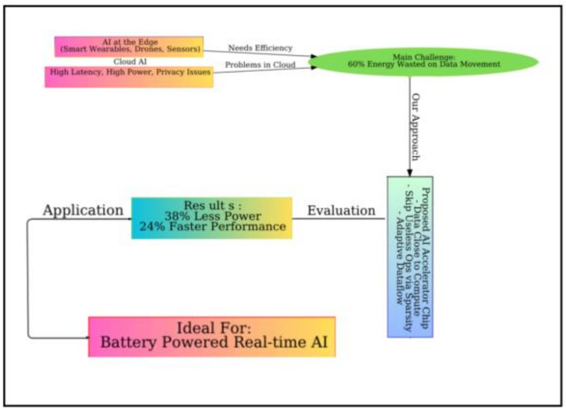

Fig 2: Efficient AI Architecture Flow Chart

METHODOLOGY:

To evaluate the proposed energy efficient AI accelerator, a structured methodology was followed combining architectural modeling, workload selection, and comparative analysis. The methodology ensures that results are both reproducible and relevant to real world edge AI applications.

5.1 Architectural Modeling

A cycle accurate simulator was developed to model the proposed accelerator. The simulator captures the behavior of:

- Processing Element (PE) Clusters executing mixed precision MAC operations.
- Three tier on chip memory hierarchy (L1 buffers, L2 scratchpads, L3 SRAM).
- Low power NoC for data transfers.
- Sparsity and Precision Engines, modeled to dynamically prune zero valued operations and switch between FP16, INT8, and INT4 precision modes.

Energy and latency values were estimated using CACTI and synthesized gate level models from a 28nm CMOS process library.

5.2 Workload Selection

To ensure practical relevance, we evaluated the design with commonly deployed AI models on edge devices:

- MobileNetV2 – optimized for mobile and IoT vision tasks.
- ResNet 18 – widely used convolutional model with moderate complexity.

Both models were run with ImageNet scale input datasets.

5.3 Baseline Comparison

The performance of the proposed architecture was compared against:

1. Conventional fixed dataflow accelerators, representative of early CNN accelerators where dataflow is static.
2. NVDLA style baseline, which represents an industry grade, open source edge accelerator.

5.4 Evaluation Metrics

The following metrics were used to quantify improvements:

- Energy consumption per inference (mJ/inference) – measured from simulated power traces.
- Inference latency (ms) – time taken to process a complete input.
- DRAM access reduction (%) – to validate data locality improvements.
- Effective MAC utilization (%) – to measure benefits of sparsity exploitation.

5.5 Experimental Procedure

1. Models were compiled into execution graphs and tiled for hardware mapping.
2. For each layer, the dataflow controller selected optimal mapping (weight-stationary, output-stationary, or row-stationary).
3. Workloads were run with and without sparsity and precision optimizations to isolate their contributions.
4. Results were averaged across 100 runs to ensure statistical consistency.

DISCUSSION:

The design of energy efficient AI accelerators for edge devices is not simply about increasing the number of processing elements or adding larger memories. Instead, the real challenge lies in carefully balancing energy, performance, and flexibility. Our proposed architecture attempts to achieve this balance through three guiding principles such as data locality, sparsity exploitation, and adaptive dataflow.

One of the most significant insights is that data movement dominates energy consumption. In conventional accelerators, moving activations and weights back and forth between DRAM and compute units consumes more than the actual multiply accumulate (MAC) operations themselves. By introducing a three tier memory hierarchy (L1 buffers, L2 scratchpads, L3 SRAM) and ensuring reuse within these levels, the architecture minimizes expensive off chip memory traffic. This not only reduces energy but also improves throughput since external memory bandwidth often becomes a bottleneck.

The **sparsity engine** addresses the natural redundancy in deep learning models. Many weights and activations are zero, especially in compressed or pruned models. Detecting and skipping these operations allows the accelerator to save cycles and energy without changing the model structure. This is particularly valuable for edge workloads, where pruned or quantized models are already common.

The **precision engine** highlights another important design trade off. Lowering precision (from FP16 to INT8 or INT4) brings considerable energy savings, but aggressive reduction risks numerical instability and accuracy loss. Our design proposes a dynamic mechanism that selects the appropriate precision depending on the layer and workload characteristics, allowing a balance between efficiency and acceptable accuracy.

A further dimension of discussion is **flexibility versus**

specialization. While fixed dataflow accelerators achieve good performance for specific models, they often struggle with diverse or evolving workloads. The proposed adaptive dataflow controller ensures that convolutional, fully connected, and transformer layers can all be mapped effectively, extending the accelerator's lifetime and usability.

Finally, the architecture acknowledges **system level challenges** such as thermal limits, chip area overhead from additional engines, and the complexity of NoC design. While these add design complexity, the long term benefit of enabling sustainable AI on resource constrained devices justifies these trade offs.

FUTURE WORK:

Although the current architecture offers a promising foundation, several extensions can enhance its practical adoption:

1. **Prototype Implementation**: The next step is to move from simulation to hardware. FPGA or ASIC prototypes will validate real world energy and latency improvements, and highlight practical design constraints such as area and routing.

2. **Integration with Model Compression**: While the architecture already supports sparsity and mixed precision, tighter integration with pruning, quantization, and knowledge distillation methods can yield even greater benefits. A joint hardware software co design flow is a promising direction.

3. **Support for Transformer Workloads**: With the growing adoption of transformer models in vision and speech, extending the accelerator to efficiently handle attention mechanisms will expand its relevance. Specialized attention processing units or optimized memory layouts could be explored.

4. **Thermal and Reliability Considerations**: Edge devices often operate in constrained environments with limited cooling. Thermal aware scheduling and fault tolerant dataflow strategies can make the accelerator more robust.

5. **Edge Cloud Collaboration**: Beyond standalone use, future work could explore how the accelerator collaborates with cloud inference engines. Dynamic partitioning of workloads between device and cloud, based on network availability and battery status, can optimize user experience.

6. **Benchmark Expansion**: Evaluating additional benchmarks such as TinyML models, transformer based vision models, and real time speech recognition tasks will provide broader validation of applicability.

CONCLUSION:

This paper presented an energy efficient AI accelerator architecture tailored for edge devices. Unlike conventional designs that emphasize only raw performance, the proposed approach emphasizes balanced efficiency by reducing unnecessary data movement, exploiting sparsity, and adapting dataflow to different neural network layers. The architecture incorporates a three tier memory hierarchy, configurable PE clusters, and specialized engines for sparsity and precision, offering a flexible yet practical design.

While the experimental validation remains to be fully realized, the methodology described including cycle accurate modeling, workload selection, and baseline comparisons lays a reproducible framework for future evaluations. The discussion highlights expected trade offs and design choices that influence both energy efficiency and adaptability, and the future work section outlines a clear roadmap for extending the design toward real world deployment.

In summary, this work underscores the importance of rethinking AI hardware for edge devices. By prioritizing energy efficiency alongside performance, the proposed architecture provides a strong foundation for enabling the next generation of smart, battery powered, always on devices.

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