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Employment Compensation Capacitor to Improve Two Stage CMOS Operational Amplifier Design

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***Abstract* - This paper exhibits a decently characterized system for the design of two stage CMOS operational amplifiers according to given specifications. In order to achieve design operates at this limitation and analyze the effect of various aspect ratios on the characteristics of this operational amplifiers (Op-Amp), by CMOS technology. This paper focused on Employed Compensation capacitor to improved CMOS (Op-Amps) design work. Both the theoretical calculations and computer aided simulation analysis have been given in details. Design has been carried out in T-Spice as tool. The results accomplished by the simulation justify the given parameters and are very acceptable.**

Keywords: Analog Circuit, Phase Margin, Gain margin, CMOS, Unity Gain-bandwidth and, Compensation capacitor.

I. INTRODUCTION

There are many of techniques that can help us to overcome on the issues related with mismatches during layout of CMOS circuits. The designing of Op-Amps puts new challenges in low power applications with reduced channel length devices. Advancements which have appeared recently through new techniques and technologies, give us multiple alternatives in implementations. Involvement of Design Automation tools in analog and mixed signal design is still not matured as it is in the digital design domain. Accommodation of short channel effects in Design Automation for mixed-signal design is also challenging task for EDA designers.

Operational amplifiers with moderate DC increases, high yield swings and sensible open-circle pick up transmission capacity item (GBW) are typically actualized with two-stage structures. Without recurrence remuneration, these Op-Amps are not steady in shut circle applications [1]. Various recurrence remuneration systems are proposed to balance out a shut circle two-stage speaker [2]. Among them, course pay is getting to be more prevalent in fast applications [3].

This is because of the way that it brings about lower power utilization (with comparative rate), higher speed (with comparable power utilization), and higher power supply dismissal degree (PSRR) when contrasted with its significant rivals like Miller pay [4]. By the by, the investigation of course repaid Op-Amps is to some degree muddled. The principle explanation behind this intricacy is the increment in the request of the framework after the pay is connected. These outcomes in a significant outlining exertion for the planner to discover the advanced transistor measurements and predisposition streams before executing the circuit into silicon pass on [5]

CMOS technology continues to mature with minimum feature sizes now. Designing high performance analog integrated circuits is becoming increasingly exigent with the relentless trend toward reduced supply voltages and transistor channel length. A large part of the success of the MOS transistor is due to the fact that it can be scaled to increasingly smaller dimensions, which results in higher performance [6]. The highlight size of individual transistor is lessening from no-limit entirety micrometer (DSM) to much nanometer area. As the size of blend enhances, more transistors, speedier and littler than their antecedent, are being stuffed into a chip. This prompts the unfaltering development of the working recurrence and transforming limit every chip [7].

In this paper applied the method to a specific two stage CMOS op-amp. The simulation results have been obtained CMOS technology. Design has been carried out in T-spice tool.

II. TWO-STAGE OPERATION AMPLIFIER DESECRATION

MOS Op-Amps are everywhere integral parts in various analog and mixed- signal circuits and systems. Op-Amps are the intensifiers that have sufficiently high forward gain so that when negative feedback is connected, the shut circle exchange capacity is essentially autonomous of the addition of the Op-Amp [8-9]. This guideline has been abused to create numerous valuable simple circuits and frameworks. The essential necessity of an Op-Amp is to have an open circle pick up that is sufficiently substantial to actualize the negative input idea [10]. The specific two-stage CMOS Op-Amp was consider as shown in Figure (1).The circuit consists of an input differential transconductance stage forms the input of the Op-Amp followed by common-source second stage. The common source second stage increases the DC gain by an order of magnitude and maximizes the output signal swing for a given voltage supply. This is important in reducing the power consumption [11-12]. If the Operation-Amplifier must drive a low resistance load the second stage must be followed by a buffer stage whose objective is to lower the output resistance and maintain a large signal swing

[13-14]. Bias circuit is provided to establish the operating point for each transistor in its quiescent stage. Compensation is required to achieve stable closed loop performance [15-16]. However, due to an unintentional feed forward path through the Miller capacitor, a right-half-plane (RHP) zero is also created and the phase margin is degraded. Such a zero, however, can be removed if a proper nullifying resistor is inserted in series with the Miller capacitor [17].

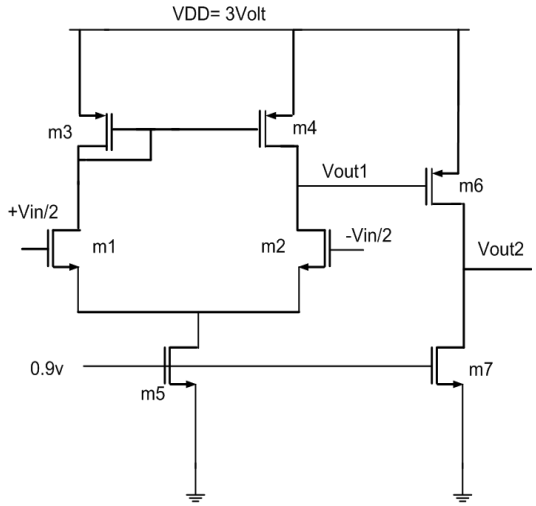


Figure (1) schematic of two stage Op-Amp

In this paper the design of an Op-Amp, numerous electrical characteristics, gain-band width, slew rate, common-mode range, output swing, offset, all have to be taken into consideration. This Op-Amp is a generally utilized universally useful Op-Amp; it discovers applications for instance in exchanged capacitor channels, simple to computerized converters, and sensing circuits.

III. CMOS OP-AMP DESIGN AND CONSIDERATION

Figure (2) shows the Op-Amp Schematic of an unbuffered, two-stage CMOS Op-Amp with N-channel input pair Fundamental Implications.

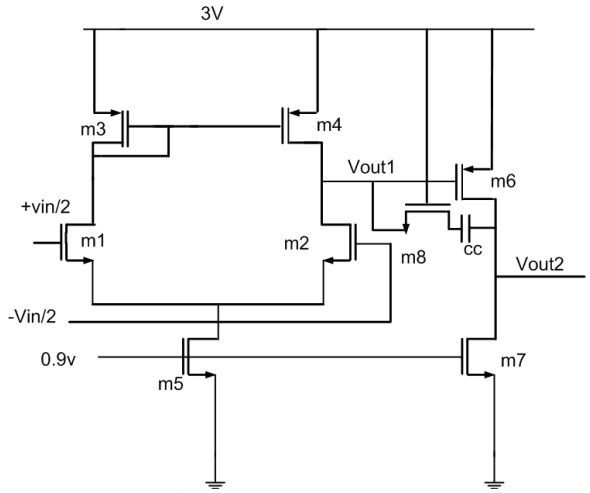


Figure (2) schematic of two stage Op-Amp with C_C and Nulling transistor

Table (1) Design Specifications of the operation amplifier

Parameter	***SPECIFICATIONS***
A_v	85 dB >
GB	20MHz >
Output Voltage Swing	2.1V >
Slew Rate	9 V / µs
P_D	< 1 Mw
Input Common Mode Range	1.7V >
Phase Margin	55^0 >
Gain margin	27 dB >

The topology of this paper is that of a regular CMOS Op-Amp. It included two subsections of circuits, namely differential gain stage and second gain stage. It was finding that this topology was able to successful convene all of the design condition. Examining the subsections further will provide valuable insight into the operation of this amplifier as follow:

A. Differential Gain Stage

The first section of interest is the differential gain stage, which is contained transistors M1 through M4. Transistors M1 and M2 are standard N channel MOSFET (NMOS) transistors, which development the essential information period of the intensifier. The door of M1 is the changing data and the entryway of M2 is the non-altering information. A differential information sign associated over the two data terminals will be increase according to the expansion of the differential stage. The gain of the stage is basically the transconductance of M2 times the aggregate yield resistance seen at the channel of M2. The two primary resistances that add to the yield resistance are that of the data transistors themselves and the yield resistance of the dynamic burden transistors, M3 and M4. The current mirror dynamic burden utilized as a part of this circuit has three particular favorable circumstances. To start with, the utilization of dynamic burden gadgets makes a vast yield resistance in a generally little measure of pass on territory. At long last, the heap assists with regular mode dismissal proportion.

B. Second Gain Stage

The purpose of the second gain stage, as the name infers, is to give extra pick up in the enhancer. Comprising of transistors M6 and M7, this stage takes the yield from the channel of M2 and enhances it through M6, which is in the standard basic source setup. Once more, like the differential addition arrange, this stage utilizes a dynamic gadget, M7, to serve as the heap resistance for M6. The addition of this stage is the transconductance of M6 times the powerful load resistance embodied the yield resistances of M6 and M7.

C. *Methodology Of Op-Amp Design*

Determine the necessary open-loop gain as following

$$I_D = \frac{K}{2}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \quad (1)$$

$$g_m = \sqrt[2]{\frac{2\ I_D\ K\ W}{L}} \quad (2)$$

$$GB = \frac{g_{m\,1}}{2\pi * C_C} \quad (3)$$

$$AV_1 = \frac{g_{m1}}{gds2 + gds4} \quad (4)$$

$$gds = \frac{1}{rds} = \frac{1}{\lambda \times I_D} \quad (5)$$

$$P_1 \cong \frac{1}{2\pi g m_{II} r_I r_{II} C3} \quad (6)$$

$$P_2 \cong \frac{1}{2\pi P_1 r_I r_{II}(C1C2 + C3C1 + C3C2)} \quad (7)$$

$$R_Z = \frac{1}{gm_{II}} + \frac{1}{C_C P_2} \quad (8)$$

$$R_Z = \frac{1}{K\left(\frac{W}{L}\right)(V_{GS} - V_T)} \quad (9)$$

$$P_D = Total\ current \times V_{DD} \quad (10)$$

$$Slew\ Rate = \frac{I_{SS}}{C_C} \quad (11)$$

$$Slew\ Rate = \frac{dy}{dx} \quad (12)$$

$$PSRR^+ = \frac{AOL}{vout/_{v^+}} \quad (13)$$

$$PSRR^- = \frac{AOL}{vout/_{v^-}} \quad (14)$$

Where
I_D is Drain bias current of transistor
V_{GS} is the Gate-source voltage,
$V_{T\,is}$ threshold voltage
K is the Transconductance Parameter
g_m is the transconductance
λ is channel-length modulation parameter (volts^{-1})
rds is output resistance.
C1, C2 and C3 are parasitic capacitance.

All transistors are assumed to be at saturation operation region for (1) - (14).

IV. DESIGN PARAMETERS

Table (2) the design parameters of NMOS and PMOS Transistors

Type of MOS									
NMOS					*PMOS*				
M	***Stage No.***	$V_{GS}(volt)$	$I_D(\mu A)$	$\left(\frac{W}{L}\right)(\mu m)$	***M***	***Stage No.***	$V_{SG}(volt)$	$I_D(\mu A)$	$\left(\frac{W}{L}\right)(\mu m)$
M_1	First	0.531	7	80	M_3	First	0.7	8	9
M_2	First	0.531	7	80	M_4	First	0.7	8	9
M_5	First	0.9	16	1.5	M_6	second	0.7	75	77
M_7	Second	0.9	75	8.5					

V. SIMULATION RESULTS

In AC- Analysis determination of Phase margin, Gain and GB of the Op-Amp. Both Gain and Phase margin are calculated using DC operating point and AC analysis. From Figure (1), Determine the current in the first stage based upon proper mirroring and minimum values for M_2 and M_4. The voltage gain (AV_1) in the first stage is given in equation (4).

- To calculate The Common-Mode Gain (A_{CM}) The input voltage is varies from 0-3V and the linear range of the graph shown in Figure (3). The common-mode gain is A_{CM}=1.506 that got by finding two focuses as far separated in the direct range about the working point. Point max (1.88, 2.83), Point min (0.337, 0.506).

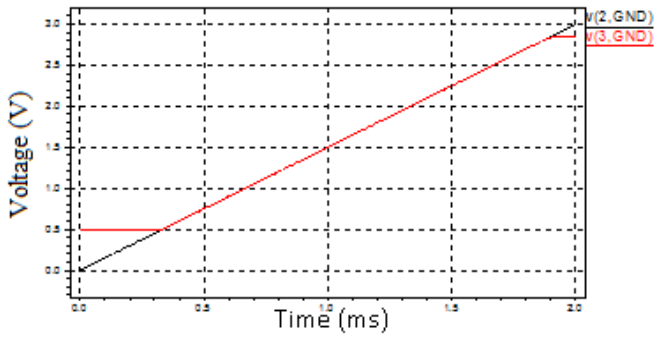
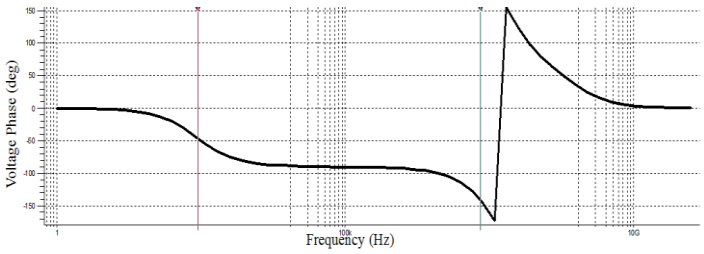


Figure (3) CMRR curve from T-Spice

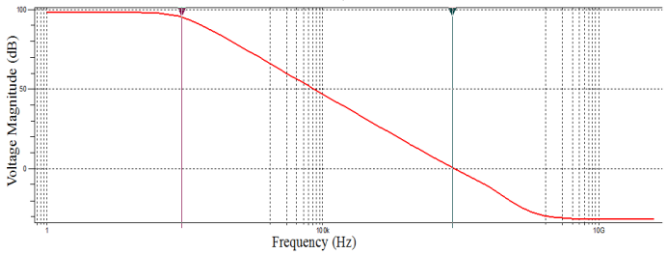
-Gain and phase margin with capacitance (Cc):

In Figure (4a&b), Compensation capacitor moved the pole 2 further, GB of 20MHz and phase margin (40^0). The Op-Amp will clearly be unstable. Since the open loop gain of the Op-Amp to be much less than one when the phase shift is 180^0.

At the same time, move the higher frequency pole, f2, higher in frequency (to split the poles).to solve this problem added R_Z to getting phase margin than with R_Z.



a)



b)

Figure (4)compensation (Cc) with Voltage Phase,
b) compensation (Cc)with voltage magnitude

-Improvement of Phase Margin: To Improve phase margin and To eliminate the zero Nulling Resistor was used, Figure (5) shows that the unity –gain GB is 37.23MHz while the zero moved down to unity –gain frequency . after that the system been stable. In stability case the parameter gain margin (GM) 30dB and phase margin (PM) 60^0 was calculated.

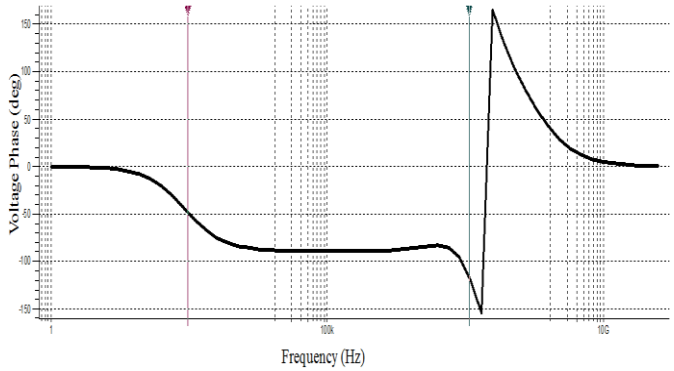


Figure (5) a) compensation (Cc,Rz)with Voltage Phase

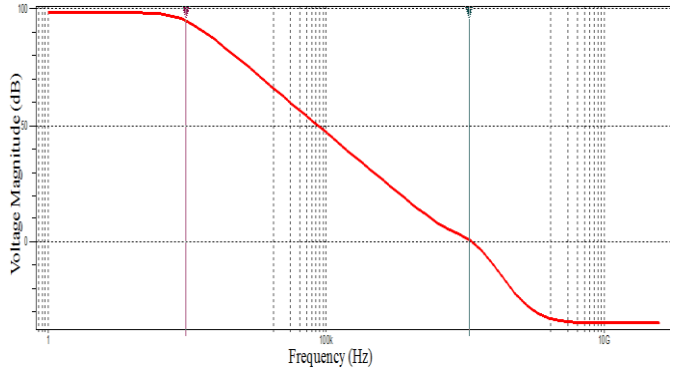


Figure (5) b) compensation (Cc,Rz)with Voltage Magnitude

-Output Swing

The transistor at the second stage is bias for the maximum output swing. Total allowable swing is estimate to be 2.4Volt, as comparing the output swing of the Op-Amp from simulation that the output swing is 2.58Volt as shown in Figure (6).

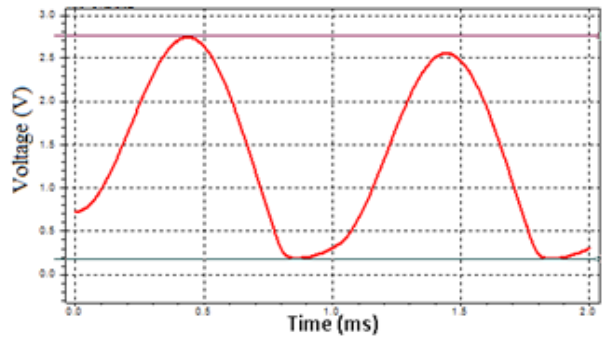


Figure (6) output swing of Op-Amp

-Slew Rate of Op-Amp: The total maximum current can be source and drain from the Op-Amp for the large signal operation determine the value of the slew rate of the Op-Amp is $8V/\mu s$ can be express in equation (11). Slew rate of simulation transient response as shown in Figure (7) is $14V/\mu s$ this is computed from two points on the rising edge. That is in equation (12).

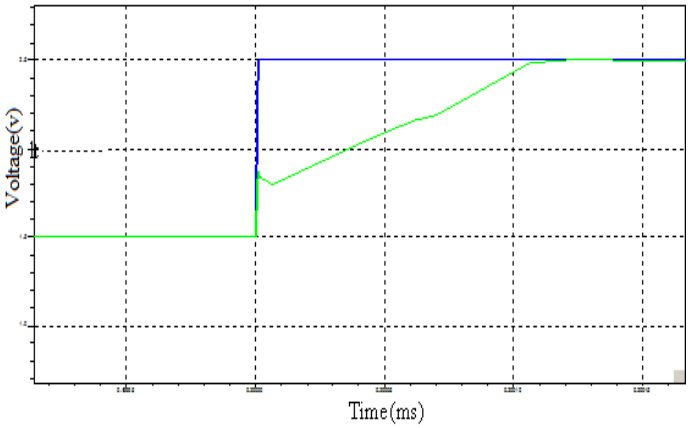


Figure (7) slew Rate measure from the slope of curve

Figure (8&9) shows The Positive Power Supply Rejection Ratio ($PSRR^+$) is measure by setting the VDD to vary as a sinusoidal waveform and is calculated using equation (13).

Figure (10&11) The Negative Power Supply Rejection Ratio ($PSRR^-$) is measure by setting the V_{ss} to vary as a sinusoidal waveform and is calculated using equation (14).

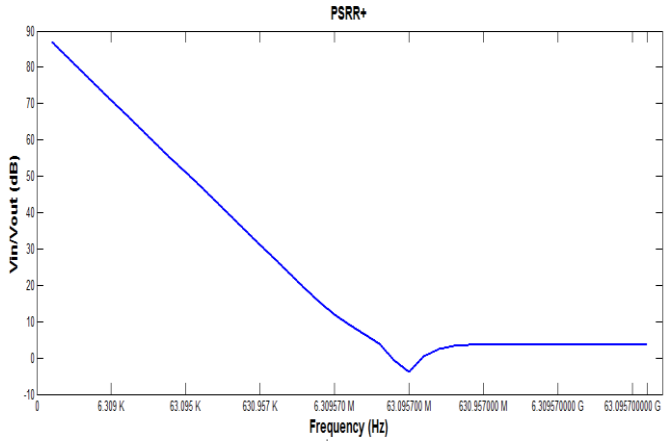


Figure (8) $PSRR^+$ versus frequency

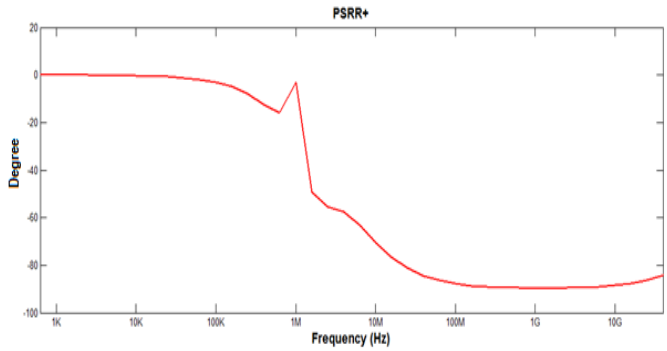


Figure (9) $PSRR^+$ phase response frequency

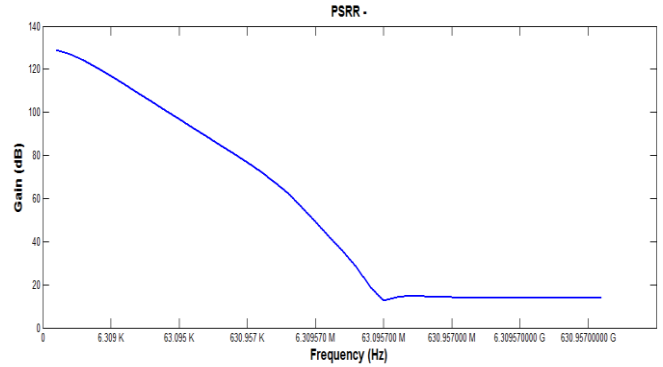


Figure (10) PSRR$^-$ versus frequency

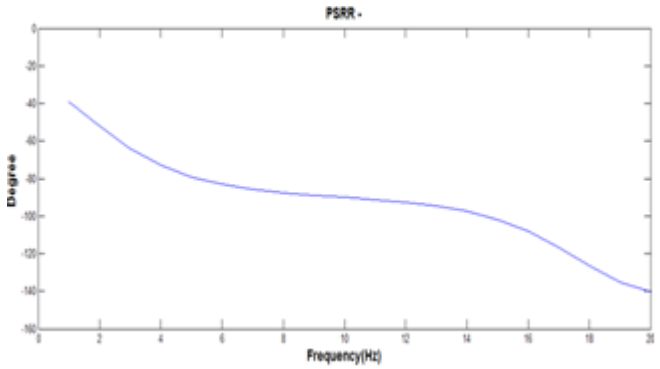


Figure (11) PSRR$^-$ phase response frequency

From the simulation and the graph obtained, the PSRR$^+$ is reducing with increase of the frequency of Vin at supply and unity gain is 63MHz. From Figure (10&11) the graph obtain the PSRR$^-$ and from curve can be estimate the unity gain GB=63.09MHz.

Table (3) Op-Amp Characteristic Comparison

Parameter	SPECIFICATIONS	Calculated results	Simulation results
A_v	85 dB >	94.7 dB	98.4dB
GB	20MHz >	20 MHz	37.3 MHz
Output Voltage Swing	2.1V >	2.4 V	2.6V
Slew Rate	9 V / µs	8 V / µs	14 V / µs
P_D	< 1 mW	0.73mW	0.222 mW
Input Common Mode Range	1.7V >	1.869V	2.79 V
Phase Margin	55^0 >	55^0	60^o
Gain margin	27 dB >	28dB	30dB

VI. CONCLUSION

This paper presented the two-stage Op-Amps employing compensation capacitor using CMOS technology and analyzed its behavior for various aspect ratios. Design technique for this Operation Amplifier, its calculations and computer-aided simulation results are given in details. The results show that the designed amplifier has successfully satisfied all the specifications given in advance. Here the gain has been increased by employing thin and long transistors into the design at output stage and wide transistors in input stage. These two techniques are able to increase the gain up to a great extent by increasing the output resistance and input trans-conductance respectively. A careful analysis of circuit and deep insight into the circuit topologies and device operations leads to good implementation and desired results. As summaries **to** the simulation results show that as following:

- ❖ Op-Amp performed to inside specs for all the predefined parameters.
- ❖ The utilization of the standard CMOS Op-Amp topology had the capacity meet all the sought details.
- ❖ The standard topology CMOS enhancer is the expansive increase it can attain to. The two addition stages acquire the extensive single increase.
- ❖ The open circle addition of the Op-Amp was measure to view the reproduction consequence of T-spice.
  The large number rate of the standard CMOS operational intensifier in this outline was influence by two separate parameters. Both the stage edge and the yield channel current.

a. Slew rate of the intensifier will modify the settling time.
b. The slew rate of the standard Op-Amp is sufficient for accomplishing the determination of settling time in this configuration.
c. In this paper the large number rate was 14 V/us. The huge number rate could have been increment, yet it was constrained because of the measure of current that was permitted by the force dispersal spec.

- ❖ PSRR is a measure of the influence of power supply ripple on the Op-Amp is output voltage. It can be calculate by putting the Op-Amp in the unity-gain configuration with the input shorted.
- ❖ The Miller compensation capacitor allows the power supply ripple at the output to be Large.
- ❖ The two-stage Op-Amp will never have good PSRR unless some modifications are madding.

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