Empirical Model Based Variability Analysis of Terminal Currents of MOSFET of a 65nm SRAM Cell in Process-Voltage-Temperature (PVT) Space

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Abstract*—Three dimension (3D) process/device simulation and optimization of MOS transistor of 65nm SRAM cell is done using implant 'dose matching' technique saving optimization time and computational resources. For this optimized transistor, source/drain (s/d) junction leakage (to substrate) current I_b, drain current I_d, and gate leakage current I_g are empirically modeled in terms of five "process-voltage-temperature (PVT) parameters such as gate length L_g, device operating temperature 'tempr', substrate bias V_b, drain bias V_d, and gate bias V_g using standard 3-level Design of Experiment technique over the entire bias range from 0V to 1.2V, in two steps (DoE). The second order empirical models for the responses: I_b, I_d, and I_g are used to estimate their variability in terms of variability of the PVT parameters. The 3σ variability of electrical variables: V_b, V_d, and Vg are seen highly significant compared to the 3σ variability in nonelectrical variables: L_g and tempr. Among the 3 bias voltages, V_g ranks first with a contribution of 44.78% on I_d, 46% on I_b, and 22.94% on I_g; V_d ranks 2nd, with a contribution of 39.76% on I_d, 44.34% on I_b, and 23% on I_g; and V_b rank 3rd with a contribution of 10% on I_d, 4.3% on I_b, and 23.2% on I_g. Among the nonelectrical variables, tempr (over 270-330°K range about mean 300°K) contributes: 1.97% on I_d, 2.8% on I_b, and 16.41% on I_g; the contribution of L_g (over 58.5-71.5nm range about mean 65nm) is: 3.43% on I_d, 2.54% on I_b, and 14.43% on I_g. These contributions are in the vicinity of 'threshold', 'subthreshold' and 'linear' region. A similar estimation is done in 'above threshold' and 'saturation' region as discussed further in this paper.

Keywords: Process sensitivity, Bias sensitivity, Temperature sensitivity, Manufacturing process modeling, Gate leakage, Substrate currents, and Statistical variability.

I. INTRODUCTION

Two issues of integrated circuit (IC) industry are increasing of yield and improving product quality, which are simultaneously achieved at lowest production cost [1]. This goal is met using advanced process control (APC) and monitoring technologies. The goal of process control is to achieve minimum variability in the process outputs which in turn depend on variability in process parameters (PPs). The APC involves highly adaptive control technique based on virtual metrology (VM). In VM based APC, the process is monitored based on process outputs calculated using process based predictive models (PMs) for accurate process conjecturing [2, 3]. Modern process control is data driven, wherein controllers are trained, using metrology data or some estimated data and process recipes [3, 4, 5]; this training is a continuous process.

In modern deep submicron (DSM) devices, random discrete dopants (RDD), is a dominant source of statistical variability, due to the discrete nature of charge. Apart from RDD variability, fluctuations in poly line edge roughness, poly-Si granularity, oxide thickness, interface trapped charges, etc., will also contribute to (intrinsic) variability [6]. The total variability is the combined effect of process variability and intrinsic variability. The total variability increases with miniaturization of MOSFET devices [7].

In this paper, PMs are experimentally derived for 3 terminal currents such as s/d junction leakage current I_b, drain current I_d, and gate leakage current I_g of a 65nm NMOSFET of a $0.594\mu m^2$, SRAM cell [8] in terms of 5 PVT parameters such as gate length L_g, device operating temperature 'tempr', substrate bias V_b, drain bias V_d, and gate bias V_g using standard 3-level face centered central composite (FCCC) DoE. The modeling is done through 3D process/device simulation and optimization of this 65nm NMOSFET, to capture second order effects [9] accurately. These PMs are used to predict variability [10] in I_b, I_d, and I_g in terms of variability in Lg, tempr, V_b, V_d, and V_g. In deriving these PMs, novel 3D device design/optimization technique (discussed later) is followed, saving significant computation time and resources.

Section II of this paper present basic concept of modeling. Section III discusses a heuristic called 'dose matching' technique to reduce the 3D process/device simulation and optimization time. This technique is used to optimize 3D

devices' implant doses against reference 2D devices' analytical implant profiles. In section IV, second order empirical models (EMs) for 3 responses I_b, I_d, and I_g are obtained in terms of 5 PVT parameters L_g, 'tempr', V_b, V_d, and V_g. Section V discusses statistical analysis of I_b, I_d, and I_g using their EMs (acronym EM, and PM are synonymously used). In section VI, we conclude with the discussion on the results.

II. AN OVERVIEW OF MODELING METHODOLOGY

Fig. 1 gives relationship between response vector r_l in terms of PP vector x_n, $n=1, 2, \ldots k$. This relationship between vector r and x can be written as:

$$r_l = f\ (x_1, x_2, \ldots., x_k) \text{ for } l=1, 2, \ldots m. \quad (1)$$

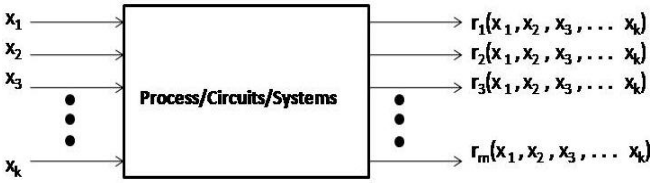


Fig. 1: General relationship between input PP '**x**' and the process output (response) variable '**r**' in a manufacturing process.

Generally f is second order polynomial relation [11, 12], given as:

$$r_l = b_0 + \sum_{i=1}^{5} b_i x_i + \sum_{i=1}^{5} b_{ii} x_i^2 + \sum_{i=1}^{5} \sum_{j=i+1}^{5} b_{ij} x_i x_j \quad (2)$$

for $l=1, 2, \ldots m$, m=3 for 3 responses I_b, I_d, and I_g; k=5 for 5 PVT parameters: L_g, tempr, V_b, V_d, and V_g, where b_0 is a constant term, b_{ii} are coefficients of quadratic term, and b_{ij} are the coefficients for cross coupled terms.

Eqn. 2 is obtained using 3-level FCCC DoE. The FCCC DoE needs 43 (2^5=32 factorial points, 2×5=10 axial points and one point at center of design, adding to 43) experiments, for 5 factors; each experiment is a 3D process/device simulation; 21 coefficients of Eqn. 2 are elements of columns of matrix B, obtained from DoE data, given as:

$$B = [X^T X]^{-1} X^T r \quad (3)$$

where $B=[B_1,B_2,B_3]$, is a 21×3 dimension coefficient matrix, $r=[r_1, r_2, r_3]$ $(=[I_b, I_d, I_g])$, is a 43×3 dimension response matrix, X is a 43×21 dimension design matrix for 3-level FCCC DoE for 5 factors; $B_1 = [X^T X]^{-1} X^T r_1$, $B_2 = [X^T X]^{-1} X^T r_2$, and $B_3 = [X^T X]^{-1} X^T r_3$ are coefficient vectors whose elements are b_0, b_i, and b_{ij} in Eqn. 2. The 3 responses I_b, I_d, and I_g are extracted from 43, 3D process/device simulations.

III. DEVICE DESIGN METHODOLOGY FOR 3D STRUCTURE

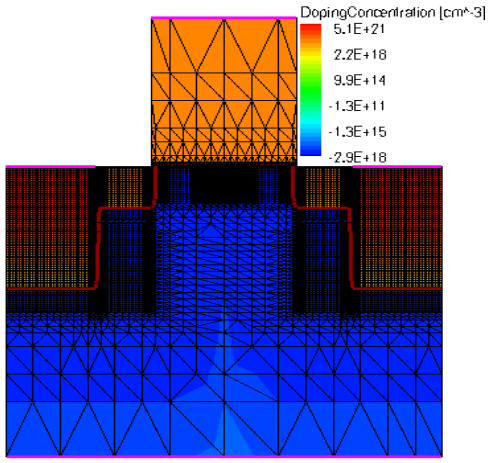
The dose matching technique [13] requires calculation of implant doses for 3D nominal device from optimized analytical implant profile for 2D reference device. In this work, construction and optimization of 2D reference device is done by a simple script to define the boundary, doping profiles, and meshing criteria, etc., using a device editor tool. This takes a few seconds to obtain meshed 2D device. This reference 2D, 65nm device is optimized to match its characteristics with ITRS [14] specification.

Approximate ratio of mesh points between 2D and 3D devices of Fig. 2(a) and (b) is 1:5 for device simulation. The time required of constructing 2D is a few seconds, whereas the time required for process emulation of 3D device is at least an hour, where the simulation time comparison is done on same machine. As the device optimization requires iteration over various implant doses/energies, annealing temperature, etc., to get the nominal 3D device, dose matching technique provides a short-cut to obtain near optimum device through a smaller number of iterations.

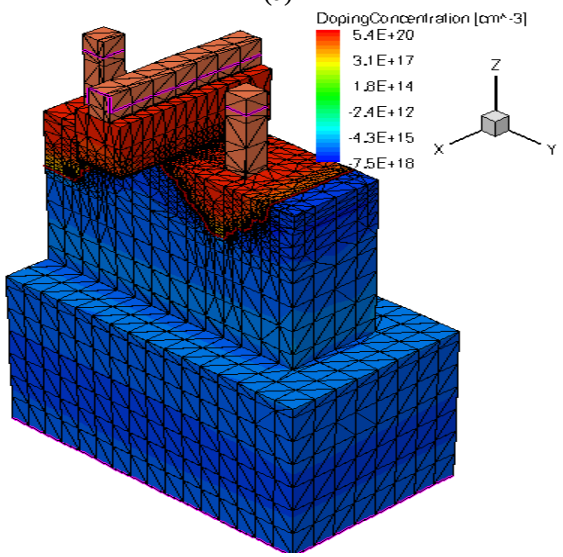
According to dose matching technique, various implant doses for a nominal 3D device (of Fig. 2(b)) are calculated using the parameters of the respective analytical implant profile of a reference 2D device (Fig. 2(a)) as [13]:

$$Dose = \frac{C_{peak} \times \sqrt{\pi} \times \sigma_y}{\sqrt{2}} \left(1 + erf\left(\frac{y_{peak}}{\sqrt{2} \times \sigma_y}\right)\right) \quad (4)$$

where C_{peak} is the peak implant concentration in cm^{-3} of Gaussian doping profile, y_{peak} is the location of C_{peak} in a direction perpendicular (along y-direction) to substrate, in cm; σ_y is the standard deviation of the Gaussian implant profile along y-direction. The parameters for the important implant doping profiles for reference 2D device along with corresponding (highlighted) implant doses for nominal 3D device are listed in Table 1.



(a)



(b)

Fig. 2: The NMOSFET device structure, (a) 2D device simulated by Sentaurus device editor and, (b) 3D device structure process emulated/simulated by Sentaurus process simulator, using layout of Fig. 3(b). The substrate contact is at bottom.

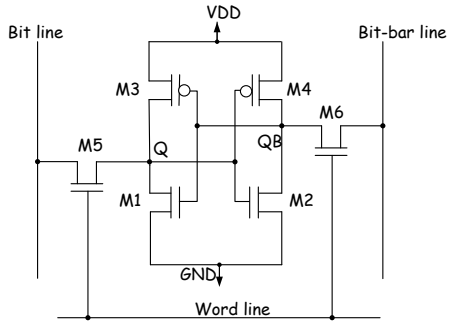
TABLE 1: 2D IMPLANT PROFILE PARAMETERS AND THE CORRESPONDING (CALCULATED) DOSES FOR 3D PROCESS SIMULATION/EMULATION.

Parameters of analytical implant profile	deep s/d	shallow s/d (or LDD)	SSRC	halo
c_{peak} (cm^{-3})	5.0×10^{21}	1.0×10^{20}	1.0×10^{18}	2.0×10^{18}
σ_{y} (cm)	1.4×10^{-6}	5.0×10^{-7}	5.0×10^{-6}	5.0×10^{-6}
y_{peak} (cm)	0	5.0×10^{-7}	1.0×10^{-6}	3.0×10^{-6}
Dose (cm^{-2})	8.8×10^{15}	1.0×10^{14}	1.3×10^{13}	2.3×10^{13}

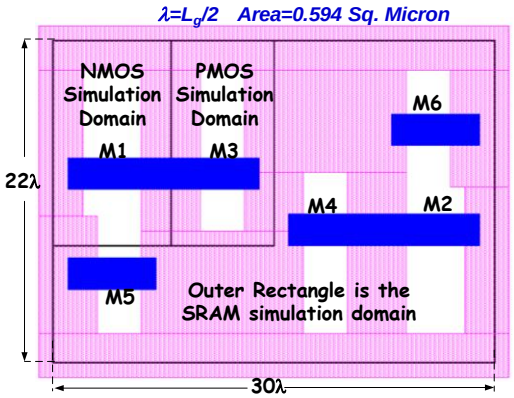
In the process emulation steps for 3D NMOS device (Fig. 2(b)) is followed from the reference [8]. The main implant parameter values give in Table 1. The main implants that characterize the device performance in DSM regime are deep s/d implant, low drain doping (LDD) implant, pocket halo implant, and super steep retrograde channel (SSRC) implant. In order to activate deep s/d, and LDD/halo implant species, 2 step annealing is performed; one at 1000°C for 15 sec to activate deep s/d implant species, and another at 1000°C for 3 sec to activate LDD/halo implant species. In order to control lateral straggle of LDD implant, a nitride spacer of 5nm thickness is deposited isotropically over poly-gate during this implant process step [15] to get s/d and gate overlap of 3D device identical to that of 2D device. Halo and SSRC implants are used to control short channel effect (SCE) [9].

Word 'process emulation' is used here, as some of the structural parameters are process emulated by Sentaurus TCAD tool's 3D geometric operation capability [13], which is computationlly economical. The process steps such as implantation, annealing, etc., are simulated, and the process steps such as etch, deposition, etc., are emulated.

Fig. 3(a) shows 6T SRAM cell circuit and Fig. 3(b), the corresponding layout with cell area=0.594μm^2. Fig. 3(b) is a simplified layout to highlight the necessary details for the mask driven process simulation/emulation. This layout encompasses the simulation domain of 3D NMOSFET (M1) device marked and labeled by a rectangle. This rectangle contains all the layers that are required to simulate/emulate the 3D structure of Fig. 2(b). The structure of Fig. 2(b) representing transistor M1 of SRAM cell is simplified by removing (200nm) trench oxide and interlayer dielectric (ILD) to save mesh points for device simulation. In Fig. 2, gate stack consists of *15Å* of SiO_2, over which a 65nm thick polysilicon, deposited. On top of polysilicon, copper contact is added. In the current view the boundaries of *15Å SiO2* gate dielectric is not noticeable, as it is extremely thin compared to other thicknesses.



(a)



(b)

Fig. 3: A 6T SRAM cell (a) circuit schematic, (b) simplified view of layout used for 3D process emulation of SRAM cell/circuit of Fig. 3(a).

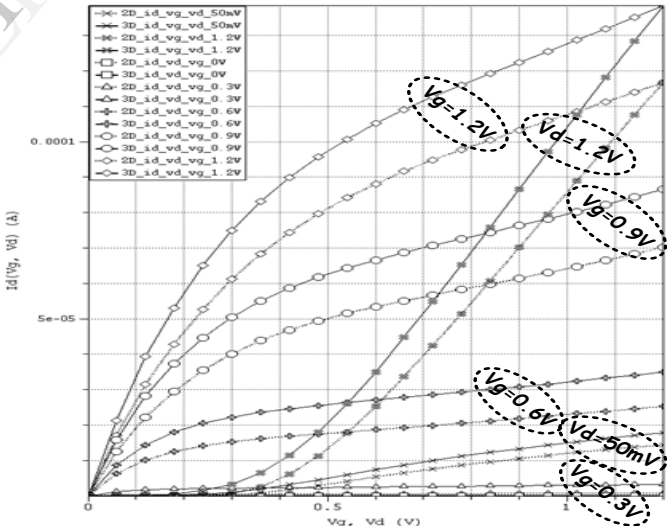


Fig. 4: The overlapped I-V curves of reference 2D device and the calibrated 3D device (M1 in Fig. 2). Important device characteristics of 2D and 3D devices match with error less than 20%. The calibrated 3D device is superior compared to the reference 2D device. All the currents are simulated with 120nm gate width.

The I_d-V_d and I_d-V_g curves of both reference 2D and nominal 3D devices of Fig. 2 are shown overlaid in Fig. 4. The reference 2D device of Fig. 2(a) is optimized for 1mA/μm drive current in saturation region of operation at 1.2V of supply (V_{dd}). The dose matched nominal 3D device is superior to reference 2D device by over 17% in I_d and 15% in G_m, in saturation region both devices' width W_g=120nm. This difference is attributed to a more realistic doping distribution

and slightly more s/d gate overlap in the case of nominal 3D device due to annealing, as compared to reference 2D device.

In Table 2 important device parameters extracted for devices of Fig. 2 are tabulated for comparison in both linear and saturation region. The extracted threshold voltage is the constant current V_t=V_g at I_d=40nA×(W_g/L_g), with W_g=120nm and L_g=65nm. The notation in Table 2 is as follows: V_t is the threshold voltage, DIBL is drain induced barrier lowering, SS is the subthreshold slope, G_m is the device transconductance, I_d is the drain current. The device parameter suffixes are interpreted as follows: 'sat' is saturation region, 'lin' is linear region, 'drive' is on state (at V_g=1.2V), and 'leak' is the leakage (at V_g=0V). For e.g. '$I_{dsatdrive}$' is the on state saturation region drain current, $I_{dsatleak}$ is the leakage current in the saturation region, etc. The linear and saturation region curves are simulated at V_{dd}=50mV and 1.2V respectively. During the device simulation of the 2D and 3D device structures, various physical models to account for second order effects in 65nm devices are used. Models to account for hot carriers, channel mobility degradation, tunneling through gate and junctions, channel carrier quantization, lattice temperature effect, etc., are used. Donor/acceptor trap density of 5×10^{10}/cm^2, at Si/SiO2 interface is used during device simulation.

TABLE 2: COMPARISON OF REFERENCE 2D AND NOMINAL 3D 65nm NMOSFET DEVICE PERFORMANCE IN LINEAR AND SATURATION REGION, WITH EQUAL DEVICE WIDTHS (=120nm).

Device Parameters	2D Structure	3D Structure
V_{tsat} (V)	0.2	0.09
V_{tlin} (V)	0.25	0.13
DIBL (mV/V)	43.19	35.01
SS_{sat} (mV/dec.)	88.65	84.81
SS_{lin} (mV/dec.)	77.72	70.52
G_{msat} (mS/120nm)	158.93	177.98
G_{mlin} (mS/120nm)	21.21	24.38
$I_{dsatdrive}$ (mA/120nm)	0.12	0.14
$I_{dsatleak}$ (nA/120nm)	10.76	5.27
$I_{dlindrive}$ (mA/120nm)	0.01	0.02
$I_{dlinleak}$ (nA/120nm)	0.04	1.34

IV. MODELING OF DEVICE TERMINAL CURRENTS

To empirically model the 3 terminal currents I_b, I_d, and I_g of nominal 3D NMOSFET device (Fig. 2(b)), standard FCCC DoE for 5 factors (PPs) is used, which requires 43 process/device simulations (section II). Three responses: I_b, I_d, and I_g are measured for all the 43 process/device simulations and tabulated in a spreadsheet.

As MOSFET devices are highly nonlinear over complete bias range (from 0V to 1.2V) over the 3 terminals: substrate, drain and gate, (at source voltage V_s=0V), 2 models for each response variables I_b, I_d, and I_g are fitted using FCCC DoE data, twice corresponding to 2 regions defined in Table 3.

TABLE 3: 3-LEVELS FOR FCCC DoE OVER 2 BIAS RANGES TO CAPTURE HIGH NONLINEARITY.

In the vicinity of threshold/subthreshold and linear region: **Region-1**			
	-10% (= -3σ)	Nominal	+10%(= +3σ)
L_g (μm)	0.0585	0.065	0.0715
tempr (^{o}K)	270	300	330
V_b (V)	0	0.15	0.3
V_d (V)	0	0.15	0.3
Vg (V)	0	0.15	0.3
Above threshold and in saturation region: **Region-2**			
L_g (μm)	0.0585	0.065	0.0715
tempr (^{o}K)	270	300	330
V_b (V)	0.3	0.75	1.2
V_d (V)	0.3	0.75	1.2
Vg (V)	0.3	0.75	1.2

The DoE data for 3 responses over Region-1 and Region-2 (Table 3) have been used to fit regression models in terms of 5 PVT parameters using the technique discussed in section II, earlier. For illustration the EM for the drain current I_d in Region-1, is given in Eqn. 5 below:

$$I_d = 1.78\times10^{-7} + (-2.60\times10^{-8})\times(L_g-0.065)/0.0065 + (1.36\times10^{-8})\times(tempr-300)/30 + (-7.61\times10^{-8})\times(V_b-0.15)/0.15 + (3.01\times10^{-7})\times(V_d-0.15)/0.15 + (3.39\times10^{-7})\times(V_g-0.15)/0.15 + (-1.25\times10^{-7})\times((L_g-0.065)/0.0065)\times((L_g-0.065)/0.0065) + (7.36\times10^{-10})\times((L_g-0.065)/0.0065)\times((tempr-300)/30) + (3.37\times10^{-9})\times((L_g-0.065)/0.0065)\times((V_b-0.15)/0.15) + (-2.73\times10^{-8})\times((L_g-0.065)/0.0065)\times((V_d-0.15)/0.15) + (-2.72\times10\text{-}08)\times((L_g-0.065)/0.0065)\times((V_g-0.15)/0.15) + (-7.46\times10^{-8})\times((tempr-300)/30)\times((tempr-300)/30) + (-8.52\times10^{-9})\times((tempr-300)/30)\times((V_b-0.15)/0.15) + (1.30\times10^{-8})\times((tempr-300)/30)\times((V_d-0.15)/0.15) + (1.27\times10^{-8})\times((tempr-300)/30)\times((V_g-0.15)/0.15) + (-6.69\times10^{-8})\times((V_b-0.15)/0.15)\times((V_b-0.15)/0.15) + (-7.81\times10^{-8})\times((V_b-0.15)/0.15)\times((V_d-0.15)/0.15) + (-7.79\times10^{-8})\times((V_b-0.15)/0.15)\times((V_g-0.15)/0.15) + (-1.25\times10^{-7})\times((V_d-0.15)/0.15)\times((V_d-0.15)/0.15) + (3.16\times10^{-7})\times((V_d-0.15)/0.15)\times((V_g-0.15)/0.15) + (5.30\times10^{-7})\times((V_g-0.15)/0.15)\times((V_g-0.15)/0.15) \quad (5)$$

The model of Eqn. 5 is having 1-constant term, 5-linear terms, 5-pure quadratic terms, and 10-two factor interaction terms, adding to a total of 21 terms. Similar models were obtained for I_b, and I_g over both the regions: Region-1 and Region-2, and analyzed for statistical inferences, presented in next section.

V. OBSERVATIONS AND ANALYSIS

The EMs developed in Sentaurus work bench (SWB) are ported to Sentaurus' 'PCM studio framework' (PCMF). The PCMF provides a graphical user interface (GUI) for an interactive analysis and optimization of various responses.

In order to understand impact of 5 PVT parameters: L_g, tempr, V_b, V_d, and V_g on 3 responses: I_b, I_d, and I_g, contour plot are generated in 2 PVT spaces: Region-1, and Region-2 by superimposing the contours of 3 responses. Three sets of

contours, corresponding to I_b, I_d, and I_g, overlaid provide a deep insight into simultaneous optimization of the 3 responses, interactively in PCMFs' GUI as shown in Fig. 5. Three isolines form a set of contours corresponding to a given response. These 3 isolines demarcate light colored, white colored and dark colored regions (Fig. 5). The light color represents the values of response less than selection range. The dark color represents the values of response higher than the selection range, and white color represents the value of the response, within the selection range. Different colors are used to distinguish different responses.

The PPs' influence on the 3 responses: I_b, I_d, and I_g in Region-1 and Region-2 of the PVT space is mapped on an X-Y plane as shown in Fig. 5. In this figure quantities plotted on X and Y axes are the tempr and V_d, respectively. The white region in the tempr-V_d plane is the intersection area of selection ranges for the 3 responses. There are two ranges, first: each variable in an EM will have an allowable ±3σ (i.e., ±10%) range and second: a 'selection range (SR). The SR must lie within ±3σ range for any PVT PP. The SR of a response depends on whether it has any specified target value, for e.g. V_t of the device. Responses may also need to be maximized, for e.g. drain current; some responses may need to be minimized, for e.g. leakage.

The common (white) SR contains simultaneously optimized (contour or isoline) values for the 3 responses in the tempr-V_d plane. In Fig. 5, the choice of values of remaining 3 parameters (L_g, V_b, and V_g) has to be done carefully such that common SR (CSR) corresponding to simultaneously optimized responses remains within tempr-V_d plane. The ranges of the setting for these 3 parameters such that the CSR lies within tempr-V_d plane constitute the process window [13]. Fig. 5(a) and (b) are the contour plots (response surfaces) corresponding to the EMs of 3 responses: I_b, I_d, and I_g in Region-1; and Fig. 5(c) and (d) are the contour plots corresponding to the EMs of same 3 responses in Region-2. In Fig. 5(a) setting V_b to zero causes partly visible CSR in tempr-V_d plane. Among 3 isolines in the CSR the red is the expected I_d, green is the expected I_b, and the blue is the expected Ig.

In Fig. 5(b) setting V_b to 0.15V results in larger CSR visible in tempr-V_d plane, with the locations of red, green and blue contours being changed. The new location of red, green and blue isolines may be desired or not have to be decided from the process stability perspective.

Fig. 5(c) and (d) are the contour plots corresponding to the EMs of 3 responses: I_b, I_d, and I_g in Region-2. In Fig. 5(c) setting V_b to 0.3V causes a small CSR visible in tempr-V_d plane. Again, among the 3 isolines visible, the red is the expected I_d, green is the expected I_b, and the blue is the expected Ig. In Fig. 5(d) setting V_b to 0.6V results in larger CSR visible in tempr-V_d plane, with the location of the red, green and blue contours being changed. The new location of red, green and blue isolines is the desired one or not, has to be decided from the process stability perspective.

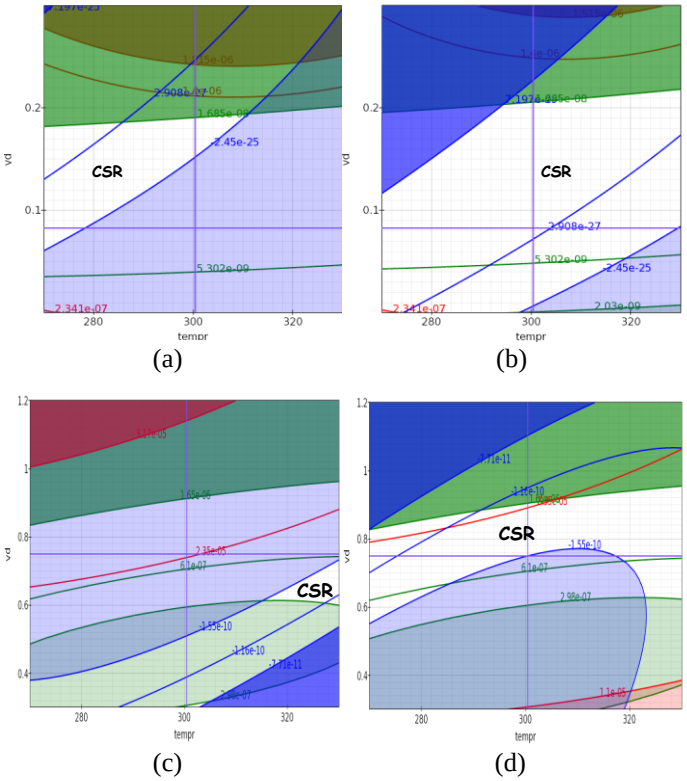
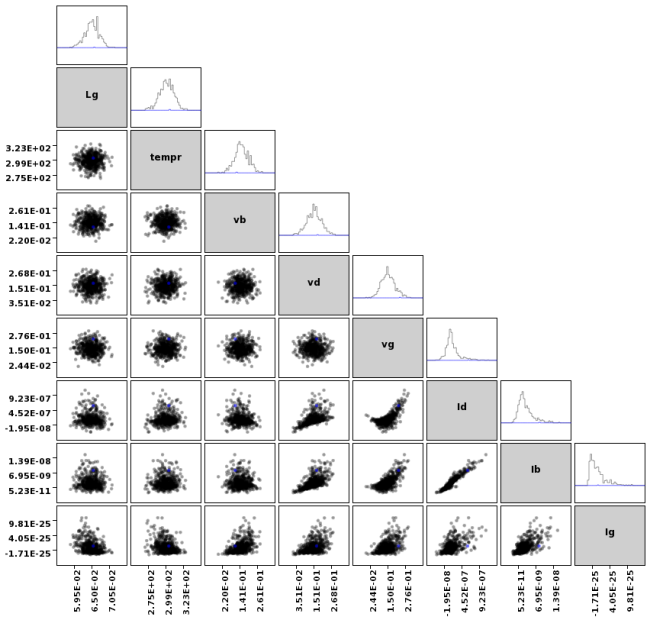


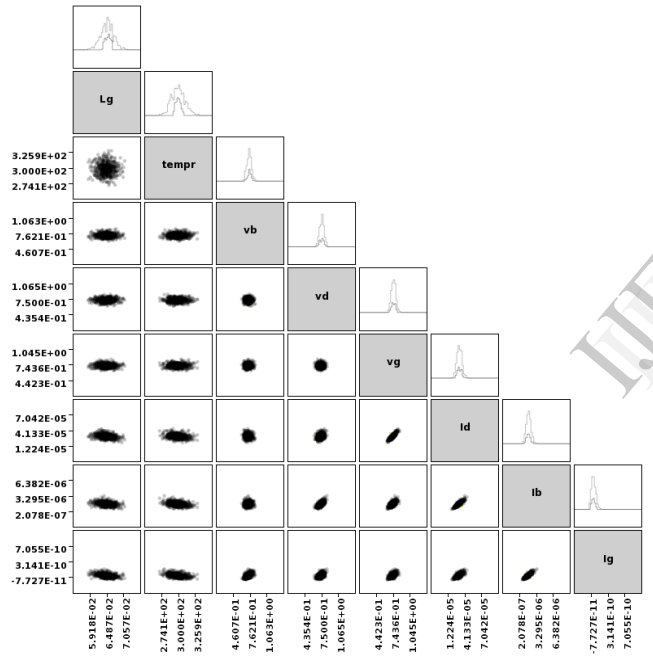
Fig. 5: The contour plot representation of response surfaces for I_b, I_d, and I_g in tempr and V_d space for the 2 sets of EMs (a) and (b) in Region-1, and (c) and (d) in Region-2.

EMs for I_b, I_d, and I_g in Region-1 and Region-2 provides a basis for the pair-plots of Fig. 6(a) and (b), respectively presented in half matrix form. Pair-plots are a set of scatter plots [10] generated, taken two PPs or response variables at a time using their random values (RVs), in specific order. An individual plot in the array of pair-plot is a scatter plot between 2 variables (with their RVs on X-Y axes) that appear in the EM. The variables that appear in the EMs, both in Region-1 and Region-2 are 5 PVT parameters and 3 response variables. A total of 28 scatter plots are arranged in half matrix form in Fig 6(a) and (b) corresponding to Region-1 and Region-2, respectively. The matrix diagonal is replaced by (5 PVT) PPs and 3 responses acronyms.

It is clear from Fig. 6, that the scatter plot for the pair-wise consideration of 5 PVT parameters has no pattern, indicating that they are uncorrelated. In the scatter plots among 5 PVT parameters and 3 responses, there is sufficient evidence of strong correlation. The correlation is significant for some pairs of 5 PVT parameter-response pairs. For e.g., in Fig 6(a), there is strong correlation between V_g and I_d, and V_d and I_d as expected in Region-1. Also, in Fig. 6(b), there is strong correlation between V_g and I_d, but V_d and I_d shows significantly less correlation compared Fig. 6(a) as expected in Region-2 (i.e., saturation region). In each scatter plots, the values on the x-y axes are the mean±3σ ranges. The values of 5 PVT parameters are the normal random numbers resulting in corresponding normal values for the 3 responses.



(a)



(b)

Fig. 6: Pair plots from EMs of 5 PVT parameters and 3 terminal currents of NMOSFET depicted as half -matrix. (a) in Region-1 (500 random experiments) and (b) in Region-2 (1000 random experiments).

Looking at responses, there is a strong correlation between I_d and I_b both in Region-1 and Region-2. Even though there is some haze (due to numerical noise, model insufficiency, etc.) some plots in last 3 rows of Fig. 6(a) and (b), one can see considerable dependence/correlation on PVT parameters and among the responses themselves.

The percentage contribution of 5 PVT parameters to I_b, I_d, and I_g, derived from the Pareto chart for 3 responses is presented in Table 4 in both Region-1 and Region-2. The overall contribution of V_g on the 3 response variables is highest, both in Region-1 and region-2. The contribution of drain bias V_d to I_d and I_g is almost same as V_g in Region-1; the significant contribution of V_d to I_d continues in Region-2, which is the manifestation of DIBL and channel length modulation (CLM) effect. Among non-electrical parameters, the response I_g has stronger dependence on L_g and tempr. As the gate current is due to hot carrier injection and various tunneling effects, I_g is likely to increase with temperature. Also, I_g being the total gate current, it is total gate area dependant, which in turn makes it L_g dependent.

The simulation study of this research highlights significant gate and substrate currents due to severe SCE, which is effectively captured by 3D process/device simulations. Further, this fact is corroborated by models of I_b, I_d, and I_g. The process/device simulation, modeling of I_b, I_d, and I_g, and statistical analysis of the models is done using Synopsys' Sentaurus TCAD and PCM studio.

The method of process/device simulation, modeling and statistical analysis of this paper is very useful in the present context of IC manufacturing. Any Information based on manufacturing process modeling of performance parameters of interest is a valuable input to process control to minimize process variability, which in turn achieves good performance of ICs and result in high yield.

TABLE 4: THE PERCENTAGE CONTRIBUTION OF 5 PVT PARAMETERS OBTAINED FROM PARETO CHART FOR THE 3 RESPONSES.

Parameters	I_b	I_d	I_g
Region-1			
L_g	3.43%	2.54%	14.43%
tempr	1.97%	2.80%	16.41%
V_b	10.05%	4.30%	23.15%
V_d	39.76%	44.34%	23.08%
V_g	44.78%	46.03%	22.94%
Region-2			
L_g	5.01%	4.90%	5.53%
tempr	6.16%	4.62%	6.91%
V_b	2.47%	7.72%	30.02%
V_d	43.21%	19.04%	26.78%
V_g	43.15%	63.72%	30.76%

VI. CONCLUSIONS

In view of accurate modeling of the 3 terminal currents of NMOS transistor of a 65nm SRAM cell in terms of process, voltage and temperature (PVT) parameters 3D device structure is process/device simulated and optimized using dose matching technique. The dose matching technique involves mapping optimized 2D devices' analytical implant profiles to 3D devices' implant doses. The dose matching technique has saved computation time and resources by than an order. Standard 3-level FCCC DoE based second order EMs for the 3 responses I_b, I_d, and I_g in terms of 5 PVT parameters L_g, tempr, V_b, V_d, and Vg, is obtained using standard techniques. The 3-levels for 5 PVT parameters are nominal value, and ±10% (±3σ) of nominal values. Detailed statistical analysis of the EMs has been done through contour plots, pair-plots, and Pareto charts. Correlations among 5 PVT parameters and 3 response currents are predicted to underscore second order effects in 65nm regime SRAM technology. The phenomenon of process drift is analyzed using contour plots of EMs for I_b,

I_d, and I_g. A quantitative assessment of relative impact of 5 PVT parameters on I_b, I_d, and I_g are performed. The method of process/device simulation, modeling and statistical analysis of this paper is very useful in the present context of IC manufacturing. Any Information based on manufacturing process modeling of performance parameters of interest is a valuable input to process control to minimize process variability, which in turn achieves good performance of ICs and lead to high process yield.

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