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Electrostatic Field Effects in Hardware Module Interface in Automotive Application

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Abstract – *Electrostatic Discharge (ESD) causes electrostatic field effect, charge injection effects, and effects due to fields generated by ESD currents. Proper system cable design can help combat and reduce the failure effects. Effects will be classified in to two categories, due to radiated noise & due to conducted noise. Radiated noise included the effects of both electrostatic filed electronic and magnetic fields generated by the discharge current. Conducted noise includes direct charge injection and current inducted by electronic and magnetic fields. We can't eliminate these effects in the system, but we can minimize the risk by design and configuration.*

Index Item – EMC, ESD effects, Module Interface, Interface cables

I. Introduction

Today many automotive applications comes with lot of features including, car entertainment, automotive networking, automotive immobilizers and keyless entry & start and etc. The inputs and outputs of all these modules will be connected via cables. Many of those are not different from non-automotive, especially with respect to ESD. Once installed into the system, the components inside the modules are not threatened anymore. In the automotive world, product pins directly interfacing with the outside world (battery monitors, airbag sensors) may see another type of ESD threat. This is the so-called system level ESD. At 20KV an arc can jump 2cm through air. And cables between modules can easily be efficient antennas at a frequency of few hertz to few megahertz.

II. Module Interfaces

The main function of the interface circuit is to provide a data link between different systems or subsystems. There are a number of interface standards that cover different data link and signal specifications for transmitting through a cable, from several inches within the same system block to several meters between systems within the same vehicle.

Example, In comparison with DAC, one the major specifics of advanced interface products is the high speed of the data transmission. From an ESD specific point of view, a typical requirement may include on-chip system-level pins. Typically, the cable discharge event protection level is specified. Another peculiarity of the interface circuit is the presence of high common-mode voltages in the input signal.

Just like RF-amplifiers, the high-speed input interface pins require broadband characteristics. This eliminates the possibility of application of a number of narrow band, LNA-specific input solutions that rely on ESD pulse bandwidth filtering. Over recent years, interface applications are heading toward few Gbps links. Achieving these goals requires not only increase of speed but also corresponding reduction in power consumption and noise.

III.Representation

Interface parameters are related to the power moving in the network and in and out of the integrated circuits. The interface characteristics are often described in terms of the equivalent S-parameters.

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The *transducer gain* parameter G_T is the ratio of the power delivered by a network to a load (P_{dl}) to the power available from the source (P_{as}). Transducer gain is a function of the source and load reflection coefficients and the networks-parameters. This can be expressed as shown in the following formula:

$$G_T = \frac{P_{dl}}{P_{as}}$$

The maximum power-transfer theorem says that to transfer the maximum amount of power from a source to a load, the load impedance should match the source impedance. In the basic circuit, a source may be dc or ac, and its internal resistance (R_I) or generator output impedance (Z_S) drives a load resistance (R_L) or impedance (Z_L).

At matching load and source impedance,

$$Z_L = Z_S = 50\ \Omega/100\ \Omega \text{ and } G_T = |S_{21}|$$

The *operating power gain* parameter G_P represents the ratio of the power delivered to the load to the power delivered to the network.

The *operating power gain* parameter G_P represents the ratio of the power delivered to the load to the power delivered to the network. The power delivered to the network is dependent on the S_{11} parameter. In this case, $G_P > G_T$ and G_T is closer to G_P with better input matching.

The *available power gain* G_A is the ratio of the power available at the output of a network (Pao) to the power available from the source to the source (Pas). This can be expressed as shown in the following formula:

$$G_A = \frac{P_{ao}}{P_{as}}$$

Since the power available from the network is dependent on S_{22}, $G_A > G_T$, while G_T approaches G_A with better load matching. A functional block diagram an interface application is presented in Fig.1.

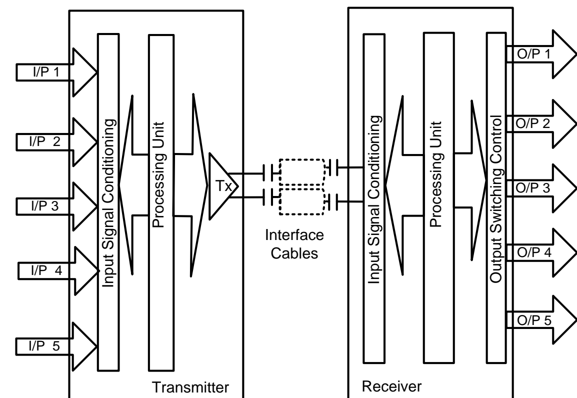

Fig. 1 Function block diagram, for example, module interface solution

In terms of the ESD protection challenge, the interface application requires the CDE protection for the selected pins directly interfacing with cable. To address the design specific, the next section presents the CDE test methodology.

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IV. ESD Protection for Cable Interface

External cabling is a greater problem. Due to their direct illumination during ESD, cables become unintentional, but efficient antennas, converting the radiated field into induced voltages and currents. Fig.2 shows a summary of what happens to external cables during an ESD event. To combat the effects of this ESD coupling, two approaches are available, which depend on the nature of the external cables and of the equipment enclosure.

If the external cables are shielded (maybe for other EMC reasons, and probably not just against ESD), they will perform efficiently against ESD, provided some precautions are taken, the same as those used for good RF shielding results.

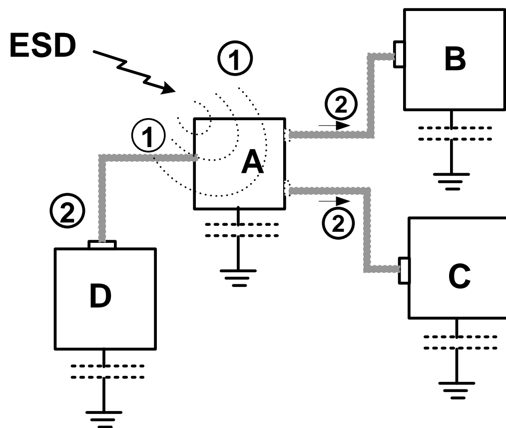

Fig.2 External cables to ESD coupling

If the system external cables are not normally planned to be shielded, and the equipment box is eventually plastic, there is no sense in shielding them for meeting an ESD immunity level. In this case, the ESD-induced pulses could penetrate the equipment by the external cable conductors, and they must be filtered, or eventually clamped, at the cable entry port.

V. Magnetic Field Coupling

Figure 3 shows a simplified model of this phenomenon, based on the discharge current only. A first thing to point out is that the dimensions of the ESD generating circuit are large compared to its distance to the receiving circuit. Therefore, it cannot be treated as a punctual source. Simple solutions of Maxwell's equation for small electric or magnetic doublets with their resulting $(1/d)^2$ and $(1/d)^3$ field-to-distance dependency cannot be straightforwardly applied.

A rigorous approach would be to apply the method of moments to the current path, broken down in small filaments. The much simpler model shown assimilates the ESD current path to a long radiating wire for which the resulting magnetic field is easily calculated from the Biot and Savart law. The ESD drain path to ground being long versus the distance of observation the magnetic field is given by:

$$H(A/m) = I/(2\pi d) \text{ ---------- Eq1}$$

Where

I = ESD current in amperes
d = distance from ESD path to victim circuit

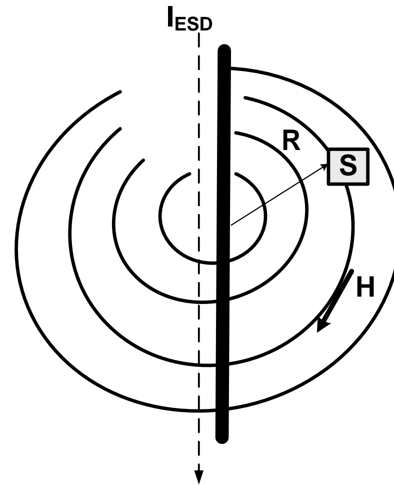

Fig. 3 ESD coupling by radiation.

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Simplified model: the H field is modeled from an infinite straight wire, carrying I_{ESD}

Ampere's law: $H = I / 2\pi R$

Example: I_{ESD} = 15 A (from a 4 kV simulated ESD)

Distance R	H Peak	Voltage Induced in 1 cm^2 loop	
		Rise time 1ns	Rise time 10ns
3 cm	80 A/m	10V	1V
10 cm	24 A/m	3V	0.3V
30 cm	8 A/m	1V	0.1V

If the area of the circuit illuminated by the ESD field is known, a derivation of the field over the rise time gives an approximation of the open-loop voltage induced, generally sufficient for a quick prediction.

$$V_i = -\frac{d\phi}{dt} = \frac{AdB}{dt}$$ -------- Eq2

Where

Vi = Induced voltage in V
A = Victim circuit area in m^2
B = Induction in teslas, with 1 tesla = 10^4 gauss = 80×10^4 A/m

Rearranging Eqs (1) and (2) and using more convenient units, we end up with:

$$V_i = 2\left(\frac{\Delta IA}{\Delta td}\right)$$ -------- Eq3

Where

ΔI = Change in ESD current in A
A = Victim circuit loop area in cm^2
Δt = Rise time of the ESD current in ns
d = Distance from ESD path to victim circuit in cm

Fig.3 gives the results in voltages induced per centimeter squared of victim area, for three distances from the ESD path, assuming rise times of:

• 1 ns typical of the fast precursor peak with a hand/tool discharge ≤ 8 kV

• 10 ns more typical of simple hand discharge or air discharge above 8 kV

VI. Summary

In this paper, ESD protection challenges and solutions have been discussed. When a unit is designed (and/or hardened) to meet a given ESD severity criteria, it must be checked, during design and testing face. The level that has been achieved for the maximum system configuration (all possible cables, features, and peripherals installed) is still met for the minimum size or, eventually, a stand-alone configuration. Immunity does not rely exclusively on a drastic treatment of the I/O cables and interfaces. A good ESD performance built upon an intensive use of well-shielded cables and capacitive decoupling of I/O ports may deteriorate when the unit is not equipped with all these cables, or some unit(s) at the other end presents higher common mode impedance to ground than what was used as a test vehicle. To reduce the time-to-market for such R&D work, physical device and mixed-mode simulations are critically important tools.

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