Electronics Properties of Si Nanocrystals Mixed-LaF_3 layer produced by a novel chemical bath deposition technique

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Abstract

Electronic properties of Si-nanocrystal (Si-NCs) mixed in Lanthanum Fluoride (LaF_3) layer fabricated using a novel chemical bath deposition technique has been reported here. The Si-NCs was fabricated by sonicating porous silicon. Thin layer LaF_3 containing Si-nanocrystals was deposited by a novel chemical method. Scanning electron microscopy (SEM) confirmed the presence of Si-NCs and energy-dispersive X-ray (EDX) analysis of the deposited layer revealed a non-stoichiometric LaF_3 layer embedding Si-NCs. Electronic properties of the deposited layer were investigated using the capacitance-voltage (C-V) and conductance–voltage (G–V) measurement of MIS device fabricated in [Ag/LaF_3/Si-NCs/Si/Ag] structure. Capacitance-voltage (C-V) study revealed that resonant tunneling of electron and charge storage was there. The effect of thermal annealing on the electronic properties was also studied. The Size uniformity of the Si-NCs can be improved by annealing.

Keywords: Silicon nanocryatals, Capacitance, Conductance, Metal-insulator-semiconductor (MIS) device, chemical bath deposition

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1. Introduction

In the last few years, metal–insulator–semiconductor (MIS) devices with semiconductor nanocrystals embedded in insulating layers have attracted in nanoscale electronic and optoelectronic devices [1-3]. Such nanoscale quantum structures are also excellent candidates for investigations of fundamental physical properties and for potential applications in next-generation memory devices [4-6]. The physical phenomenon of the constructed MIS [Ag/LaF_3/Si-NCs/Si/Ag] structures is the direct tunneling of electron through the ultra-thin insulating layers (LaF_3) into the NCs. The NCs act as charge storage centres whose charge state may be influenced by application of a DC bias voltage across the device. Therefore, the formation of the silicon nanocrystals (NCs) and the ultrathin LaF_3 layers is a key technology to ensure the operation of such charge storage elements based MIS devices. Good size uniformity for Si-NCs and high quality for ultrathin LaF_3 layer is an important feature for such MIS structures. Several studies reports the use of different high-k materials such as SiO_2 [4], Si_3N_4 [7], HfO_2 [8], ZrO_2 [9], etc. Researcher have been developed for nanocrystal formation in a dielectric matrix, such as electron beam evaporation [10], low-energy ion implantation [11-14], chemical vapor deposition [15-18], or ion beam co-sputtering [19], [20]. In this work, the use of silicon nanocrystals (Si-NCs) embedded lanthanum fluoride (LaF_3) insulating layer in MIS device fabricated for the first time by using a novel chemical bath deposition (CBD) technique. LaF_3 has been chosen as alternative candidates for gate insulator because of their large band gap, high dielectric constant, and large refractive index. Moreover, the lanthanide fluorides (LaF_3) show good characteristics without pre-formed interfacial layer, and regarded as high-k dielectrics [21]. The structural and electrical properties on a novel chemical bath deposited Si-NCs-embedded LaF_3 for MIS device have been analyzed in this paper. The focus of this work is the experimental (C–V) and conductance–voltage (G–V) characteristics of Ag/LaF3/Si-NCs/Si/Ag structures at different annealing temperatures.

2. Experimental methods

MIS device containing a layer of Si-NCs embedded in LaF_3 were fabricated on a p-type <111> single crystal silicon substrates. Device fabrication began with Ultrasonic cleaning of the substrate and formation of porous silicon (PS) & silicon nanocrystals (Si-NCs).
Porous silicon sample were prepared by standard electrochemical etching of *p-type* <111> Si wafers in a homemade double tank cell at different current densities for 30 minutes under room light illumination. Etching was done in a 2.5:1 (v/v) solution of 48% HF and absolute ethanol. Colloidal suspensions of silicon nanocrystals were prepared from as made porous silicon in hydrofluoric (HF) acid by Ultrasonic Vibration (sonication) at a frequency of 40 kHz. After the etching process, the

PS samples were immersed in hydrofluoric acid (HF) in a small plastic container and this container was immersed in water. Ultrasonic wave was applied to the water through the ultrasonic probe to vibrate the PS layer for about 60 minutes. The sonication was done at various ultrasonic powers of 12, 18 and 32 W. The sonication crumbles the top layer of the as made PS, a weakly interconnected nanostructures network into ultra-small particles and produces a luminescent and reddish, colloidal suspensions of Si-NCs.
After formation of the colloidal suspensions of silicon nanocrystals in HF, using a novel chemical bath (CBD) deposition technique, warm 0.6M-lanthanum chloride ($LaCl_3$) solution in HCL was allowed to react with the HF of the colloidal solution that contains Si-NCs. Due to high solubility of $LaCl_3$ in HCL solution, HCL was chosen as a solvent of $LaCl_3$. The solubility of $LaCl_3$ in HCl solution depends on temperature [22] and why the solution was heated at 45°C for 20 minutes before reacting with the colloidal solution. The chemical reaction was done on a Si substrate and the possible chemical reaction of the of HF in the colloidal solution, $LaCl_3$ and hydrochloric (HCl) could be,

$$HF + LaCl_3.7H_2O \longrightarrow LaF_3 + HCl + H_2O$$

The samples were annealed at 100°C 400°C for 10 min.
A schematic diagram of a completed Si:NC-MIS [Ag/LaF_3/Si-NCs/Si/Ag] device is depicted in figure 1. SEM observations were performed in a JEOL-JSM-6490LA scanning electron microscope operating at 30 kV. *C-V* and *G-V* measurements were performed by using an impedance analyzer at different frequency. Ohmic contacts were fabricated by silver (Ag) evaporation on both sides of the prepared samples.

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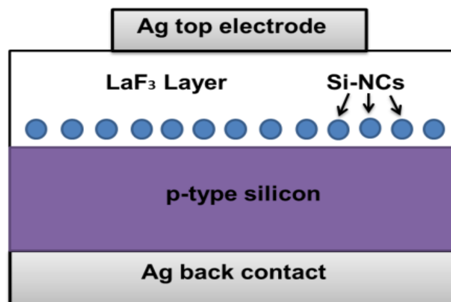


Figure 1: Schematic diagram of a fabricated Si:NC-MIS [Ag/LaF_3/Si-NCs/Si/Ag] structure.

3. Experimental results and discussion

SEM photograph as shown in figure 1 clearly depicts the presence of silicon nanoparticles. Various sizes of nanoparticles were viewed there. The smallest size was found to be of the order of 50 nm. The average size of the Si-NCs was dependent on the anodization current during the fabrication of porous silicon and sonication power.

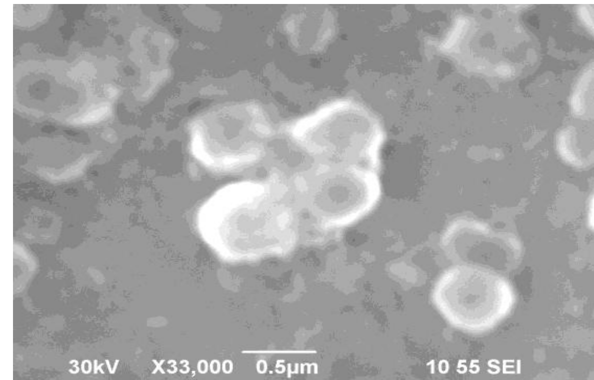


Figure 2. SEM image of silicon nanocrystals.

EDX studies were used to analyze the elemental composition of the Si-NCs embedded in lanthanum fluoride deposited Si films. As shown in figure 5, the EDX spectrum revealed small carbon in the system because carbon tape were used for contact the sample with the sample stage. The elemental composition of above mention samples are shown in Table 1.
Table 1 shows the atom and weight percentage of various elements in the LaF_3/Si-NCs/Si system which confirms the non-stoichiometric nature of LaF_3 deposited sample.

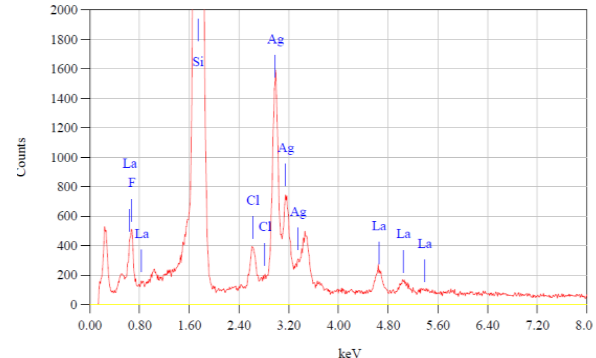
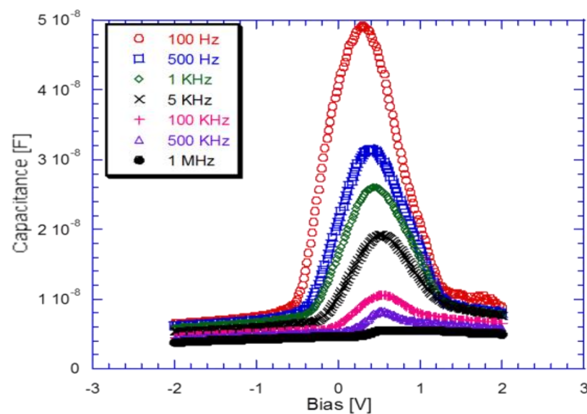


Figure 3: EDX spectrum of the LaF_3/Si-NCs/Si system.

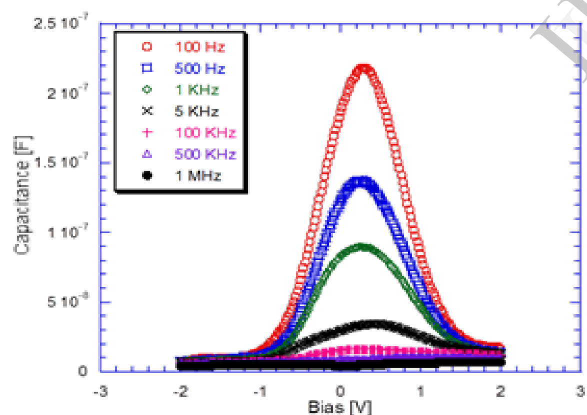
TABLE 1: ATOM PERCENTAGE OF THE WHOLE SYSTEM

Elements	Weight%	Atom%
C	10.31	10.80
F	7.29	14.25
Si	34.11	59.18
La	11.15	2.98
Ag	37.14	12.79

Figure 3 shows the Capacitance-Voltage (*C-V*) curves of the Ag /LaF_3/Si:NCs/Si/Ag configuration act as Si:NC-MIS device samples for various frequencies (from 100 Hz to 1MHz). Figure 3(a) and 3(b) shows the *C-V* characteristics of the sample annealed at 100°C or 10 min and 400°C for 10 min. Capacitance-Voltage (*C-V*) measurements were performed at room temperature using a standard *C-V* measurement setup. The measurements were obtained by sweeping the bias from -2V to +2V and back to -2V. The DC voltage was applied to the top Ag electrode with respect to the back Ag contact and superposed with various frequencies with the signal amplitude of 50mV.



(a)Annealed at 100°C



(b)Annealed at 400°C

Figure 3. The Capacitance-Voltage (*C-V*) characteristics of the annealed sample at 100°C for 10 min (a) and 400°C for 10 min (b), respectively.

From the *C-V* curves, clear capacitance peaks were observed in the inversion region at the lower frequencies, while for the reference sample (that is, the MIS structure not containing Si-NCs), no peaks were observed in the *C-V* characteristics. The capacitance peaks were attributed to carrier exchange between the semiconductor substrate and bound states quantum confinement of carriers in the Si-NCs.

The capacitance peaks indicate the results from the size fluctuation of the Si-NCs. The variations of capacitance peak with annealing temperature are shown in Figure 4. Enhanced peak was observed for higher annealing temperature (400°C) than that at a lower annealing temperature (100°C) for the same annealing time. These manifest that annealing can improve the size uniformity of the Si-NCs. At the higher temperature, the size of the Si-NCs becomes more uniform than that at the lower temperature.

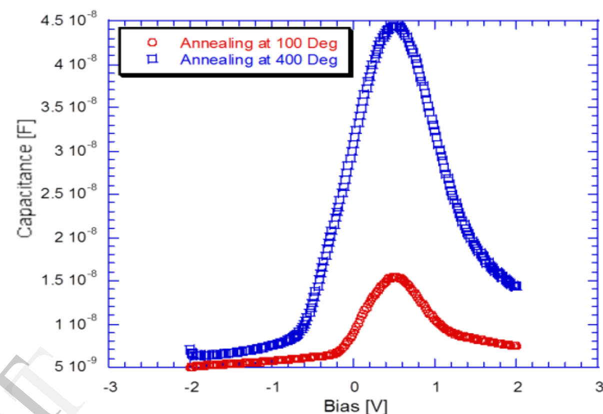


Figure 4: Variation of capacitance with annealing temperature.

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From the capacitance- frequency (*C-f*) characteristics in Figure 5, it is apparent that the capacitance value does not change with frequency when the frequency higher than 500 kHz, and the capacitance value increases with decreasing frequency when the frequency is lower than 500 kHz. These are related to the different tunneling ability of the electrons at the different frequencies. At lower frequencies, electrons have more time to tunnel into Si-NCs; while higher frequencies, electrons cannot follow ac modulation and cannot tunnel into Si-NCs.

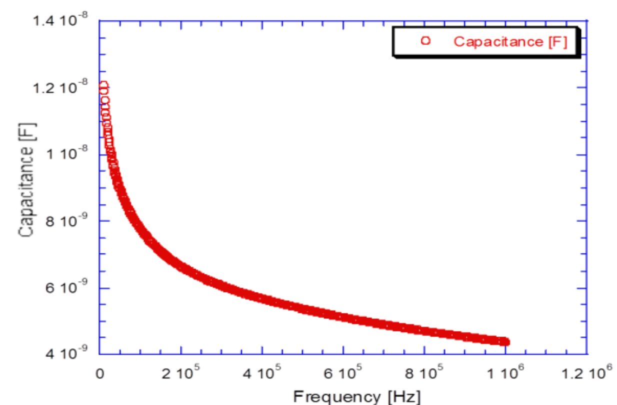
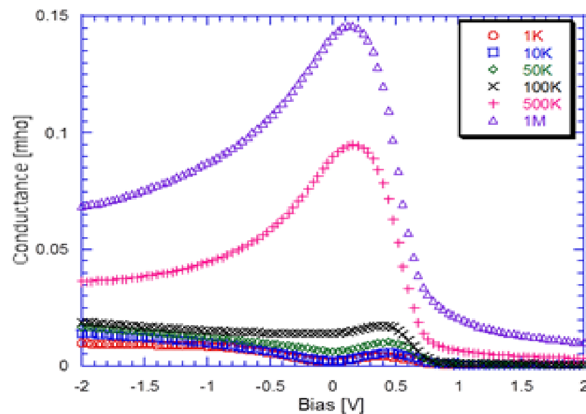
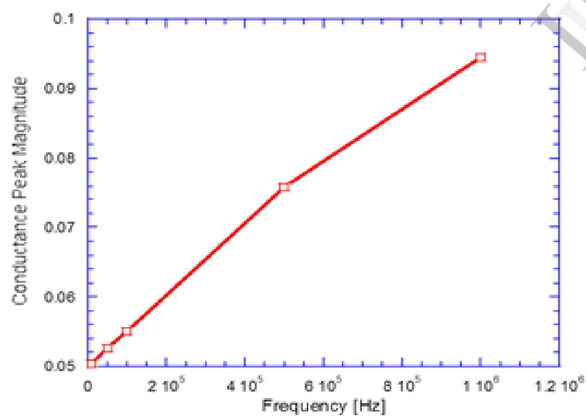


Figure 5: The capacitance-frequency characteristics for the annealed samples.

Figure 6(a) shows the conductance voltage (*G–V*) curves of the Si:NC-MIS devices, were measured at room temperature for various signal frequencies of 1 kHz, 10 kHz, 50 kHz, 100kHz, 500kHz and 1 MHz with bias voltage (Forward Scan). The voltage was applied to the top Ag electrode with respect to the back Ag contact and the bias voltage was swept from negative to positive. One can be seen in the conductance voltage (*G-V*) measurements of Figure 6 for the 100°C annealed sample, a conductance peak can be observed due to the electron charging into the Si-NCs in the region where the capacitance peak appear, as shown by curve in Figure 4(a).



(a)



(b)

Figure 6. Conductance–Voltage (G-V) characteristics for the 100°C annealed sample at different frequencies (a), and Variation of conductance peak magnitude with frequency (b)

The *G-V* peak curve reports the displacement current in the sample and thus the conductance increases, causes of electrons in the substrate tunnel through the ultrathin LaF_3 layer into the Si-NCs. It is also observed from the *G-V* characteristics that conductance peaks whose magnitude and position are highly dependent on frequency which attribute two features: (a) Increases in the small signal frequency shift the peak to less negative bias voltage; (b) the magnitude of the conductance peak increase linearly with frequency, as shown in Figure 6(b).

4. Conclusion

In summary, silicon nanocrystals embedded in a LaF_3 layer for metal-insulator-semiconductor (MIS) device have been successfully fabricated by a novel chemical bath deposition (CBD) technique. The SEM image also confirmed the presence of silicon nanocrystals and it has been obtained various sizes of the Si-NCs during sonication. From the EDX spectrum, it was observed that the deposited LaF_3 layer was non-stoichiometric. By C-V and G-V measurements, resonant tunneling of electron and charge storage was observed in silicon nanocrystals at room temperature. The size uniformity of the Si-NCs can be improved by high temperature annealing. The *C-V* curve for Ag/LaF_3/Si-NCs/Si/Ag capacitors showed an MIS behavior with capacitance peak due to the quantum-confinement effect of the silicon nanocrystals in spite of the possible existence of the ultrathin LaF_3 layer. The *G-V* curve also showed a conductance peak due to the electron charging into the Si-NCs in the region close to the capacitance peak.

It can be concluded from this present result that MIS device containing silicon nanocrystals in the LaF_3 insulating layer fabricated by a very simple CBD technique can be of enormous interest in future silicon nanoelectronic devices such as nonvolatile memory devices.

5. References

[1] L. Jiang, S. S. Li, N.-T. Yeh, J.-I. Chyi, C. E. Ross, and K. S. Jones, "$In_{0.6}$ $Ga_{0.4}$ As/GaAs quantum-dot infrared photodetector with operating temperature up to 260 K", Appl.Phys. Lett. (2003), vol. 82, pp. 1986-1988.

[2] X. Li, Y. Wu, D. Steel, D. Gammon, T. H. Stievater, D. S. Katzer, D. Park, C. Piermarocchi, and L. J. Sham, "An All-Optical Quantum Gate in a Semiconductor Quantum Dot," Science, (2003), vol. 301,pp. 809-811.

[3] N. J. Craig, J. M. Tayler, E. A. Lester, C. M. Marcus, M. P. Hanson, and A. C. Gossard, "Tunable nonlocal spin control in a coupled-quantum dot system," Science, (2004), vol. 304, pp. 565-567.

[4] S. Tiwari, F. Rana, H. Hanafi, A. Hartstein, E. F. Crabbe, and K. Chan, "A silicon nanocrystals based memory", Appl. Phys. Lett. (1996), vol. 68, pp. 1377-1379.

[5] C. D. Chen, Y. Nakamura, and J. S. Tsai, "Aluminum single-electron nonvolatile floating gate

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memory cell",Appl. Phys. Lett. (1997), vol. 71, pp. 2038-2040.

[6] S. J. Baik and K. S. Lim, "Characteristics of silicon nanocrystal floating gate memory using amorphous carbon-SiO2 tunnel barrier", Appl. Phys. Lett. (2002), vol. 81, pp. 5186-5188.

[7] Chang-Hee Cho, Baek-Hyun Kim, Tae-Wook Kim, Seong-Ju Park, Nae-Man Park and Gun-Yong Sung, "Effect of hydrogen passivation on charge storage in silicon quantum dots embedded in silicon nitride film", Appl. Phys. Lett. (2005), vol. 86, pp. 143107.

[8] V. Mikhelashvili, R. Brener, O. Kreinin, B. Meyler, J. Shneider, and G. Eisenstein,"Characteristics of metal-insulator-semiconductor capacitors based on high-*k* HfAlO dielectric films obtained by low-temperature electron-beam gun evaporation", Appl. Phys. Lett. (2004), vol. 85, pp. 5950-5952.

[9] Q. Wan, N. L. Zhang, W. L. Liu, and T. H. Wang, " Memory and negative photoconductivity effects of Ge nanocrystals embedded in ZrO_2/Al_2O_3 gate dielectrics", Appl. Phys. Lett. (2003), vol. 83, pp. 138-140.

[10] Q. Ye, R. Tsu, and E. H. Nicollian, "Resonant tunneling via microcrystalline-silicon quantum confinement", Phys. Rev. (1991), Vol. 44, No. 4, pp. 1806–1811.

[11] H. Hanafi, S. Tiwari, and I. Khan, "Fast and long retention-time nano-crystal memory", IEEE Trans. Elec. Dev,(1996), Vol 43, No. 9, pp. 1553-1558.

[12] Choi S.-H and Elliman R.G, "Reversible charging effects in SiO2 films containing Si nanocrystals", Appl. Phys. Lett. (1999), Vol. 75, No. 7, pp. 968-970.

[13] E. Kapetanakis, P. Normand, D. Tsoukalas, G. Kamoulakos, D. N. Kouvatsos,J. Stoemenos, S. Zhang, J. van den Berg, and D. G. Armour, "MOS Memory Using Silicon Nanocrystals Formed by Very-Low Energy Ion Implantation", in Proc. 30th European Solid State Device Research Conf. ~ESSDERC 2000, Cork, Ireland, 11–13 September 2000, p. 476-479.

[14] E. Kapetanakis, P. Normand, D. Tsoukalas, K. Beltsios, J. Stoemenos, S. Zhang, and J. van den Berg, "Charge storage and interface states effects in Si-nanocrystal memory obtained using low-energy Si+ implantation and annealing", Appl. Phys. Lett, (2000), Vol. 77, No. 21, pp. 3450-3452.

[15] T. Maeda, E. Suzuki, I. Sakata, M. Yamanaka, and K. Ishii, "Electrical Properties of Si Nanocrystals Embedded in an Ultrathin Oxide", Nanotechnology, (1999), Vol. 10, No. 30, pp. 127-131.

[16] N. Takahashi, H. Ishikuro, and T. Hiramoto, "Control of Coulomb blockade oscillations in silicon single electron transistor using silicon nano-crystal floating gates", Appl. Phys. Lett. (2000) Vol. 76, No. 2, pp. 209-211.

[17] P. Photopoulos, A. G. Nassiopoulou, D. N. Kouvatsos, and A. Travlos, "Photoluminescence from nanocrystalline silicon in Si/SiO2 superlattices", Appl. Phys. Lett. (2000) Vol. 76, No. 24, pp. 3588-3590.

[18] P. Photopoulos and A. G. Nassiopoulou, "Room- and lowtemperature voltage tunable electroluminescence from a single layer of silicon quantum dots in between two thin SiO2 layers", Appl. Phys. Lett. (2000), Vol. 77, No. 12, pp. 1816-1818.

[19] Q. Zhang, S. C. Bayliss, and D. A. Hutt, "Blue photoluminescence and local structure of Si nanostructures embedded in SiO2 matrices", Appl. Phys. Lett. (1995), 66, pp. 1977-1979.

[20] J. U. Schmidt and B. Schmidt,"Investigation of Si nanocluster formation in sputter-deposited silicon sub-oxides for nanocluster memory structures", Mat. Sci. Eng. B, (2003), 101, pp. 28.

[21] A.J. Steckl, J. Xu, H. C. Mogul and S. M. Prokes,"Si Oxyhydrides on Stain-Etched Porous Si Thin Films and. Correlation with Crystallinity and Photoluminescence", J. Elecrochem. Soc, (1995), 142 (5), pp. 69-71.

[22] Yang-Guo Chen, Zheng Fang, Kun-Yang Yuan, Quan-Ru Zhang, and Shao-Fen Wang, "Solubilities of $LaCl_3$ in HCl Aqueous Solution at (25, 35, and 45)°C ", J. Chem. Eng. Data, (2008), Vol. 53, No. 1, pp. 262-264.

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