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Efficient Wide Frequency Range Voltage Control Oscillator for PLL using 180nm CMOS Technology

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***Abstract* – This paper proposes a design technique of efficient wide frequency range voltage control oscillator (VCO). Here,A Five stage CMOS VCO is implemented in Tanner S-Edit environment with high oscillation frequencies for different input control voltage (D.C.) & low power consuming circuit with low W/L Ratio. The 180µm technology is used for circuit simulation. This circuit gives different Oscillation from 342.4 MHz to 1.683 GHz at input control voltage range from 0.5V to 1.0V. Circuit simulation resulted that Average Power consumption at 1.0V is 2.1288e-004 W.**

Keywords:Power, Low W/L ratio, Voltage Control Oscillator (VCO), Phase lock loop (PLL).

I. INTRODUCTION

A Phase locked loop (PLL) is designed in feedback loop that helps to lock the on chip clock phase for an input clock or signal. A PLL are widely used in a digital circuit for clock generator as well as for timing recovery. For this purposes the high performance PLL are in need. Although the clock generation in off-chip reference frequency are limited for a crystal oscillator (Typically in several MHz). A PLL received the clock and multiplies with several GHz operating frequency. Timing recovery pertains to the data communication between all parts of the chip. To satisfy the increase in on-chip processing rate there must to increase in data rate. The input data and the on-chip clock are not fixed.

A PLL is a closed loop control system which compares both the input and output phase. High performance digital system are ought to clock for a sequential operation and synchronization between functional unit and ICs. Since there is rapid increase in data generation of processing technology and processor architecture, there is a necessity of high frequency clock generation. For this the well-known technology is a Phase locked loop being in admire.

II. SYSTEM OVERVIEW

The basic concept of Phase locking was being same since 1930s. However the designing techniques of PLL with voltage control oscillator (VCO) are to be a challenging for the clock timing, power consumption and area. A PLL is a multiplier for a low frequency clock for producing high frequency clock. A PLL is a negative feedback control circuit. The overall significant of the PLL is to match the clock with the feedback signal with phase mode.The PLL is continuously comparing the signal since they are lock mode the output become constant.
The PLL having five main blocks,

- Phase Detector
- Charge Pump
- Low Pass Filter
- Voltage Control Oscillator
- Divided by N Counter.

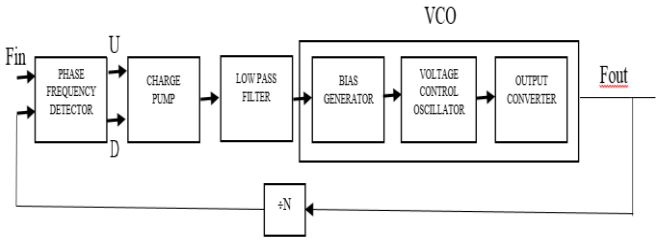

Figure 1: A block diagram of PLL

Voltage control oscillator is the very necessary block for the designing of RF transceiver for generation of local oscillation frequency to up and down convert the input signal. Oscillators generate periodic output sinusoidal signal.

The condition should be simultaneously satisfied for steady state oscillations,

- The loop gain $|H(j\omega_0)|=1$
- The total phase shift around the loop must be 0^0 or 360^0

The phase frequency detector (PFD) is possible to error output signal based on the reference clock and feedback clock. If there is a phase difference between these two signals then there is possibility for generation of up/down synchronized signal to the charge pump/low pass filter. If the

error signal from the PFD is an up signal then charge pumps charges the capacitor of low pass filter which decrease the control voltage. Control voltage is the input to the VCO. Thus LPF is necessary to allow DC signal to the VCO and also necessary to store the charge to charge pump. The purpose of VCO is to boost or slow the speed for charge pump.

III. VCO SCHEMATIC

The operation of VCO (Current Starved) is similar to Ring VCO.The PMOS_1 and NMOS_2 act as an inverter, while PMOS_6 and NOMS_10 act as current sourcewe can find inverter as a current starved. PMOS_11 and NMOS_11 since the drain current (I_D) control by the input control voltage.

The schematic representation of 5 stage current starved VCO is shown in Figure 2.Itbuilt by cascading the 5 inverter.

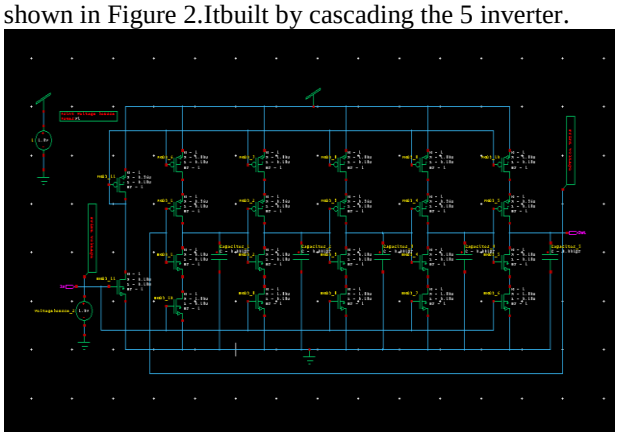

Figure 2: Schematic of 5 stages current starved VCO.

The size for figure 2 is being calculated as a total capacitance. The total capacitance C_T is given by formula,

$$C_T = \frac{[\mathrm{N} \times C_o(W_P L_P + W_N L_N)]}{2}$$

Where,

C_o is oxide capacitance

N is the number of cascade inverter

The drain current (I_D) is calculated as

$$I_D = N \times V_{DD} \times C_T \times F$$

The oscillation frequency is given by,

$$F = \frac{1}{N \times T_D}$$

Where, T_D is delay time.

IV. SIMULATION AND OUTPUT

When the output of charge pump is applied to VCO as a control signal the respective output waveform is as shown in figure-3. It seen that the 1.683 GHz output frequency is generated for 1.0 V control voltage.

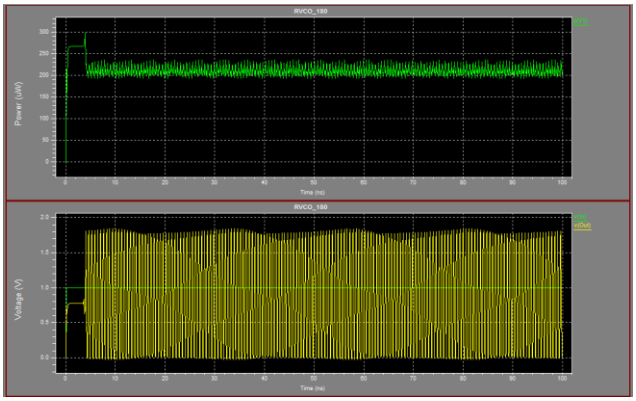

Figure 3: Output waveform of VCO

The output waveform of current starved VCO for control voltage 1.0V generates an output frequency of 1.683 GHz as shown in figure-3. The simulation results for Average power consumption for figure-2 is calculate in Tanner T-Spice is 2.1288e-004 Watt.

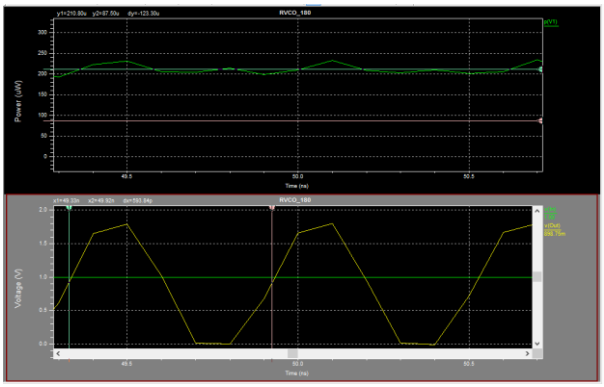

Figure 4: Measurement of output frequency.

When the control voltage is varying continuously form 0.5V to 1.0V the oscillation frequency is varying from 342.4 MHz to 1.683 GHz respectively as shown in table 1.

Table 1: Control voltage Verses output frequency.

Sr. No.	Control Voltage (Volt)	Output Frequency (Hz)
1.	0.5	342.421 MHz
2.	0.6	675.675 MHz
3.	0.7	1.244 GHz
4.	0.8	1.532 GHz
5.	0.9	1.638 GHz
6.	1.0	1.683GHz

The Control voltage verses output frequency graph shown in figure-5.

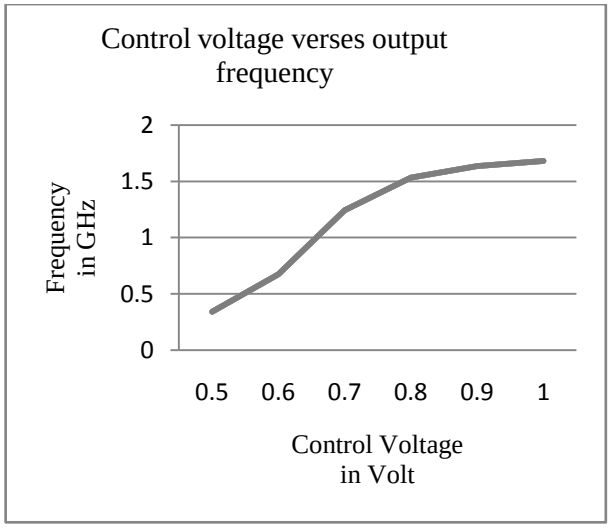

Figure 5: Graphical representation of Control voltage verses output frequency

V. CONCLUSION

This paper presents schematic of low power, output frequency 1.683 GHz current starved VCO using Tanner (S-Edit). The simulation of this project shows that the VCO could achieve high frequency of oscillation with low power consumption. This design may be compatible for PLL as a frequency multiplier. The efficient wide frequency VCO with low power consumption is successfully achieves.

REFERENCES

[1] Dongmin Park, et al, ―Design techniques for low voltage VCO with wide tuning range and low sensitivity to environmental variations‖, in IEEE Transaction on Microwave Theory and Techniques, vol. 57, no. 4, April 2009, pp 767 – 774.

[2] Akima, H. ; Dec, A. ; Suyama, K.- A wide tuning 1.3 GHz LC VCO with fast settling noise filtering voltage regulator in 0.18 µm CMOSprocess, in IEEE Transaction on Microwave Theory and Techniques, 2010, pp 333-336

[3] Bodhisatwa Sadhu, Member, IEEE, Mark A. Ferriss, Arun S. Natarajan, SonerYaldiz, Member, IEEE, Jean-Olivier Plouchart, Senior Member, IEEE, Alexander V. Rylyakov, Alberto Valdes-Garcia, Benjamin D. Parker, AydinBabakhani, Scott Reynolds, Xin Li, Senior Member, IEEE, Larry Pileggi, Fellow, IEEE, Ramesh Harjani, Fellow, IEEE, José A. Tierno, and Daniel Friedman, Member, IEEEA ---Linearized, Low-Phase-Noise VCO-Based 25-GHz PLL with Autonomic Biasing, VOL. 48, NO. 5, MAY 2013

[4] Luciano Severino de Paula, Eric Fabris, Sergio Bampi, AltamiroAmadeuSusin,‖ A High Swing Low Power CMOS Differential Voltage-Controlled Ring Oscillator‖in 2007 IEEE Computer Society Annual Symposium on VLSI(ISVLSI'07)

[5] Sang_yeop Lee, ShuheiAmakawa, Noboru Ishihara, and Kazuya Masu,‖ Low-Phase-Noise Wide-Frequency-Range Ring-VCO-Based Scalable PLL with Subharmonic Injection Locking in 0.18 µm CMOS‖, in IEEE 2010.

[6] To-Po Wang, ―A k-band low power colpitts VCO with voltage to current positive feedback network in 0.18 µm CMOS,‖ in IEEE on Microwave and Wireless Components Letters, vol. 21, no. 4, April 2011, pp 218 – 220.

[7] HaripriyaJanardhan, Mahmoud FawzyWagdy, ―Design of a 1GHz Digital PLL Using 0.18µm CMOS Technology‖ in IEEE 2006 Third International Conference on Information Technology: New Generations (ITNG'06)

[8] B .Razvi, Design of ANALOG CMOS Integrated Circuits, McGraw-Hill, 2001

[9] Nikolay T. Tchamov, Svetozar S. Broussev,‖Dual-Band LC VCO Architecture With a Fourth-Order Resonator‖ in IEEE Transactions on circuits and systems—II: Express Briefs, vol. 54, no. 3, March 2007

[10] Guochi Huang, Student Member, IEEE, and Byung-Sung Kim, Member, IEEE, "Low Phase Noise Self-Switched Biasing CMOS LC Quadrature VCO‖ in IEEE Transactions on Microwave Theory and Techniques, vol. 57, no. 2,February2009.