Efficient Implementation of an Arithmetic and Logic unit using Modified GDI technique

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***Abstract*—Low power design has become one of the primary focuses in digital VLSI circuits, especially in clocked devices like microprocessor and portable devices. Optimization of several devices for speed and power is a significant issue in low-voltage and low-power applications. These issues can be overcome by incorporating Gated Diffusion Input (GDI) technique. Using GDI cell makes it possible to reduce the number of transistors. This method is suitable for the design of low-power logic gates, with a much smaller area than Static CMOS and existing PTL techniques. As opposite to our originally proposed GDI logic, the modified GDI technique is fully compatible for implementation in a standard CMOS process. This technique allows reducing power consumption and delay of digital circuits, while maintaining low complexity of logic design. This paper presents implementation of an 8-bit arithmetic and logic unit using modified GDI technique. The design is simulated using Cadence Virtuoso in 180nm technology. The simulation shows that the design is more efficient with less power consumption, less surface area and is faster as compared to pass transistor and CMOS techniques.**

Index Terms*—GDI technique; modified GDI technique; ALU; CMOS gates; transmission gates; pass transistor logic gates

I. Introduction

In past technology, the main concentrations of the VLSI designer were performance of the device, area required, cost and reliability of the complete system. Power dissipation was secondary issue. But in todays technology, it has been changed and power dissipation is given equal weightage to area and speed considerations. So many factors have been contributed to this trend. But the main driving factor is the remarkable success and growth of personal computing devices such as multimedia products, portable desktops and wireless communication systems like personal communicators which needs high- speed computation and complex functionality with low power consumption. In such applications, low power consumption is a critical design issue.

The aim to reduce power dissipation is differ from one application to other application. In the class of micropowered batteryoperated devices like cellular phones and personal digi-tal assistants, the motive is to make long battery life, minimum weight and the packaging cost low. For good performance, portable electronic devices such as laptop, palm top and notebook computers, the aim to reduce the power consumption of the electronics portion of the system to a point which is almost half of the total power consumption. Hence, for high speed and low power performance, non-battery operated systems, such as desk-top computers, multimedia digital signal processors and digital workstations; the overall goal of power minimization is to reduce system cost for cooling, packaging and energy while maintaining long-term device reliability. These different requirements impact how power is addressed and how much the system designer is wishing to sacrifice in performance and device price to obtain minimum power consumption.

Power dissipation in CMOS circuits is caused by three main sources: 1) the charging and discharging of capacitive loads due to change in input logic levels. 2) the short-circuit current arises because of the direct current path between the supply rails during output transitions and 3) the leakage current which is determined by the fabrication technology, consist reverse bias current in the parasitic diodes formed between source and drain diffusions and the bulk region in a transistor as well as the sub threshold current that arises from the inversion charge that exists at the gate voltages below the threshold voltage, The short- circuit and leakage currents in CMOS circuits can be made small with proper device and circuit design techniques. The dominant source of power consumption is the charging-discharging of the node capacitances and it can be minimizing by reducing switching activity of transistors. Switching activity of the digital circuits is also a function of the logic style used to implement the circuit. The new Modified GDI technique called modified gate diffusion input technique allows solving most of the problems occur in various CMOS and PTL techniques. The Modified GDI technique compare to other techniques allows reducing power consumption, propagation delay, reduced number of transistors and area of digital circuits with maintaining low complexity of logic design.

Here ALU is designed in different way by using Modified GDI cells. The ALU can perform operations such as addition, sub-traction, multiplication and division using Kogge Stone Adders (KSA). The design is implemented in Cadence Virtuoso in 180nm technology.

II. Gate Diffusion Input Technique

Morgenshtein has proposed basic GDI cell shown in Fig.1. This is a new approach for designing low power digital combinational circuit.GDI technique is basically two transistor

implementation of complex logic functions which provides in-cell swing restoration under certain operating condition. This approach leads to reduction in power consumption, propagation delay and area of digital circuits is obtained while having low complexity of logic design. An important feature of GDI cell is that the source of the PMOS in a GDI cell is not connected to VDD and the source of the NMOS is not connected to GND. Therefore GDI cell gives two extra input pins for use which makes the GDI design more flexible than CMOS design.

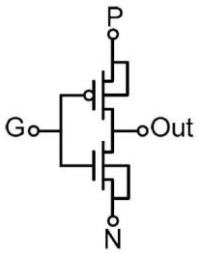

Fig. 1. Basic GDI Cell

There are three inputs in a GDI cell - G (common gate input of NMOS and PMOS), P (input to the source/drain of PMOS) and N (input to the source/drain of NMOS).Bulks of both NMOS and PMOS are connected to N and P respectively. Table 1 shows different logic functions implemented by GDI logic based on different input values. So, various logic functions can be implemented with less power and high speed with GDI technique as compared to conventional CMOS design.

N	P	G	Out	Function
0	1	A	A'	INVERTER
0	B	A	A'B	FUNCTION1
B	1	A	A'+B	FUNCTION 2
1	B	A	A+B	OR
B	0	A	AB	AND
C	B	A	A'B+AC	MUX
B'	B	A	A'B+B'A	XOR
B	B'	A	AB+A'B'	XNOR

Fig. 2. Logic functions implemented using basic GDI cell

III. Modified Gate Diffusion Input Technique

Though the original GDI cell offers a lot of advantages its performance deteriorates. In addition to this physical im-plementation of basic GDI cell is not possible in traditional p-well progression. Furthermore, realizing via twinwell/ triple-well mechanism would necessitate the fundamental GDI cell to possess an enhanced area owing to discrete wells per transistor. This fundamental conjecture is imprecise as the source along with drain nodule rely on the logic values provided at the input. Therefore, in the primary GDI cell, the substrate effect was eradicated in circumstances where the body was attached to the source, but an enhancement in threshold voltage transpired on attachment of the bulk to the drain. Moreover since the basic GDI cell obliges twin-well CMOS or SOl procedure to comprehend, accomplishment of a rudimentary GDI chip will be a dear one.

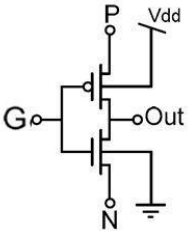

Fig. 3. Modified GDI Cell

The modified GDI cell as given away in Fig.2 overcomes the drawbacks suffered by basic GDI cell and is extremely similar to the basic GDI cell except for the fact that the bulks of PMOS as well as NMOS transistors in a modified GDI cell are persistently fixed to VDD and GND, respectively. This facilitates effortless realization of the GDI gates in typical CMOS procedures. The consequence of the body effect on circuit functioning is enormously alike to that of basic GDI cell. However with technology scaling, the influence of source-body voltage on transistor threshold voltage gets exceedingly reduced i.e. the substrate-bias coefficient in equation (1) becomes smaller.

$$V_{th} = V_{tho} + \gamma(\sqrt{|2\phi_F + V_{SB}|} - \sqrt{|2\phi_F|}) - \eta V_{DS} \qquad (1)$$

Where Vsb denotes source-body voltage, Vtho denotes the threshold voltage at Vsb= O, represents substrate-bias coefficient, '$_F$ is the Fermi potential while signifies the Drain Induced Barrier Lowering (DIBL) coefficient.

IV. Arithmetic and Logic Unit

Arithmetic and Logic Unit (ALU) serves as the primary computation core for microprocessors. In fact, ALUs are one of the most power hungry building blocks in the processor, raising the power and thermal issues. The presence of multiple ALUs (multi-cores) in current-day processors further aggravates the problem, severely impacting the circuit reliability and increasing the power cost. Hence, low power ALU design is highly desirable especially in battery-powered portable applications for extended battery lifespans. At the system-level, reduced power operation is often achieved by scaling the supply voltage VDD downwards, to near-threshold region (0.6V), and even further to sub-threshold region (0.2V).

The arithmetic and logic unit (ALU) performs all arithmetic

operations (addition, subtraction, multiplication, and division) and logic operations. Logic operations test various conditions encountered during processing and allow for different actions to be taken based on the results. The data required to perform the arithmetic and logical functions are inputs from the designated CPU registers and operands. The ALU relies on basic items to perform its operations. The design of 8-bit ALU performs four arithmetic operations such as ADD, SUBTRACT, MULTIPLY and DIVIDE. The proposed ALU is designed using Modified GDI technique.

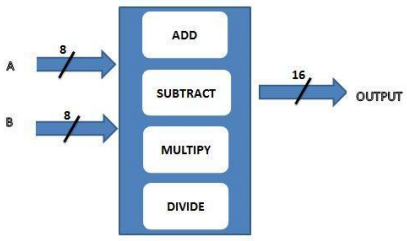

Fig. 4. Block diagram of ALU

The adder is one of the most important components of a ALU. The inputs to ALU are of 8 bits wide and output is 16 bits. The adder used in here is Kogge Stone Adder.

A. Kogge Stone Adder

The KoggeStone adder is a parallel prefix form carry look-ahead adder. It generates the carry signals in O(log n) time, and is widely considered the fastest adder design possible. It is the common design for high-performance adders in industry. It takes more area to implement than the BrentKung adder, but has a lower fan-out at each stage, which increases performance.

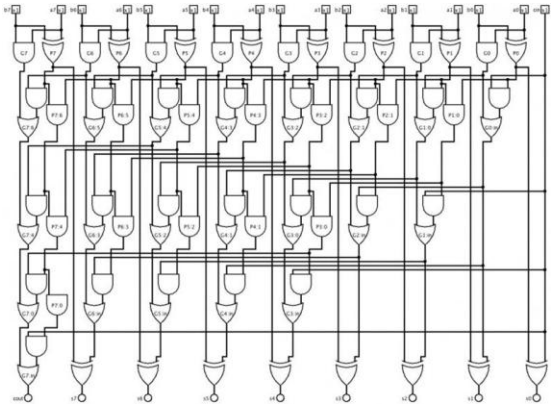

Fig. 5. Schematic of 8-bit Kogge Stone Adder

A 8-bit KoggeStone adder is shown in fig 5. Each vertical stage produces a ”propagate” and a ”generate” bit. The culminating generate bits (the carries) are produced in the last stage (vertically), and these bits are XOR’d with the initial propagate after the input to produce the sum bits.

Propagate signal Pi = Ai xor Bi
Generate signal Gi = Ai and Bi
Sum Si = Pi xor Ci-1
Carry Ci+1 = (Pi and Cin) or Gi

V. IMPLEMENTATION RESULT

The implementation of ALU is done using Cadence Virtuoso in 180nm technology. The adder and subtracter are implemented.

A. Addition

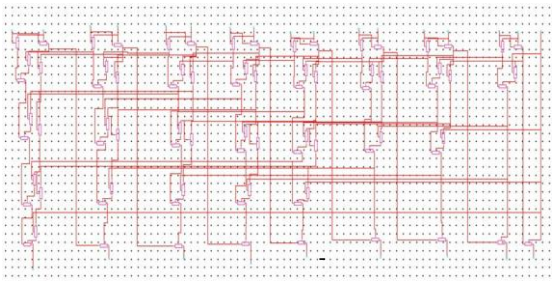

Fig. 6. Schematic of 8 bit KSA

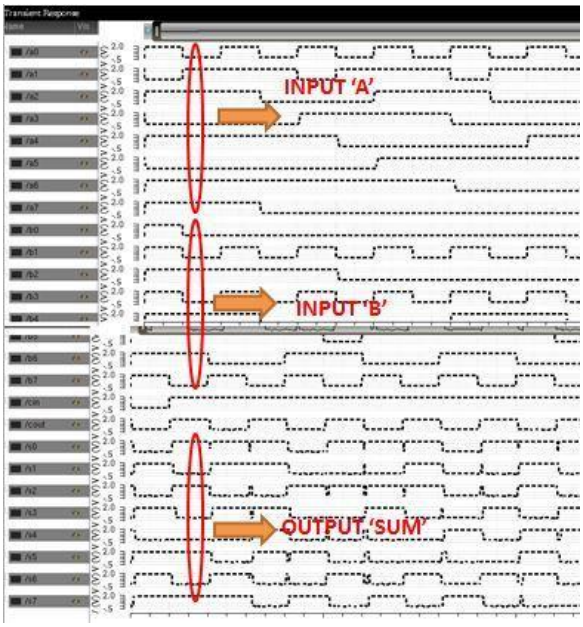

Fig. 7. Simulated Output of KSA

B. Subtraction

Subtraction is done using two’s complement method. Here two’s complement of input ’B’ is added with input ’A’ using 8 bit KSA.

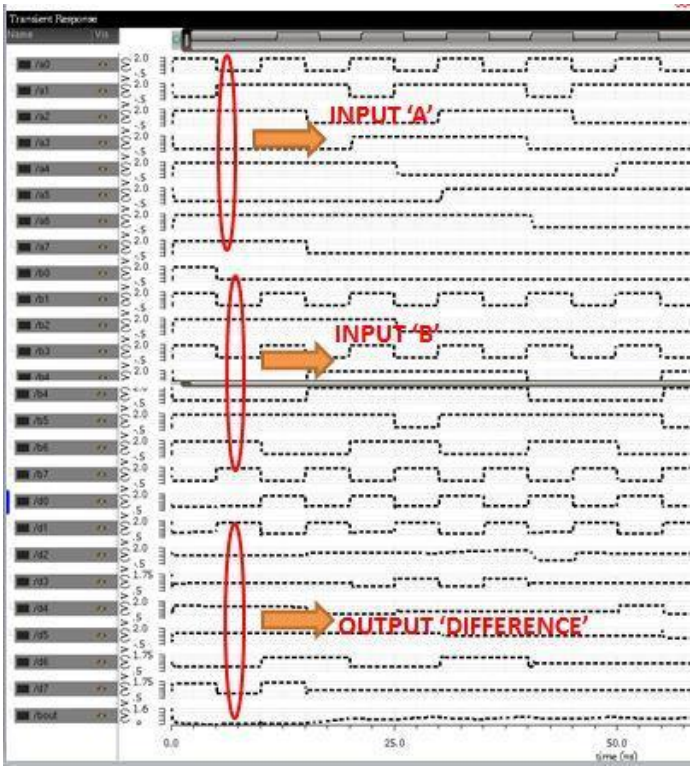

Fig. 8. Simulated Output of two's complement subtractor

Circuit	Delay	Transistor Count
KSA	9.35ns	666
KSA (with mod-GDI)	5.02ns	158
Subtractor using 2's complement	10.49ns	746
Subtractor(with mod-GDI)	5.11ns	238

Fig. 9. Comparison between Modified GDI and Standard CMOS circuits

VI. Conclusion

Power consumption in CMOS circuit is classified in two categorize: static power dissipation and dynamic power dissipation. In todays CMOS circuits static power dissipation is negligible thus not considered as compared to dynamic power dissipation. The power supply is directly related to dynamic power. The numbers of power supply to ground connections are reduced in Modified GDI implementation which reduces the dynamic power consumption. This project deals with development of an 8-bit ALU in Cadence Virtuoso. Here the ALU is designed using Modified GDI technique. Propagation delay and the number of transistors of ALU were compared using CMOS and Modified GDI techniques. Modified GDI technique proved to have best result in terms of performance characteristics.

References

[1] T. Esther Rani, M. Asha Rani, Dr. Rameshwar rao, AREA OPTIMIZED LOW POWER ARITHMETIC AND LOGIC UNIT 978-1-4244-8679-3/11/26.00 2011 IEEE.

[2] Manish Kumar, Md. Anwar Hussain, and L.L.K. Singh, Design of a Low Power High Speed ALU in 45nm Using GDI Technique and Its Pe rformance Comparison, CNC 2011, CCIS 142, pp. 458463, 2011.

[3] Morgenshtein, A., Fish, A., Wagner, I.A.: Gate-Diffusion Input(GDI) A Technique for Low Power Design of Digital Circuits: Analysis and Characterization. In: ISCAS 2002, USA (May 2002).

[4] R.Uma and P. Dhavachelvan, Modified Gate Diffusion Input Technique: A New Technique for Enhancing Performance in Full Adder Circuits 2nd International Conference on Communication, Computing and Security [ICCCS-2012].

[5] Arkadiy Morgenshtein, Idan Shwartz and Alexander Fish, Gate Diffusion Input (GDI) Logic in Standard CMOS Nanoscale Process, 2010 IEEE 26-th Convention of Electrical and Electronics Engineers in Israel.

[6] Suzuki, M.et al., A 1.5-ns 32-b CMOS ALU in double passtransistor logic IEEE Journal of Solid-State Circuits, Vol28, pp 1145-1151, 1993.

[7] P.Balasubramanin and J. Johen, Low power digital design using modified GDI method , International Conference on, Design and Test of Integrated Systems in Nanoscale Technology, (DTIS) , pp.190- 193,Sept. 2006.