EFFICIENT DESIGN OF LOGICAL STRUCTURES USING QUANTUM DOT CELLULAR AUTOMATA

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ABSTRACT--The area and complexity are the major issues in circuit design. Here, we propose different types of adder designs based on Quantum dot Cellular Automata (QCA) that reduces number of QCA cells and area compare to previous designs. The quantum dot cellular automata can implement digital circuits with faster speed, smaller size and low power consumption. The QCA cell is a basic building block of nanotechnology that can be used to make gates, wires and memories. The basic logic circuits used in this technology are the inverter and the Majority Gate (MG), using this other logical circuits can be designed. In this paper, the adders such as half, full and serial bit were designed and analyzed. These structures were designed with minimum number of cells by using cell minimization techniques. The techniques are using two cells inverter and suitable arrangement of cells without overlapping of neighboring cells. The proposed method can be used to minimize area and complexity. These circuits were designed by majority gate and implemented by QCA cells. Then, they simulated using QCA Designer. The Simulated results were verified according to the truth table. The performance analyses of those circuits are compared according to complexity, area and number of clock cycles and are also compared with previous designs.

Index Terms—Adders, nanocomputing, quantum-dot cellular automata (QCA).

I.INTRODUCTION

1.1 An Introduction to the Problem

In 1965, Gordon Moore predicted that the number of transistors that could be integrated into a single die would grow exponentially with time. Moore's law has governed microprocessor manufacturing processes, and consequently microprocessor performance ever since. However, recent studies indicate that during the next two decades, the laws of nature will begin to govern microprocessor design and fabrication. Today many integrated circuits are manufactured at 0.25-0.33 micron processes. As device sizes decrease to an order of 0.05 microns (a technology that is currently unrealizable), physical limitations of conventional electronics including power consumption, Interconnect, and lithography will become increasingly difficult [10].

1.2 An (Alternative) Solution

As an alternative to CMOS-VLSI, researchers have proposed an approach to computing with quantum dots, the Quantum cellular automata (QCA). First proposed 1 in 1994, unlike conventional computers in which information is transferred from one place to another by means of electrical current, QCA transfers information by propagating a polarization state [12, 11]. QCA is based upon the encoding of binary information in the charge configuration within quantum dot cells. Computational power is provided by the Coulombic interaction between QCA cells. No current between cells and no power or information is delivered to individual internal cells. The local interconnections between cells are provided by the physics of cell-to-cell interaction due to the rearrangement of electron positions [12]. While there is still much work to be done, early experimental results indicate that QCA may be an extremely viable alternative to CMOS. QCA cells and a simple QCA logical device have been successfully fabricated and tested [3].

The rest of this brief is organized as follows: a brief back-ground of the QCA technology II and III. QCA Standard Functions existing adders designed in QCA is given in Section IV, the novel adder design is then introduced in Section V, and QCA Implementation and Tables VI finally, in Section VII conclusions are drawn.

II. BACKGROUND

A QCA is a nanostructure having as its basic cell a square four quantum dots structure charged with two free electrons able to tunnel through the dots within the cell [1]. Because of Coulombic repulsion, the two electrons will always reside in opposite corners. The locations of the electrons in the cell (also named polarizations *P)* determine two possible stable states that can be associated to the binary states 1 and 0.

Although adjacent cells interact through electrostatic forces and tend to align their polarizations, QCA cells do not have intrinsic data flow directionality. To achieve controllable data directions, the cells within a QCA design are partitioned into the so-called clock zones that are progressively associated to four clock signals, each phase shifted by 90°.

This clock scheme, named the zone clocking scheme, makes the QCA designs intrinsically pipelined, as each clock zone behaves like a D-latch.

2.1 QCA Design Architecture

2.1.1 Basics of QCA:

The basic elements of QCA are QCA cell, Majority gate and Invertor. These is important elements. In QCA cell each cell is having four quantum dots and is having two free

electrons. The locations of the electrons determine the binary states.Fig.1 shows the QCA cell diagram.

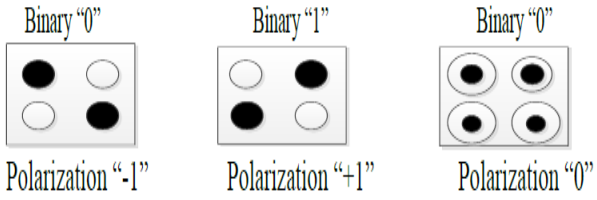

Fig.1 QCA Cell Polarization.

2.1.2 QCA Cell:

A quantum-dot cellular automata (QCA) is a square nanostructure of electron wells having free electrons. Each cell has four quantum dots [2].The four dots are located in the four corners .The cell can be charged with two free electrons. By using the clocking mechanism, the electrons tunnel to proper location during the clock transition. Thus there exist two equivalent energetically arrangements of the two electrons in the QCA cell as shown in Fig.1.These two arrangements can represent logic 1 and logic 0 respectively so that binary information can be encoded. Invertor is represented in Fig.2 and Majority gate in Fig.3.

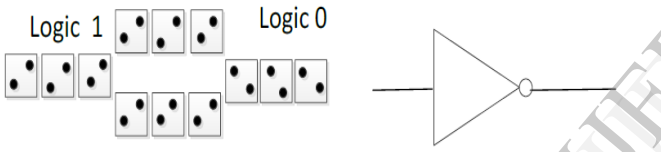

Fig.2. Invertor

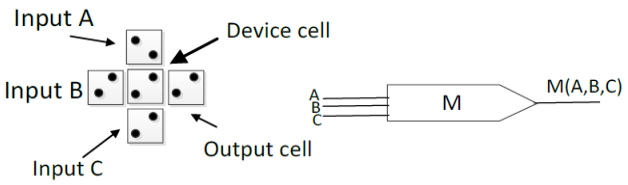

Fig.3. Majority gate

A QCA design permits two options for crossover, termed coplanar crossover and multilayer crossover. While the coplanar crossover uses only one layer but involves usage of two cell types (termed regular and rotated), the multilayer crossover uses more than one layer of cells (analogous to multiple metal layers in a conventional IC). The multilayer crossover is used in this paper for wire crossings since we can effectively cross signals over on another layer and the extra layers of QCA can be used as active components of the circuit. Further, multilayer QCA circuits can potentially consume much less area as compared to planar circuits. Moreover, some studies indicate that coplanar crossover is difficult to fabricate in the molecular implementation.

2.1.3 A Simple QCA Circuit

To implement more complicated logical functions, a subset of simple logical gates is required. For example, it would be impossible to implement a multiplexor, decoder, or adder in QCA without a logical AND gate, OR gate, or inverter. It has been demonstrated that a value's complement can be obtained simply by ripping it o_ a 45-degree wire at the proper location. Implementing the logical AND and OR functions is also quite simple. The logical function for the majority gate is:

$$Y = AB + BC + AC$$

The AND function can be implemented by setting one value (A, B, or C) in equation to a logical 0. Similarly, the OR function can be implemented by Setting one value (A, B, or C) in equation to a logical 1. This result s in the equations:

$$AND = AB + B(0) + A(0) = AB$$
$$OR = AB + B(1) + A(1) = A + B$$

It is worth noting that because this property exists (i.e. the ability to generate the AND and OR functions) and given the fact that it is possible to obtain the inverse of a signal value, the QCA logic set is functionally complete meaning that any logical circuit can be generated with QCA devices. More complex logical circuits (such as the multiplexor can then be constructed from at least AND and OR gates if not clever combinations of majority gates. QCA cells labeled anchored in have their electron polarization frozen to successfully implement AND and OR functions.

III. QCA STANDARD FUNCTIONS

The three variables A,B and C to facilitate the conversion of a sum of-products expression to minimized majority logic. Based on that to obtain the efficient majority expression for any given three-variable Boolean function amenable to QCA implementation. The simplified majority expressions for some standard functions are given in the table. The AND and OR gates are realized by fixing the polarization to one of the inputs of the majority gate to either P = −1 (logic "0") or P = 1 (logic "1").

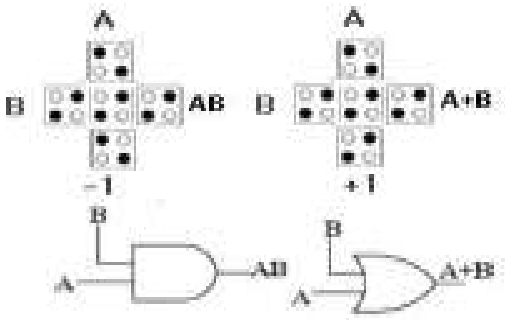

Fig. 4 .Layout of AND and OR gates.

The NAND function is the complement of AND functions. It is realized by connecting AND gate (MG) followed by an inverter. Similarly the NOR gate is realized by connecting OR gate (MG) followed by an inverter. If the last two cells are arranged as shown in the following figure then it acts as an inverter. By using this 2cell inverter, the area required and complexity can be minimized.

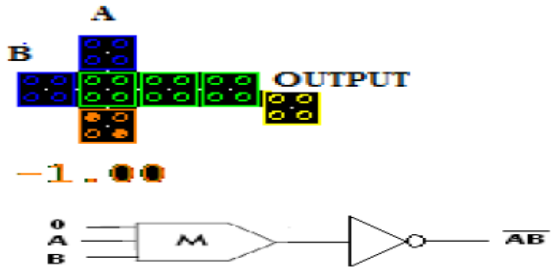

Fig. 5 .Layout of NAND gate.

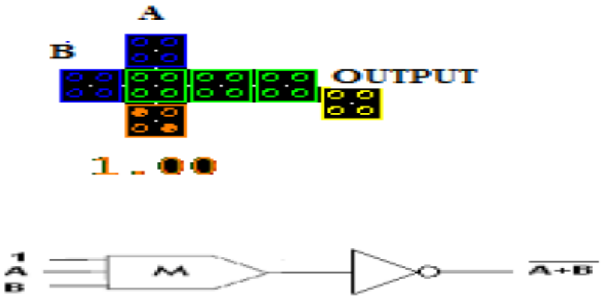

Fig. 6 .Layout of NOR gate

The XOR is a logical operation on two operands that results in a logical value of true if and only if one of the operands, but not both, has a value of true. This forms a fundamental logic gate in many operations to follow. The realization is done making use of majority gates (MGs) and following the equations as follows

$A \oplus B = A'B + AB'$

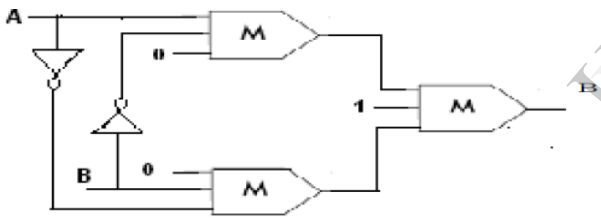

Fig.7.XOR schematic

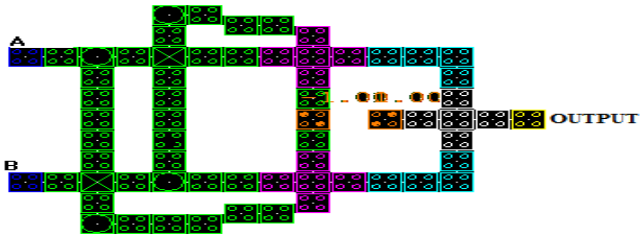

Fig.8. Layout of XOR gate

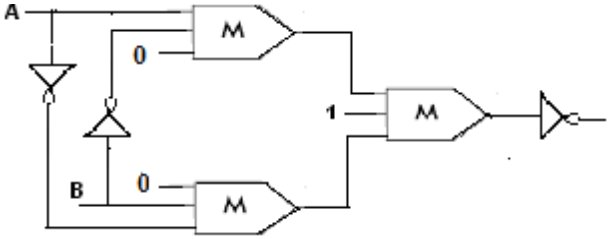

Fig.9.Ex-NOR schematic.

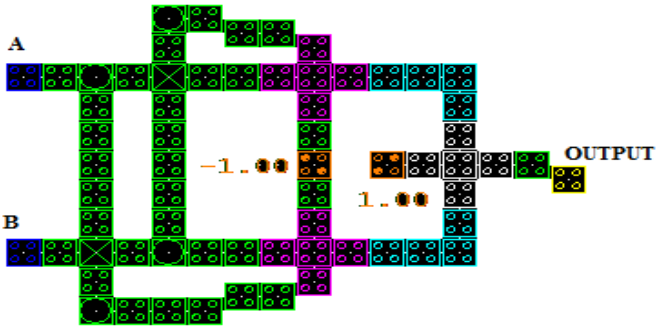

Fig.10. Layout of Ex-NOR gate

IV EXISTING QCA ADDERS

In this section, we first existing a new QCA addition algorithm and the corresponding one-bit QCA adder structure that reduces the number of the majority gates and inverters required by existing designs [5]-[6]. Then, we demonstrate that, using this structure, we can obtain efficient carry look ahead *n*-bit QCA adders.

4.1. Existing QCA Adders

We now introduce a new design of one-bit QCA adder based on the proposed algorithm. The proposed one-bit QCA adder consists of three majority gates and two inverters. It results in reduced hardware compared to the original full adder [5], [6] and retains the simple clocking scheme.

It is noted that the bit-serial QCA adder [7] uses a variant of the proposed one-bit QCA adder. To create an *n*-bit adder, we arrange *n* proposed one-bit adders vertically in a column. The clocking of the cells within the *n*-bit adder is designed such that the carry will propagate down to the last bit before the sum is calculated, thereby implementing a CLA adder. The proposed QCA adder design requires fewer majority gates and inverters while maintaining the same clocking scheme and speed in comparison with existing QCA adders. Compared to the bit-serial QCA adder, the proposed design is *n* times faster, at the expense of being approximately *n* times larger in area. Furthermore, the complicated feedbacks control.

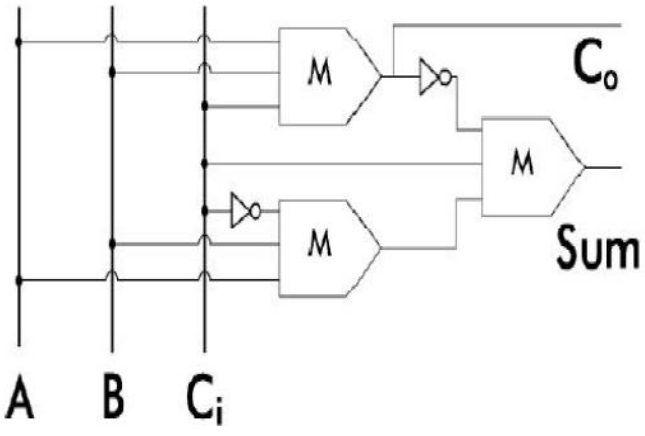

Fig 11: Existing one-bit QCA full adder

V. NOVEL QCA ADDER

To introduce the novel architecture proposed for implementing ripple adders in QCA, let consider two *n*-bit addends *A* = *an*−1, . . . , *a*0 and *B* = *bn*−1, . . . , *b*0 and suppose that for the *I* th bit position (with *i* = *n* − 1, . . . , 0) the auxiliary propagate and generate signals, namely *pi* = *ai* + *bi* and *gi* = *ai* · *bi* , are computed. *ci* being the carry produced at the generic *(i*−1) bitposition, the carry signal *ci*+2, furnished at the (*i*+1)th bit position, can be computed using the conventional CLA logic reported in (2). The latter can be rewritten as given in (3), by exploiting Theorems 1 and *2* demonstrated in [15]. In this way, the RCA action, needed to propagate the carry *ci* through the two subsequent bit positions, requires only one MG. Conversely, conventional circuits operating in the RCA fashion, namely the RCA and the CFA, require two cascaded MGs to perform the same operation.

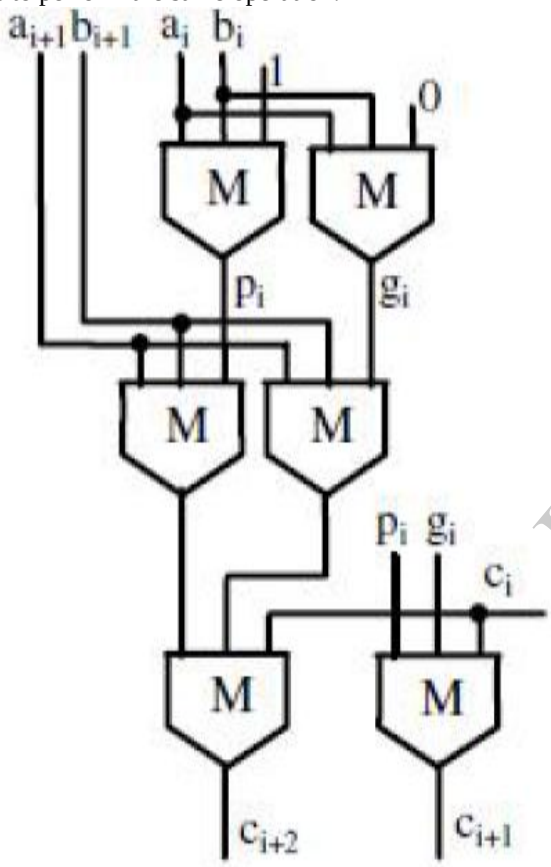

Fig 12: Novel 2-bit basic module.

In other words, an RCA adder designed as proposed has a worst case path almost halved with respect to the conventional RCA and CFA is exploited in the design of the novel 2-bit module shown in Fig. 1 that also shows the computation of the carry *ci*+1 = *M(pi gici)*. The proposed *n*-bit adder is then implemented by cascading *n*/2 2-bit modules. Having assumed that the carry-in of the adder is*cin* = 0, the signal *p*0 is not required and the 2-bit module used at the least significant bit position is simplified.

VI. QCA IMPLEMENTATION AND TABLES

6.1 Implementation of Adders using QCA

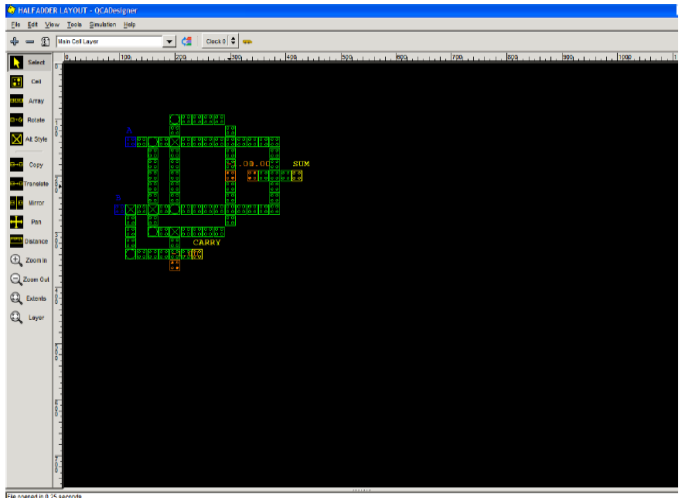

Fig.13 Design of Half Adder using QCA

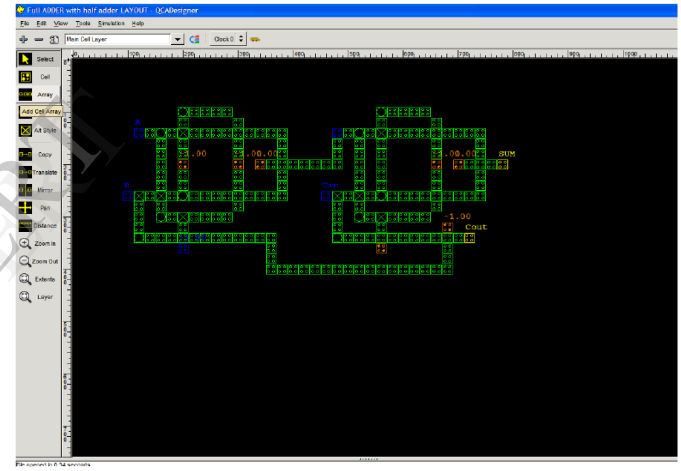

Fig.14. Design of Full adder using two half adder in QCA

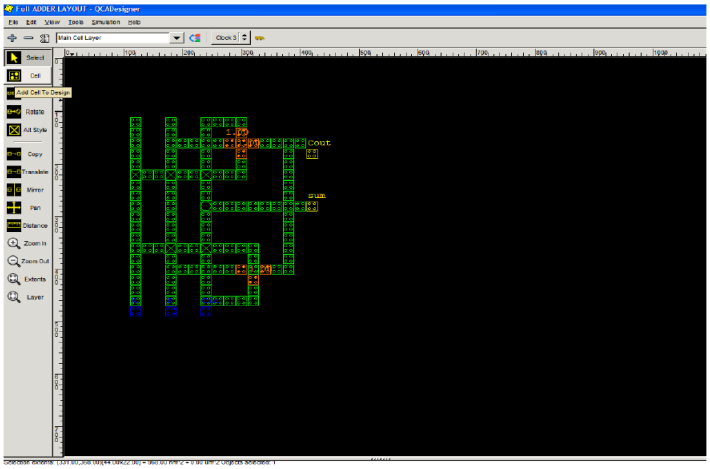

Fig.15. Design of Full adder using QCA.

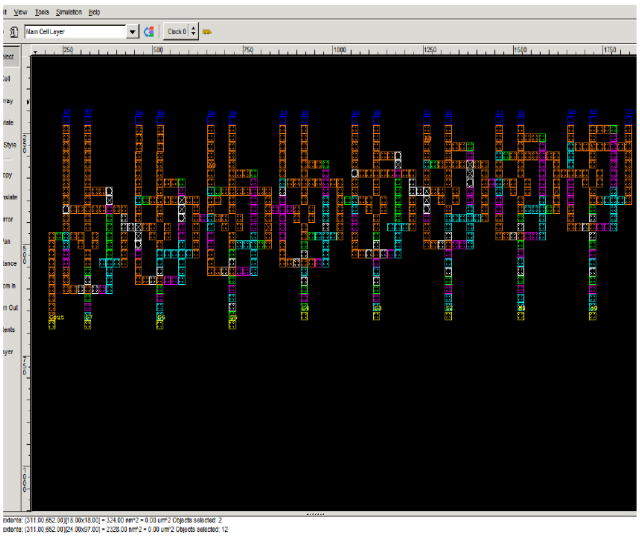

Fig.16. Design of 8-bit Ripple Carry Adder using QCA**.**

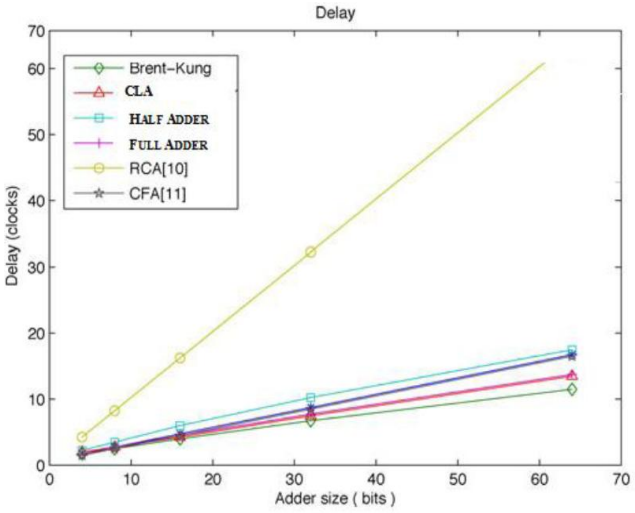

Fig 17.Graph comparing different adders.

TABLE I
COMPARISON RESULTS

Adder	n	Worst Case Path MGs	INV	Cell Count	Size $(\mu m)^2$	Delay	Clock Phases	ADP	Number of Crossovers
New	8	7	1	1606	1.13	2	8	2.26	69
	16	11	1	3587	2.66	3	12	7.98	145
	32	19	1	7691	6.65	5	20	33.25	297
	64	35	1	16667	18.72	9	36	168.48	601
CFA [12]	8	10	1	789	0.949	$2^2/_4$	10	2.37	n.a.
	16	18	1	1769	2.45	$4^2/_4$	18	11.02	n.a.
	32	34	1	4305	7.3	$8^2/_4$	34	62.05	n.a.
	64	66	1	11681	24.2	$16^2/_4$	66	399.3	n.a.
RCA [13]	8	10	1	712	0.74	$2^3/_4$	11	2.03	n.a.
	16	18	1	1602	1.99	$4^3/_4$	19	9.45	n.a.
	32	34	1	3901	6.46	$8^3/_4$	35	56.52	n.a.
	64	66	1	10926	20.92	$16^3/_4$	67	350.41	n.a.
BKA [13]	8	9	1	1782	1.49	$2^2/_4$	10	3.72	n.a.
	16	13	1	4350	3.55	4	16	14.2	n.a.
	32	17	1	11825	10.77	$6^3/_4$	27	72.69	n.a.
	64	21	1	30145	31.20	$11^2/_4$	46	358.8	n.a.
HYBA [14]	8	8	1	1422	1.11	$2^1/_4$	9	2.5	n.a.
	16	10	1	3555	2.66	$3^1/_4$	13	8.65	n.a.
	32	12	1	8946	8.21	$5^2/_4$	22	45.15	n.a.
	64	14	1	22427	25.29	$9^2/_4$	38	240.25	n.a.
CLA [15]	16	11	1	4489	3.65	$4^1/_4$	17	15.51	231
BKA [15]	8	9	1	1462	1.06	$2^2/_4$	10	2.65	104
CLA [16]	8	7	1	1785	1.46	$2^1/_4$	9	3.29	n.a.
	16	9	1	4114	3.67	$3^3/_4$	15	13.76	n.a.
	32	11	1	12540	11.84	$6^3/_4$	27	79.92	n.a.
	64	13	1	33302	35.63	$12^1/_4$	49	436.47	n.a.
CFA [16]	8	7	1	1143	1.02	$2^1/_4$	9	2.29	n.a.
	16	11	1	2817	2.45	$3^1/_4$	13	7.96	n.a.
	32	19	1	6942	6.83	$5^2/_4$	22	37.56	n.a.
	64	35	1	17586	20.46	$9^2/_4$	38	194.37	n.a.

VII. CONCLUSION

A new adder designed in QCA was presented. It achieved speed performances higher than all the existing QCA adders, with an area requirement comparable with the cheap RCA and CFA demonstrated in [13] and [16]. The novel adder operated in the RCA fashion, but it could propagate a carry signal through a number of cascaded MGs significantly lower than conventional RCA adders. In addition, because of the adopted basic logic and layout strategy, the number of clock cycles required for completing the elaboration was limited. A 64-bit binary adder designed as described in this brief exhibited a delay of only nine clock cycles, occupied an active area of 18.72 μm2, and achieved an ADP of only 168.48.

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