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Efficient Design of Digital up Converter using Xilinx System Generator

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Abstract—**Digital Signal Processing has become essential to the design and implementation of high performance audio, video, multi-media, and communication systems signal processing. An essential component of cost effective DSP algorithms is multirate signal processing. Digital Up Converter (DUC) is key component of RF systems in communications, sensing, and imaging. Transmit/receive functionality has become an area of focus as designers attempt to address the need to move data from very high frequency sample rates to chip processing rates. Digital Up Converter is used as sample rate converter. This is the important block in every digital communication system; hence there is a need for effective implementation of digital up converter so that cost can be reduced. In this paper the design of digital up converter is proposed using Xilinx System Generator in order to shorten the design cycle and increase the design productivity. DUC mainly consists of FIR filter, upsampler and DDS blocks.**

Keywords—Digital Up converte(DUC), Finite Impulse response(FIR), Direct Digital Synthesizer(DDS), Xilinx System Generator

I. INTRODUCTION

The Digital up Converter is a digital circuit which implements the conversion of a complex digital base band signal to a real pass band signal. The input complex base band signal is sampled at a relatively low sampling rate, typically the digital modulation symbol rate. The base band signal is filtered and converted to a higher sampling rate before being modulated onto a direct digitally synthesized (DDS) carrier frequency. The DUC typically performs pulse shaping and modulation of an intermediate carrier frequency appropriate for driving a final analog up converter and is used extensively in wireless and wire line communication systems. [3]

Up conversion can be defined as generating new samples by virtue of adding zeroes (also called as Interpolation) and interpolate the new samples as shown in figure1.

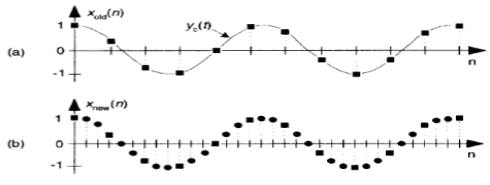

Fig.1. Interpolation (addition of zeroes)

The essential function of a interpolation filter is to increase the sampling rate and to keep the passband imaging error within prescribed bounds.

We have organized this paper as follows. Section 2 presents the working principle and all components of DUC. In Section 3, we discuss the our approach of implementation. Simulation results are given in Section 4. Paper is concluded in Section 5.

II. DIGITAL UP CONVERTOR

Digital up converter (DUC) converts a baseband low data rate signal to a high data rate IF signal. This is done by first up sampling the baseband signal to the required sampling frequency and then mixing it with the high frequency carrier. A functional diagram of the DUC is given in Figure 2.

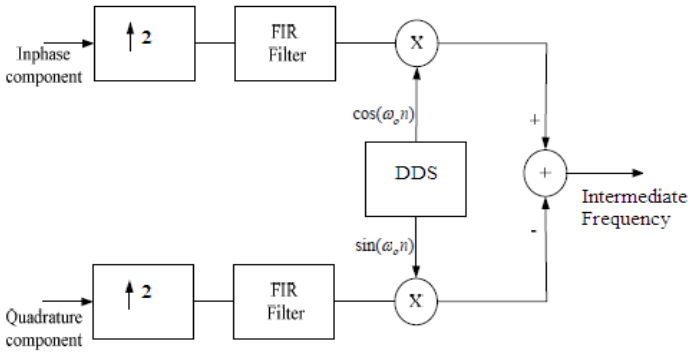

Fig.2. Block diagram of digital Up Convertor

The DUC has two identical paths, one for the inphase and the other for quadrature input. For this reason, it is also referred to as a complex DUC. The baseband signal is upsampled by 2 to before mixing with the direct digital synthesizer(DDS) output, which produces the carrier signal to produce the spectrum centered around the desired modulation frequency. A Direct Digital Synthesizer (DDS) also known as Numerically Controlled oscillator (NCO) synthesizes a discrete-time, discrete-valued representation of a sinusoidal waveform. It is an established method of generated periodic sinusoid signals whenever high frequency resolution, fast changes in frequency and phase, and high spectral purity of the output signal is

required. A major advantage of the DDS is that its output frequency, phase and amplitude can be precisely and rapidly manipulated under digital processor control. Other DDS attributes include the ability to tune with extremely fine frequency and phase resolution, and to rapidly hop between frequencies. The lowpass FIR filter acts as an anti-aliasing filter after upsampling. The specifications of this FIR filter are given inTable 1. [1].

TABLE 1. SPECIFICATIONS FOR FIR FILTER IN DUC

Stop band Frequency	20MHz
Pass band Frequency	5 MHz
Stop band ripple	0.1dB
Pass band ripple	140dB

III. OUR APPROACH

In this paper, we have designed the digital up converter using blocks available in xilinx system generator.The low pass FIR filter is designed using MATLAB FDA tool as shown in figure 3.

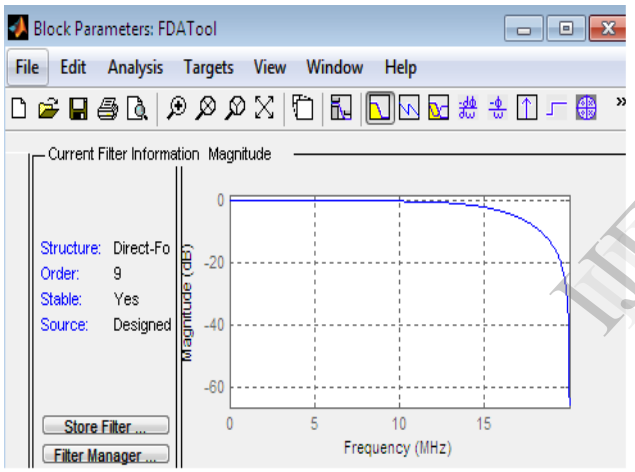

Fig.3. FIR filter response plotted using MATLAB FDA tool

Input signal is 4KHz sinusoidal wave is given to upsampler. The Xilinx upsample block increases the sample rate whose output then given to FIR compiler block. The Xilinx DDS Compiler generates the IF carrier frequency signal. Direct digital synthesizer (DDS), a digital version of the NCO, provides an accurate programmable frequency up to 20MHz. The simple equations that govern the operation of DDS is given by

$$fout=M*Fclk/2\hat{}n \quad (1)$$

$$\Delta f=fclk2n \quad (2)$$

where fclk is the reference clock frequency, fout is the output clock frequency & n is the width of the accumulator.

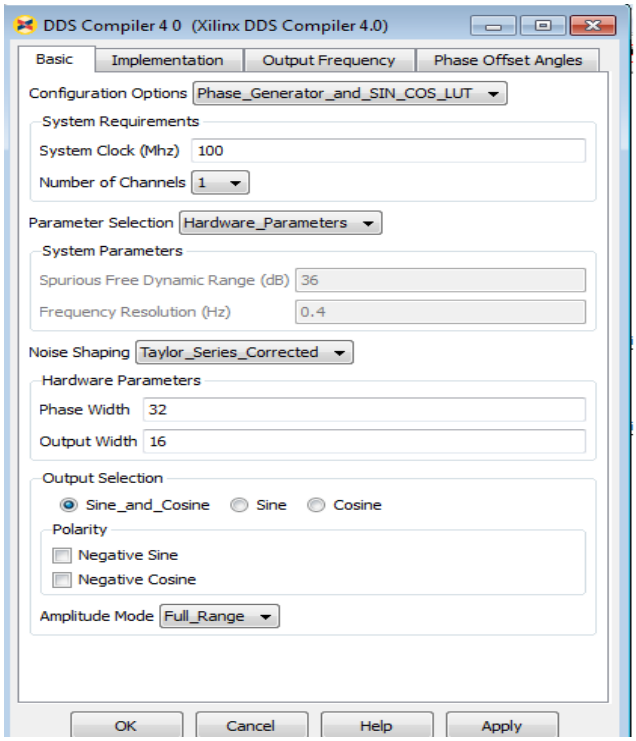

Fig.4. FIR Compiler 4.0. tool specifications

IV. SIMULATION RESULTS

Figure 5 gives the up converter design using Xilinx system generator.

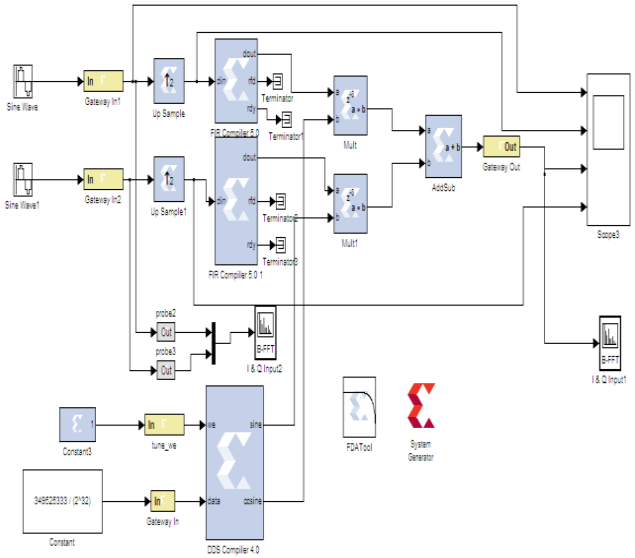

Fig.5. System Generator Implementation of Digital Up Converter

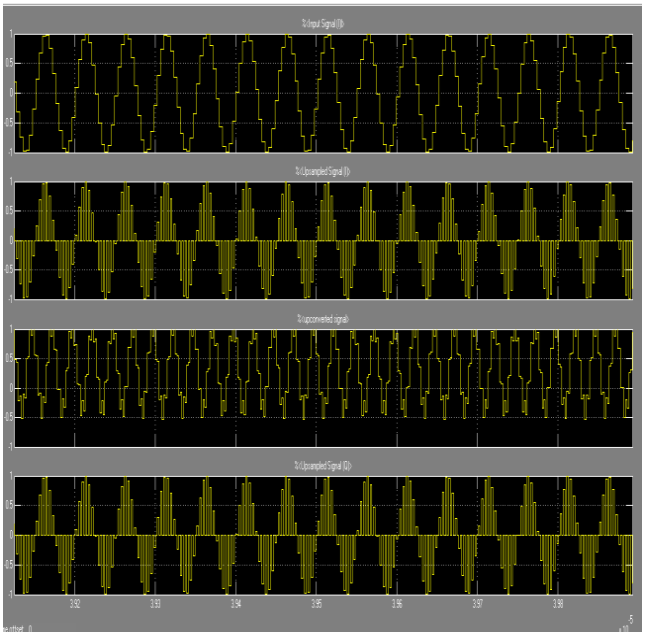

Fig.6. MATLAB output of DUC

A references model is developed for DUC. and DDC using Matlab simulink and simulated. The input of frequency4000 Hz is given to up sampler, the resultant up sampled signal is multiplied with crarrier of frequency ranging from 20MHz. The figure 6 shows the simulated output of DUC for a carrier of 20 MHz. In fig 6, the upper signal my message signal. The next is upsampler's output (in phase component). Third waveform is final upconverted signal, and fourth is upsampled signal (out of phase component).

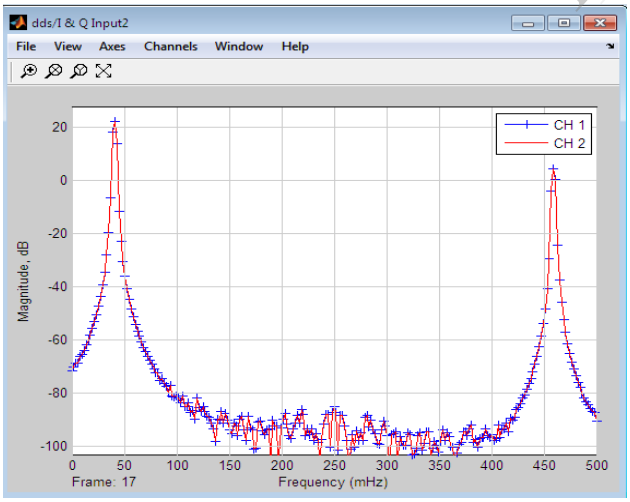

Fig. 6. Spectrum of input signal

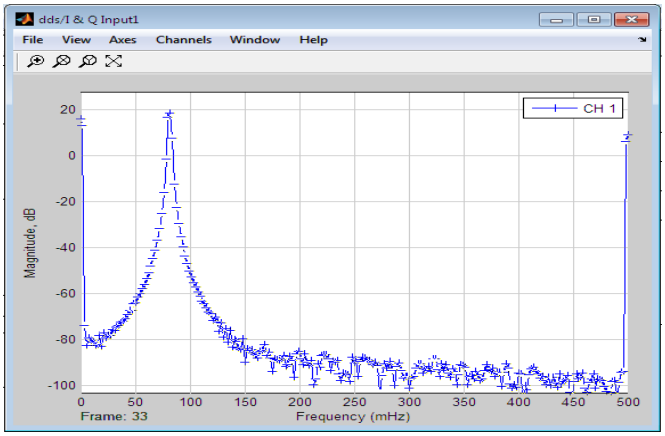

Fig.7. Spectrum of output upconverted signal

V. CONCLUSION

Digital up conversion is becoming necessary in many of today's applications including digital mixing consoles and digital audio work stations, computer communications and multimedia systems. In this paper we have presented an efficient implementation of DUC using Xilinx system generator. Experimental results verify the working of the designed circuits.

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