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# Efficient Design for Fixed-Width Adder-Tree using Carry Select Adder

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***Abstract*:- Adder tree is the design of the adders in the parallel way. The conventional (AT) have full width adder tree and fixed width adder tree types. In the existing method input vectors are truncated for the effective design of the fixed width tree to get the output more accurately The ripple carry adder (RCA) is used in the design of adder tree the proposed design fixed width adder tree is more effective than the traditional designs, and calculates the output almost with the same accuracy as the post-truncated fixed-width than of fixed-width AT. This paper mainly deals with the replacing of adders to reduce the delay. As Adder tree is conventionally proposed with Ripple Carry Adder . Hence in this paper RCA is replaced with Carry Select Adder (CSA) to lower the critical path delay to fasten the hardware system of adder tree and efficient design of adder tree with CSA Suggested.**

INTRODUCTION:

Mobile devices and DSP hardware requires low power, area, efficient designs for better performances. Fixed-point VLSI systems have Digital Signal processing (DSP) algorithms to be implemented. These designs require adder tree (AT) which are commonly used in parallel designs. The shape of adder tree is different from SAT. Consequently, word- length grows in a different order in SAT and AT. Multiplier deals with partial products. Hence, we prefer adder trees to get complex design easy. But the fixed width adder tree and multiplier are not appropriate when we compared regarding schemes. Since, the fixed width AT produces different shaped matrices compared to the fixed width multiplier. However, direct truncation and post truncation methods are employed to the FX-AT and FL-AT conventionally. In direct truncation (DT), one lower order bit of each adder output of full width adder tree is post truncated and in case of post truncation final adder output of FL-AT lower adder bits are truncated. However, these adder trees are implemented using Ripple Carry Adder to get accurate results. It is necessary to have a different approach for developing efficient FX-AT design which is currently missing in the literature. An efficient FX-AT design certainly help to improve the efficiency of dedicated VLSI systems implementing complex DSP algorithm.

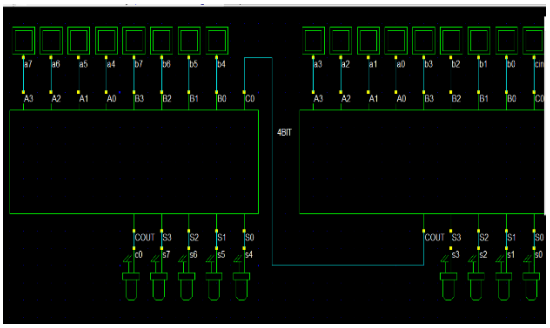


Fig 1.1 8 bit ripple carry adder designed with two 4 bit adders using DSCH2

Carry select adder contains multiplexers and adders. Giving source voltage and ground to the 2 bit adders saves time separately. And the selection line for all the multiplexers is the only one resulted carry which decides the other carry input. And this operation of the carry select adder leads to the lower delay in the hardware. Hence to achieve the lower delay RCA in the adder trees are replaced with carry select adder. As it is the main idea of the proposed paper. However, the area that occupied is more when we compared to the RCA. This area is reduced by lowering hardware measurement. And the time delay when we compare RCA to CSA in adder tree. It means the delay got increased from adder to adder to get the reasonable delay shrink to get the same accurate output. Hence, we suggest carry select adder to get into the Adder Tree. Adders like carry look etc. also gives lower delay, but they occupy higher area which gives little area than CSA at hardware design. Hence when compare to our proposed adder trees, CSA gives lower delay besides little assent area when compared to RCA.

The design like fixed width (FX-AT), full width (FL-AT) are truncated to get the output more rapidly.However we are adding compensative input to the truncated Adder Trees.Hence, bias estimated formula is required to replace neglected input to the adder which result in approximate adder adding in the design. Direct truncation and post truncation process does not give efficient design of adder tree .Hence approximate adder are introduced conventionally for replacing lower significant bits. The main contribution of this paper is:

1)Designing of proposed adder trees by replacing RCA with CSA and Lowering Critical Path Delay(CPD) .
2)Suggesting better adder tree to get the efficient output with lower CPD.

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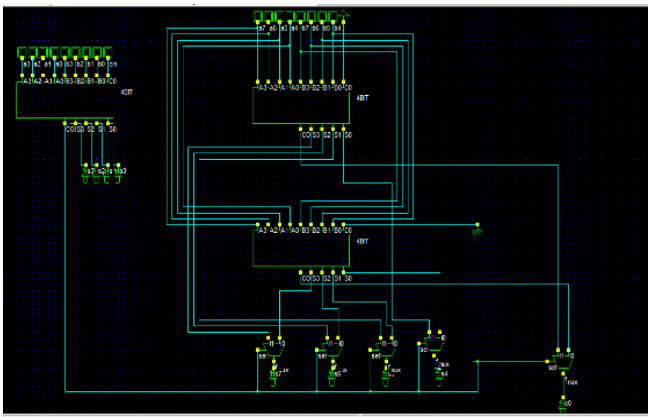

Fig 1.2 8 bit carry select adder designed with 4 bit CSA using DSH2

ARRANGEMENT OF INPUT BITS IN MATRIX FORM :

Truncation is understandable by arranging the bits in the matrix form.Bits of the vector are arranged in the column wise in the matrix. These arrangement gives understanble adder tree easily and they are arranged and divided into 2 parts : MSP and LSP.The caluculation of MSP and LSP is discussed further The truncated input columns are calculated consecutively to get the resulted output with adder inside at which the AT plays the prominent role in the CPD. Hence to cauculate this adder is designed in CSA at adder caluculation. Let the bit matrix be A for N=8 and W=8(8*8) matrix is taken as example for 8 bit. However, for the truncated input neglecting or removing LSP and calculating the MSP gives the calculation more easier than of full width adder tree and FX-AT. Earlier, the Adder trees are excecuted with RCA .And the delay having in AT is reduced by using CSA which is proposed in this paper.

$$A = \begin{array}{ccc|ccccc|ccc} & & & \multicolumn{5}{c|}{\text{MSP}} & \multicolumn{3}{c}{\text{LSP}} \\ 10 & 9 & 8 & 7 & 6 & 5 & 4 & 3 & 2 & 1 & 0 \\ & & & x_{17} & x_{16} & x_{15} & x_{14} & x_{13} & x_{12} & x_{11} & x_{10} \\ & & & x_{27} & x_{26} & x_{25} & x_{24} & x_{23} & x_{22} & x_{21} & x_{20} \\ & & & x_{37} & x_{36} & x_{35} & x_{34} & x_{33} & x_{32} & x_{31} & x_{30} \\ & & & x_{47} & x_{46} & x_{45} & x_{44} & x_{43} & x_{42} & x_{41} & x_{40} \\ & & & x_{57} & x_{56} & x_{55} & x_{54} & x_{53} & x_{52} & x_{51} & x_{50} \\ & & & x_{67} & x_{66} & x_{65} & x_{64} & x_{63} & x_{62} & x_{61} & x_{60} \\ & & & x_{77} & x_{76} & x_{75} & x_{74} & x_{73} & x_{72} & x_{71} & x_{70} \\ & & & x_{87} & x_{86} & x_{85} & x_{84} & x_{83} & x_{82} & x_{81} & x_{80} \end{array}$$

Fig 2.1 Input bit-matrix **A** of adder tree for $N = 8$ and $w = 8$.

**FULL WIDTH ADDER TREE(FL-AT) AND FIXED WIDTH ADDER TREE(FX-AT):**

A scheme to develop an efficient FX-AT design with truncated input. Use of truncated input in FX-AT offers two fold advantages: (1) area and delay saving within the FX-AT due to reduction in adder-width (by *p*-bits), and (2) creates a scope to optimize other computing blocks appear at the upstream of AT in a complex design. However, the use of truncated input introduces a large amount of error in the FX- AT output which needs to be biased appropriately.

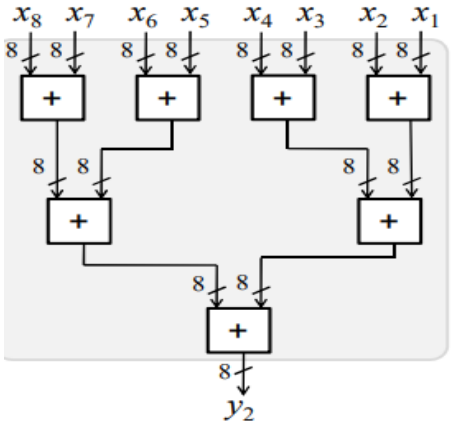


Fig 2.2 (a) Fixed Width Adder tree for A=8

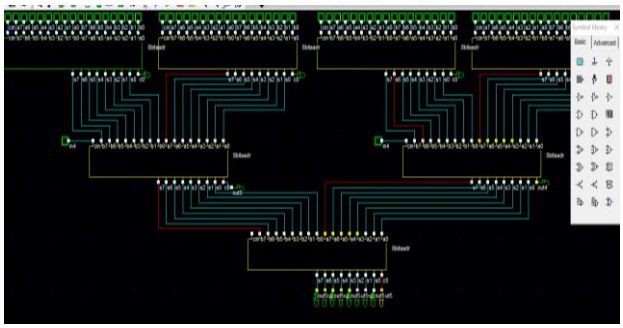

Fig 2.3(b) Design of Fixed width adder tree for A=8 in DCH2

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**TRUNCATED FIXED WIDTH ADDER TREE (TFX-AT):**

Full Width Adder Tree and Fixed Width Adder tree are truncated to get the efficient design and to reduce the CPD mainly. For truncation we need to know how many columns in the matrix are to be truncated. To achieve that we are going to know the estimate the fixed bias by using probabilistic approach.According the formula we are eliminating last 3 columns are chosen as the LSP.For proposed truncated fixed width adder tree we are calculating MSP and adding estimated input to the adder tree by using following formula. output of TFX-AT is expressed as:

$$y = MSP + 2^{p} \cdot \sigma$$
$$\sigma = N/2$$

the fixed-bias for $N$ = 8 and 16 is found to be $\sigma$=4 and 8 . The input bit-matrix of TFX-AT with fixed- bias is shown in Fig.3(a) for $N$ = 8 and $w$ = 8. The binary values of $\sigma$=4 is added to the least significant column of MSP for error-compensation.It can be seen in following figure.

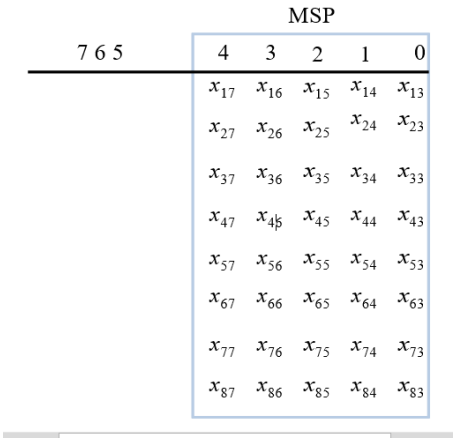


Fig 3.1 The form of matrices in TFX-AT.The design of adder with

5 input bits of matrix A is shown in figure:

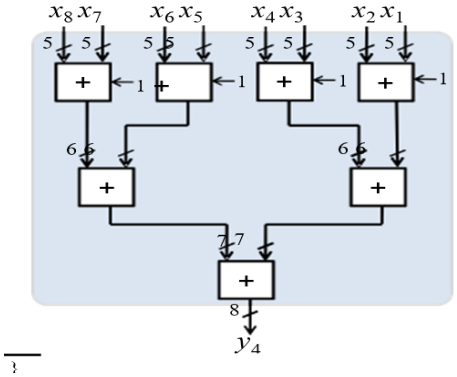


fig 3.2 Design of truncated fixed width adder tree

As when the above picture is observed 5 bit is taken as input and for the error compensation we get LSP N=3, Hence we are removing LSP and adding remaining bits in adder tree with the required adder.

**IMPROVED TRUNCATED FIXED WIDTH ADDER TREE(ITFX-AT):**

In ITFX-AT we are adding half adders and modified half adder which gets the estimated formula to calculated more efficiently.However , it also have estimation formula for MSP.The better efficient AT is ITFX-AT when compared to other adder trees .They are designed according to the usage of RCA. But to improve the fast response RCA is replaced with CSA.When CSA is used with other halfadder and modified adder delay become more.Half adder is represented as A and modified half adder is as A*.And the adder tree is represented as below

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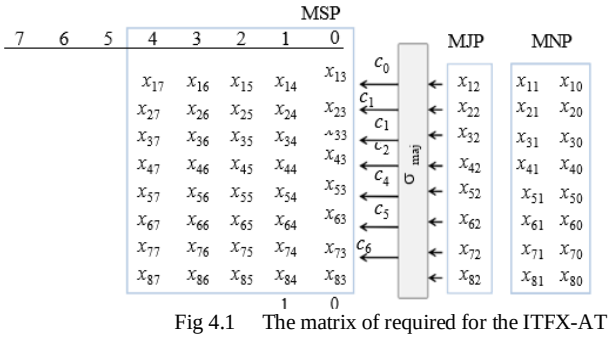


Fig 4.1 The matrix of required for the ITFX-AT

Here in ITFX-AT the carry bits which are added to the MSP is taken from the part of the LSP.Here LSP is divided into MJP(major part) and MNP (minor part).And MJP is added to MSP. To get the aprroximate result

$$\sigma = \sigma major + \sigma minor$$

$$E[MJP] = \left\lfloor \sum_{i=1}^{N} 2^{p-1} x_{i,p-1} \right\rfloor = 2^{p} \left\lfloor \sum_{i=1}^{N} \left( \frac{x_{i,p-1}}{2} \right) \right\rfloor$$

$$\sigma_{major} = \left\lfloor \sum_{i=1}^{N} \left( \frac{x_{i,p-1}}{2} \right) \right\rfloor$$

The quantized value of $\sigma_{minor}$ is estimated as:

$$E[MNP] = \left( \frac{N}{4} \right) \cdot 2^{p}(1 - 2^{-p+1})$$

$$\sigma_{minor} = round\left[ \left( \frac{N}{4} \right)(1 - 2^{-p+1}) \right] \approx \left( \frac{N}{4} \right)$$

$\sigma minor$ =N/4

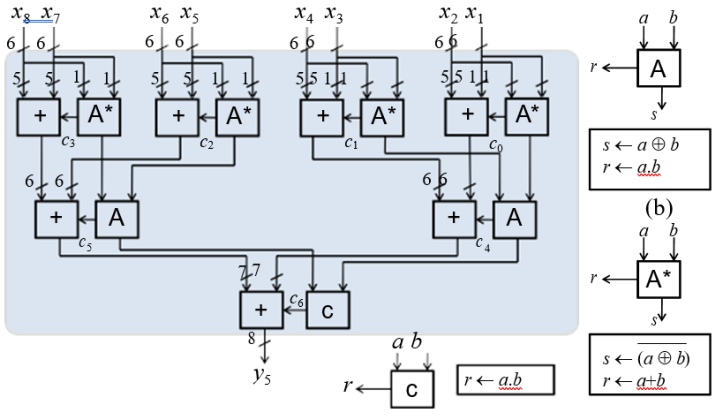


Fig 4.2 Design of ITFX-AT using half adders and modified half adders

As the MSP requires the bias, MJP needs half adder and modified adder to get the approximate adder .MJP'S is gone through required half adder and modified half adder further to get the better output.

**DESIGN OF THE DIFFERENT TYPES OF ADDERS USING DSCH2:**

Here we are using DSCH2 and microwind software technologies to get the critical path delay.As DSCH2 has Symbolizing method to get the complexity in design easier.By this we can excecute it in Verilog too. And we can get the wave forms in microwind technology and other parameters.The result is got for 8,16,32 bits gives the increasing CPD by increasing bits as input. By increasing number of bits there is high difference between critical path delay between CSA and RCA.And as coming to the efficiency TFX-AT is better than ITFX-AT to get the output . Hence TFX-AT is better than ITFX-AT in critical path delay.To know which tree is efficient as well as with lower CPD designing of adder are are done to get output nd CDA in DSCH2 is done.

In designing of adder trees there will be problem in designing in backend.Hence to redue the dsign complexity DSCH2 provides symbolising procedure .By that we can design the adders easily.

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**SYMBOLIZING:**

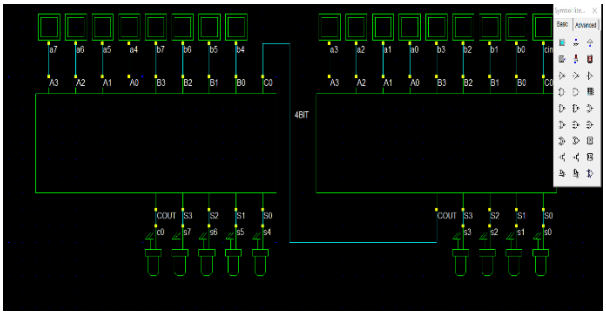

Fig5.1a 8BIT ADDER USING SYMBOLIZED 4 BIT ADDER

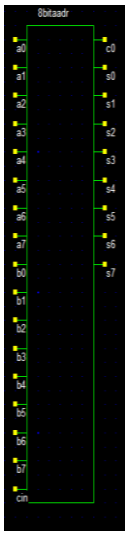

fig 5.1(b)SYMBOLIZED 8 BIT ADDER

As the above figures are observed there the 8 bit adder turns into Symbolized by this caluculation od CDA is also easy.

**DIFFERENT TYPES OF ADDER TREES USING DSCH2 BY REPLACING RCA USING CSA:**

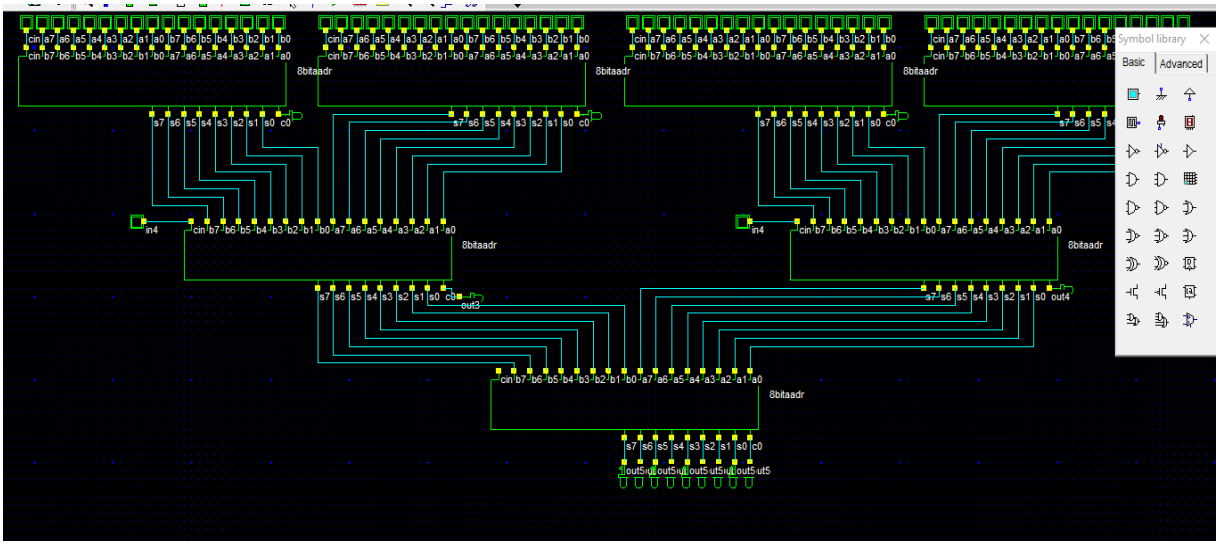

Fig 6.1 8 BIT FX-AT-DT USING RCA

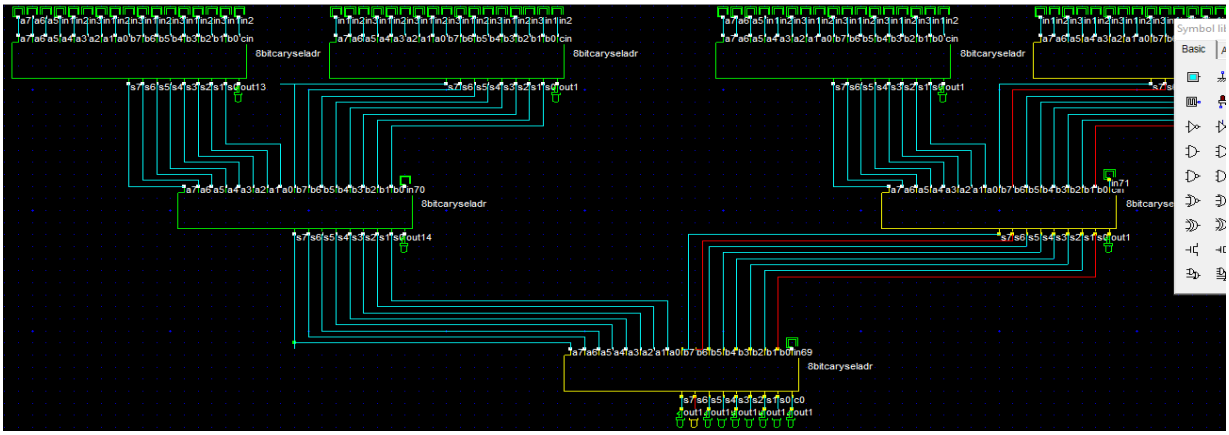

Fig 6.2 8BIT FX-AT-DT USING CSA

**B**y observing the above picture repalcing of RCA with CSA is noticed at the adder tree and by this we calculate the CPD seperately and difference in the CPD is observed.likewise below pictures are designed with CSA to caluculate CPD.

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**SUGGESTED ADDER TREE:**

In truncated adder tree, improved truncated fixed width adder tree is easy to design and get output more easily.However, we are adding half adder and modified adder tree to the improved FX-AT.Those adder slowdown the speed of getting output when CSA is used. Hence, Truncated fixed width adder tree to get low delay.

**HARDWARE TIME COMPLEXITIES:**

As the CSA has extra muxes and adders the area occupied at the hardware is little more than RCA.By following novel techniques and linear DSP algorithms and transforms,By using advanced technologies like 40nm we can reduce the area of CSA at Hardware .

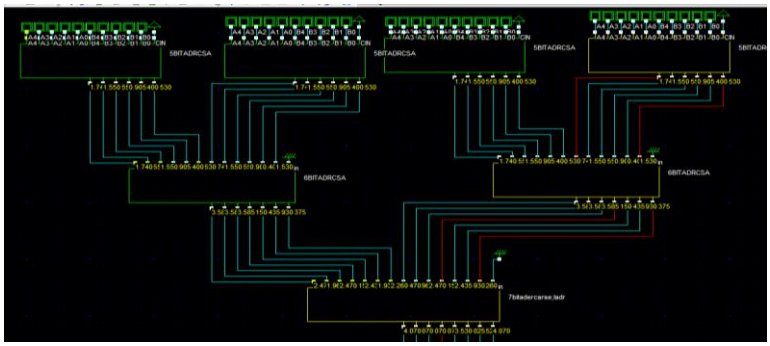

Fig 7.1 8 BIT TFX-AT USING CSA

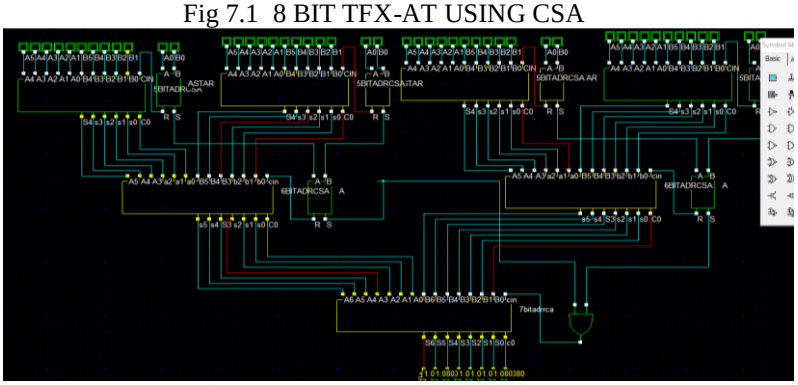

Fig 7.2 8 BIT ITFX-AT USING CSA

By the above pictures we observed the deign of ITFX -AT and TFX AT are done and CDA is caluculate.To caluculate which adder tree is better to get low CDA different types of adder trees are simulated .

## HARDWARE TIME COMPLEXITIES:

As the CSA has extra muxes and adders the area occupied at the hardware is little more than RCA.By following novel techniques and linear DSP algorithms and transforms,By using advanced technologies like 40nm we can reduce the area of CSA at Hardware .As the hardware technology can determined in microwind tool.However it may extended to the hardware to reduce the area by applying different type of algorithms. Microwind unifies schematic entry, pattern based simulator, SPICE extraction of schematic, Verilog extractor, layout compilation, on layout mix-signal circuit simulation, cross sectional & 3D viewer, netlist extraction, BSIM4 tutorial on MOS devices and sign-off correlation to deliver unmatched design performance and productivity.In the future technologies we can reduce the size of the hardware and get the approximate result and with the same CDP.

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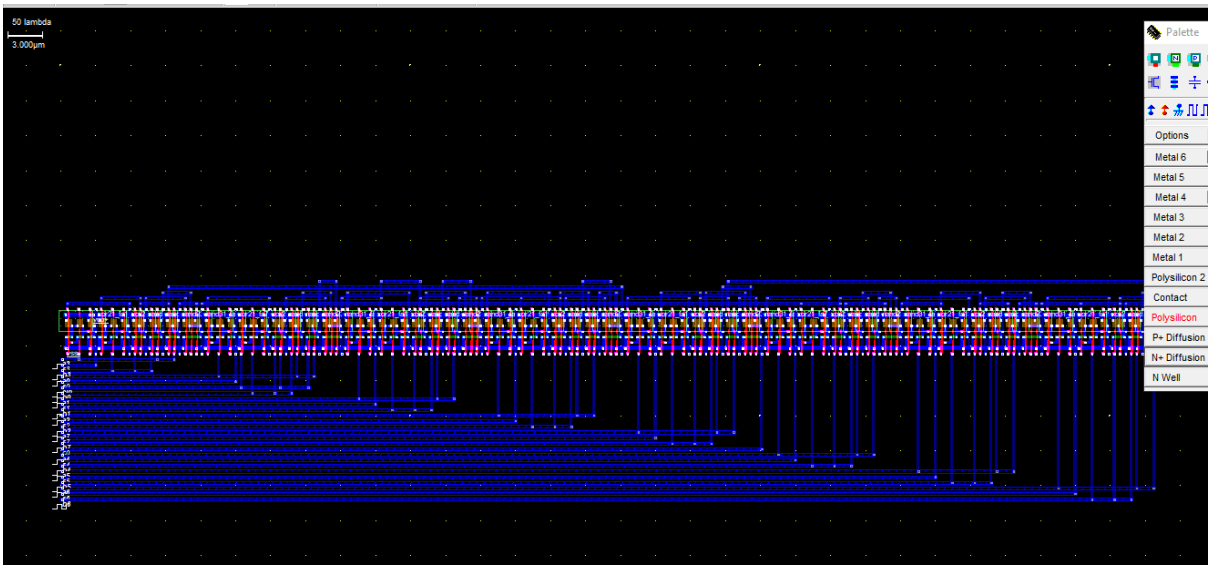


Fig 8.1 SAMPLE DESIGN OF 8BIT ADDER IN MICROWIND WHICH LEADS TO THE BETTER DESIGN IN REAL TIME HARDWARE

These leads to the design of hardware Spiceman in vlsi design technology.And the ouput is also observed in the microwind

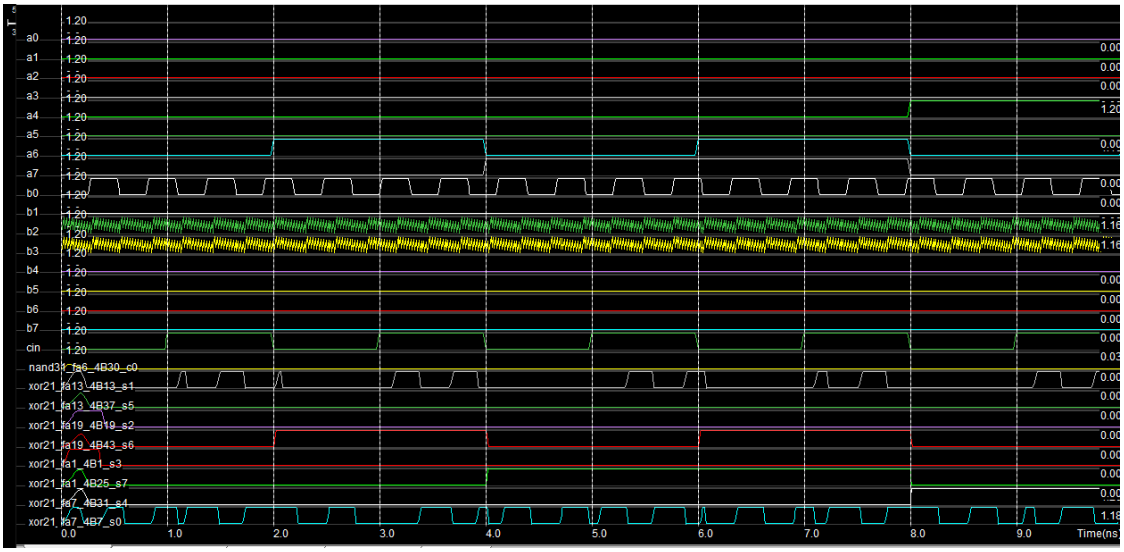


Fig 8.2 RESULT WAVE FORMS IN MICROWIND NANOMETER TECHNOLOGY

**RESULTS:**

| DESIGN | N | W=8 | W=12 | W=16 |
|---|---|---|---|---|
| | | APPROX | APPROX | APPROX |
| FX-AT-PT | 8 | 98.9% | 99.4% | 99.63% |
| | 16 | 98.3% | 99.3% | 99.3% |
| FX-AT-DT | 8 | 99.03% | 99.94% | 99.99% |
| | 16 | 98.4% | 99.86% | 99.99% |
| TFX-AT | 8 | 99.5% | 99.53% | 99.956% |
| | 16 | 99.3% | 99.50% | 99.932% |
| ITFX-AT | 8 | 99.6% | 99.65% | 99.952% |
| | 16 | 99.4% | 99.845% | 99.955% |

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**ERROR ESTIMATES OF PROPOSED DESIGNS AND EXISTING DESIGNS**

| DESIGN | N | CPD(RCA) (ns) | CPD(CSA) (ns) |
|---|---|---|---|
| FX-AT-PT | 8 | 1.23 | 0.84 |
| FX-AT-DT | 8 | 3.97 | 0.98 |
| TFX-AT | 8 | 2.37 | 1.04 |
| ITFX-AT | 8 | 3.08 | 1.08 |

**COMPARISION OF SYNTHESIS RESULTS FROM RCA TO CSA**

## APPLICATIONS:

Multifunctioning of electronic device is the best application of the adder tree .Application of passwords ,securitypatches,encrypted languages etc. In electronic devices like mobiles,laptops we do multitasks with less amount of delay.Interpreters,compilers applications.Image recognition applications likeSharpening images,Editing images via adder trees.Calculating bar codes,QR codes etc.However, In TFX-AT error compensation fixed bias leads to reconstruction of image via WHT transform and sharpens the image with low time delay. We have estimated CPD of all the designs, and the estimated values are also listed. For word-length (8, 12, 16), the proposed ITFX-AT offers (37%, 23%, 22%) and (51%, 30%, 27%) ADP saving over the FX-AT-PT for $N$ = 8 and 16, respectively, and calculate outputs with almost the same accuracy of FX-AT-PT and TFX-AT has better result when we compared to the other when the results are seen it on table.

## CONCLUSION:

In this paper,RCA is replaced with CSA in AT to get lower CPD.As adder tree deals mainly the area and delay in getting the out put.Hence, we undergone ,different types of truncated adder tree .Based on the proposed scheme truncated adder tree .Based on the proposed scheme truncated fixed width adder tree is the best possible way to get the output with the least delay.

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