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# Efficient 8x8 Multiplier Based On Gate Diffusion Input Technique

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## Abstract

Power consumption has become a critical concern in today's VLSI system design. The growing market for fast DSP and multi-core processors has created a demand for low power, area efficient multipliers. A Wallace tree multiplier is an improved version of tree based multiplier architecture. It uses carry save addition algorithm to reduce the latency. This paper aims at additional reduction of power and area using compressors based on Gate Diffusion Input Technique. Full adder designed by GDI technique use only 10 transistors and it is used in compressors. In this paper Wallace tree is constructed using 4:3 and 5:2 compressors. Therefore, minimizing the transistor count make it low power and area efficient.

**Keywords:** GDI , Compressor, Low Power, Area Efficient .



## 1. INTRODUCTION

Arithmetic circuits, like adders and multipliers, are one of the basic components in the design of communication circuits. Recently, an overwhelming interest has been seen in the problems of designing digital systems for communication systems and digital signal processing with low power at no performance penalty.

Designing low power high-speed arithmetic circuits requires a combination of techniques at four levels; algorithm, architecture, circuit and system levels. Digital multipliers are the most commonly used components in many digital circuit designs. They are fast, reliable and efficient components that are utilized to implement any operation. Depending upon the arrangement of the components, there are different types of multipliers available. Particular multiplier architecture is chosen based on the application. The power dissipation in a multiplier is a very important issue as it reflects the total power dissipated by the circuit and hence affects the performance of the device. This paper proposes the Wallace tree multiplier using compressor based on GDI technique.

A multiplier can be divided into three stages: Partial products generation stage, partial products addition stage, and the final addition stage. In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products. The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier. The speed, area and power consumption of the multipliers will be in direct proportion to the efficiency of the compressors. Thus, in order to satisfy the requirement of small area low power high throughput circuitries, this paper provides novel designs of 4:3 and 5:3 compressors with minimum number of transistors. The proposed designs are highly efficient in terms of small area low power and high throughput. The details of the proposed designs are mentioned in detail in the upcoming sections.

## 2. GATE DIFFUSION INPUT TECHNIQUE

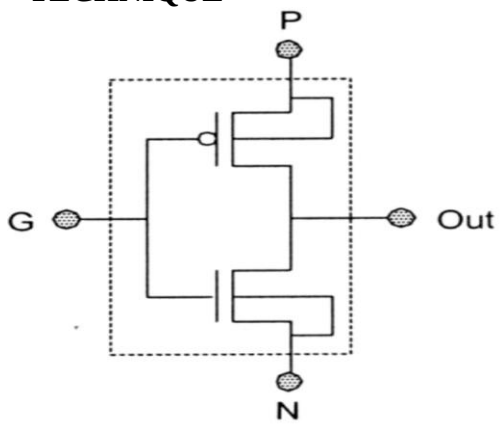


Fig 1. GDI Basic Cell

GDI method is based on the use of a simple cell as shown in Figure 2 [1]. At a first glance the basic cell reminds the standard CMOS inverter, but there are some important differences: (1) GDI cell contains three inputs – G (common gate input of NMOS and

PMOS), P (input to the source/drain of PMOS), and N (input to the source/drain of NMOS). (2) Bulks of both NMOS and PMOS are connected to N or P (respectively), so it can be arbitrarily biased at contrast with CMOS inverter. It must be remarked, that not all the functions are possible in standard P-Well CMOS process, but can be successfully implemented in Twin-Well CMOS or SOI technologies.

Table I shows how a simple change of the input configuration of the simple GDI cell corresponds to very different Boolean-
functions [1]. Most of these functions are complex (6-12 transistors) in CMOS, as well as in standard PTL implementations, but very simple (only 2 transistors per function) in GDI design method.

Table I. Some logic functions that can be implemented with a single GDI cell [1]

| N | P | G | OUT | FUNCTION |
|---|---|---|---|---|
| '0' | B | A | A'B | F1 |
| B | '1' | A | A' + B | F2 |
| '1' | B | A | A + B | OR |
| B | '0' | A | AB | AND |
| C | B | A | A'B + AC | MUX |
| '0' | '1' | A | A' | NOT |

As can be seen in [1], GDI cell structure is different from the existing PTL techniques and has some important features, which allows improvements in design complexity level, transistor counts, static power dissipation and logic level swing.

### 2.1 Full Adder Implementation

In this design the SUM as well as CARRY cell is designed using GDI technique[2].

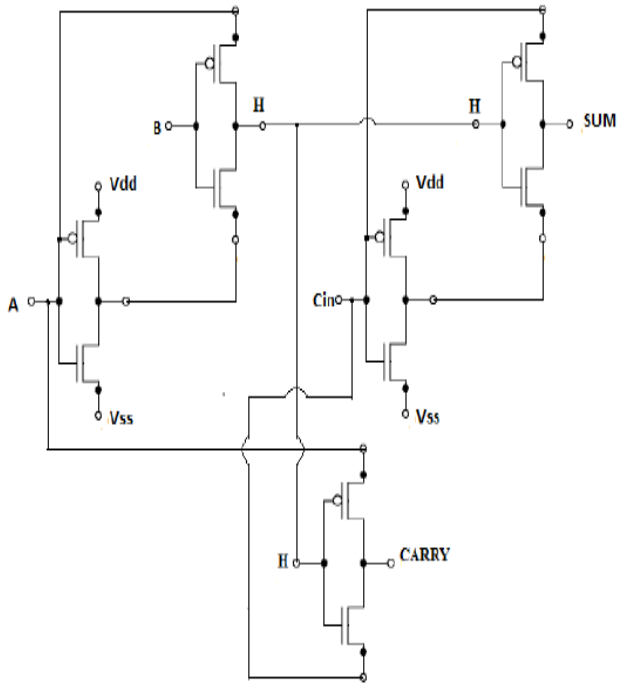


Fig 2. GDI full adder

It needs totally 8 transistors to implement the SUM cell and 2 transistors to design CARRY cell. Firstly H function i.e. XOR is implemented using GDI technique and then using this H function as input, the overall SUM as well as CARRY cell is been implemented.

## 3. COMPRESSOR

Compressors are mostly used in multipliers[3] to reduce the operands while adding terms of partial products. With use of compressors the partial product can be reduced.

### 3.1) 4:2 Compressor

The 4:2 compressor[4] structure actually compresses five partial products bits into three. The architecture is connected in such a way that four of the inputs I1, I2, I3, I4 are coming from the same bitposition of the weight j while one bit Cin is fed from the neighboring position j-1(known as carry-in). The outputs of 4:2 compressor consists of sum. Carry and Cout bit.

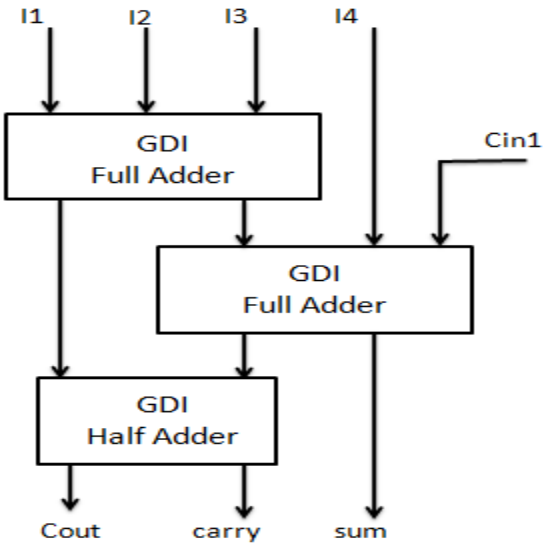


Fig 3. 4:2 compressor using GDI adder

Figure 3 shows the block diagram of 4-2 compressor. A 4-2 compressor can be built using two 3-2 compressors(full adders)and one half adder.

### 3.2) 5:2 Compressor

The 5:2 compressor[4] structure actually compresses seven partial products bits into three.

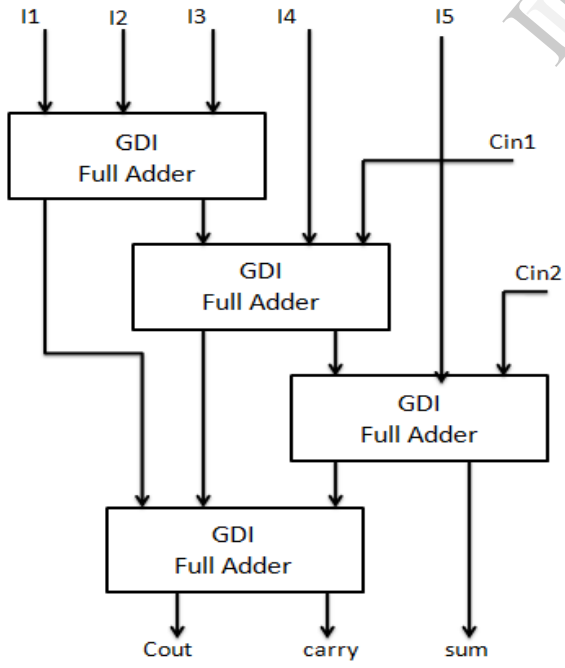


Fig 4. 5:2 compressor using GDI adder

The architecture is connected in such a way that four of the inputs I1, I2, I3, I4, I5 are coming from the same bit position of the weight j while one bit Cin1 and Cin2 is fed from the neighboring position j-1 and j-2 (known as carry-in). The outputs of 5:2 compressor consists of three sum. Carry and Cout bit. Figure 4 shows the block diagram of 5-2 compressor. A 5-2 compressor can be built using four 4-2 compressors(full adders).

## 4. MULTIPLIER

A basic multiplier can consist of three parts (i) partial product generation (iii) partial product addition and (iii) final addition [9]. A multiplier essentially consist of two operands, a multiplicand "Y" and a multiplier "X" and produces a product ". In the first stage, the multiplicand and the multiplier are multiplied bit by bit to generate the partial products product The second stage is the most important, as it is the most complicated and determines the speed of the overall multiplier to add these partial product to generate the Product "P". This paper will be focused on the optimization of this stage[5], which consists of the addition of all the partial products. If speed is not an issue, the partial products can be added serially, reducing the design complexity. However, in high-speed design, the Wallace tree construction method is usually used to add the partial products in a tree-like fashion in order to produce two rows of partial products that can be added in the last stage. Although fast, since its critical path delay is proportional to the logarithm of the number of bits in the multiplier, the Wallace tree introduces other problems such as wasted layout area and increased complexity. In the last stage, the two-row outputs of the tree are added using any high-speed adder such as carry save adder to generate the output result.

## 5. WALLACE TREE MULTIPLIER

A fast process for multiplication of two numbers was developed by Wallace [6]. Using this method, a three step process is used to multiply two numbers; the bit products are formed, the bit product matrix is reduced to a two row matrix where sum of the row equals the sum of bit products, and the two resulting rows are summed with a fast adder to produce a final product.
In the Wallace Tree method, three bit signals are passed to a one bit full adder ("3W") which is called a three input Wallace Tree circuit[5], and the output signal (sum signal) is supplied to the next stage full adder of the same bit, and the carry output signal thereof is passed to the next stage full adder of the

same no of bit, and the carry output signal thereof is supplied to the next stage of the full adder located at a one bit higher position[5].

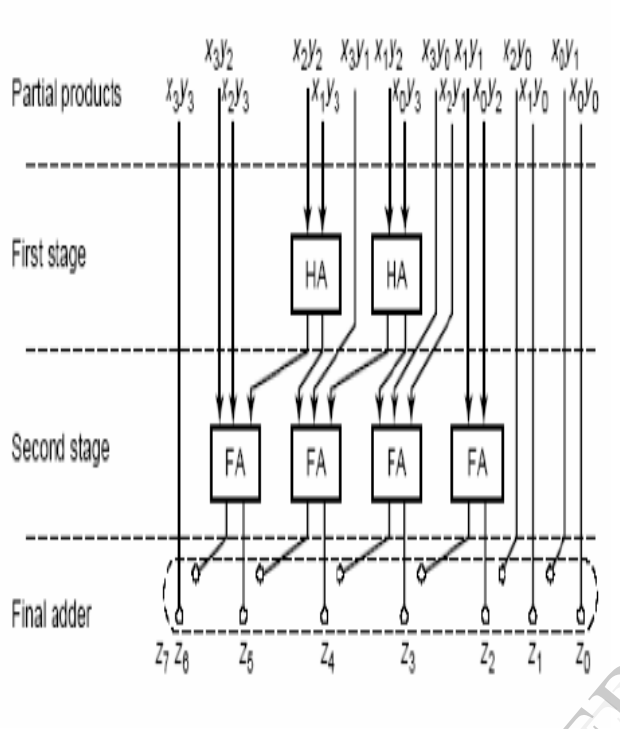


Fig 5. Wallace tree Multiplier

A 16-bit multiplier is constructed by using Wallace tree architecture. The architecture has been shown in Figure 6. Partial products are added in five stages. Adders and different compressors are used to minimize the stage operations[7]. Compressors and adders are used carefully so that minimum number of outputs would be generated. Consider the column number eight where eight bits are added at the first stage. These eight bits could be added by using two 4-2 compressors, but that will generate six (three of each compressor) outputs, instead of this we have used one 5-2 compressor that add seven bits and generate three outputs and one bit is promoted to next stage that eventually decrease the number of bits for the next stage. Thus by using minimum number of adders/compressors partial products are added without compromising the number of bits generation for the next stage operation.

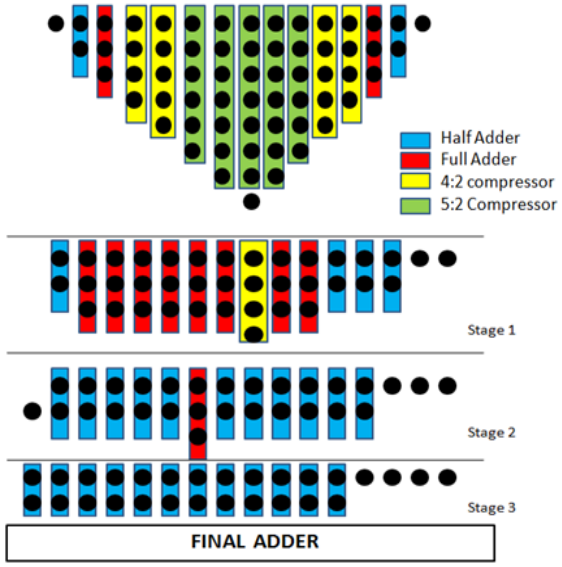


Fig 6. Wallace tree Architecture using compressors

This architecture helps to reduce the partial product stages. Only in 3 stages the final products are given to Final adder which perform high speed addition and give the final results.

## 6. PERFORMANCE AND COMPARISON

All the adders, compressors and multiplier are designed and simulated in Cadence Virtuoso 180nm technology. Their performances are measured in different supply voltages such as 3V at 100MHz. The delay was measured from 50% of the input voltage swing to 50% of the output voltage swing. Mainly three parameters are compared in this analysis; they are Delay, Power Consumption and no. of transistors used in design. The comparison is done with CMOS technology. Use of higher order compressors reduces multiplication delay and power consumption and area. These compressors are more effective for high order multiplication. The performance results are shown in Table II.

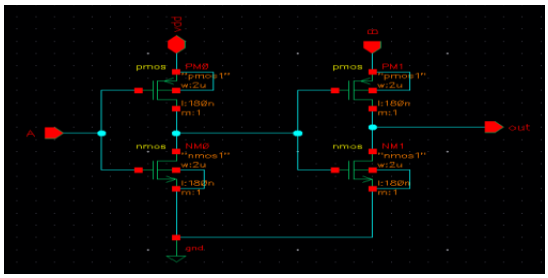

Figure 7. AND Gate using GDI Technique.

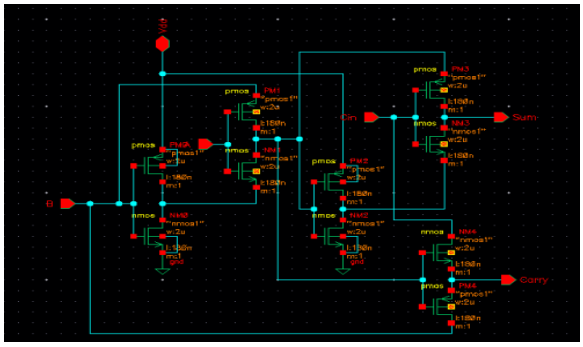

Figure 8. GDI Full Adder

8x8 mutiplier based on GDI technique shown in below figure.It contain 64 AND gate and series of Half Adder, Full Adder ,4:3 and 5:3 compressors to reduce the partial product.

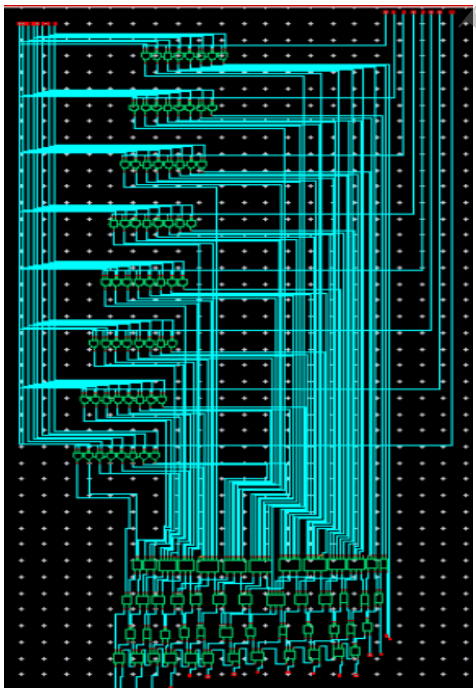

Figure 9. 8x8 GDI Multiplier Schematic

Table II Simulation Result using Cadence

| | CMOS | | | GDI | | |
|---|---|---|---|---|---|---|
| Module | Power | Delay | #Transistors | Power | Delay | #Transistors |
| AND Gate | 10.11uW | 5.112ns | 6 | 7.19uW | 5.08ns | 4 |
| Full Adder | 97.84 uW | 5.12ns | 28 | 66.25uW | 5.05ns | 10 |
| 4:3 Compressor | 449.7uW | 5.091ns | 70 | 403.5uW | 5.16ns | 28 |
| 5:3 Compressor | 527.5uW | 5.162ns | 112 | 442.7uW | 5.015ns | 40 |
| 8x8 Multiplier | 19.42mW | 5.98ns | 2108 | 17.03mW | 5.85ns | 960 |

## 7. CONCLUSION

The Wallace tree multipliers can be solved & analyzed using a new modified method of Wallace tree construction using compressors based on GDI technique.The modified tree has a less no. of transistors which requires less area. This modified design of multiplier which consist of 5:2 compressor, 4:2 compressor, full adders and reduced no. of half adder and reduces the complexity and reduce the time delay. The proposed Multiplier using Compressor has 54.43% less area and it consume 13.21% less power. The delay is almost same in both techniques. The limitation in this technique is that first pulse may be garbage output. So first output pulse is not considered as result.Hence for low size and low power the proposed Multiplier is suggested.



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