Dynamic Fuzzy-Controlled Voltage Scaling with In-Situ Detectors in Commercial FPGAs

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***Abstract* -Energy proportional computing (EPC) enables the allocation of energy to tasks depending on computational demands. Computing at full speed and then dynamically turning off modules when they are not required for a period of time can be used to obtain EPC and it is an alternative to voltage scaling techniques in which the computation is slowed down. This project investigates the viability of physical power gating FPGA devices that incorporate a hardened processor in a different power domain. The run-time power gating approach is applied to FPGA devices that incorporate a hardened multi-processor. power down followed by a full reconfiguration can be controlled by the embedded processor autonomously is shown. The time that the FPGA must remain in power-on state is feed and remaining power is saved when the required voltage is lowered below critical level. These modules take into account the overheads of controlling the programmable voltage regulators interfaced to the FPGA and the overhead of the reconfiguration needed when the device must be returned to the active state.**

INTRODUCTION

ENERGY and power efficiency in field programmable gate arrays (FPGAs) has been estimated to be up to one order of magnitude worse than in ASICs and this limits their applicability in energy constraint applications. Since FPGAs are fabricated using CMOS transistors power can be divided into two main categories, dynamic power and static power. As a result, voltage scaling is often combined with frequency scaling in order to compensate for the variation of circuit delay. Essentially, voltage and frequency scaling attempts to exploit performance margins so that tasks complete just in time obtaining power and energy savings. An example of this is dynamic voltage and frequencyscaling (DVFS) which is a technique that uses a number of pre-evaluated voltage operational points to scale power, energy and performance. With DVFS, for worst case since it operates in an open-loop configuration. For this reason, in adaptive voltage scaling (AVS) with in-situ detectors run-time monitoring of performance variability in the silicon is used together with system characterization to influence the voltage closed-loop configuration. Addressing these issues the contributions of this work can be summarised as follows:

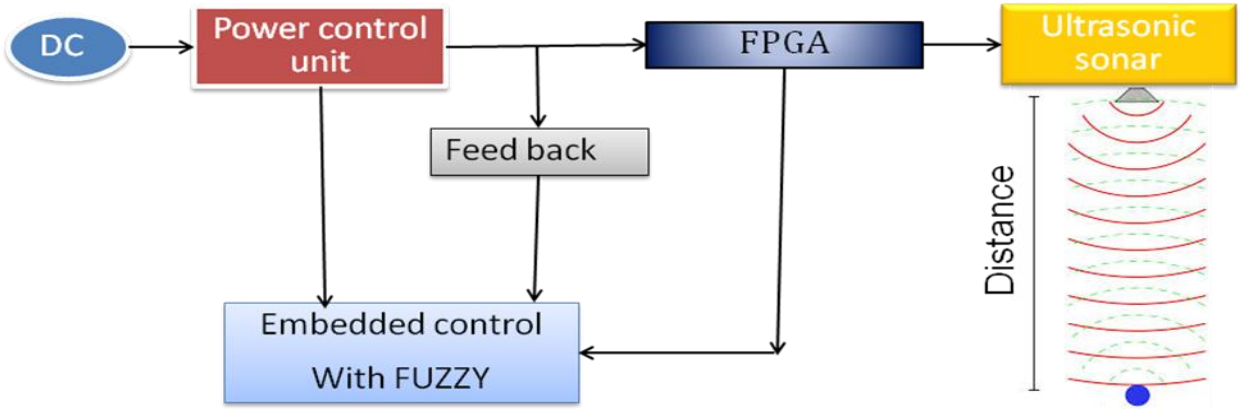
1.We present a power adaptive architecture based on in-situ detectors and adaptive voltage scaling suit-able for commercially available FPGAs.
2.We present fuzzy algorithm in control unit for control the power
3.We demonstrate the power and energy savings possible.

RELATED WORK

In order to identify ways of reducing the power consumption in FPGAs, some research has focused on developing new FPGA architectures implementing multi threshold voltage techniques, multi-Vdd techniques and power gating techniques.Other strategies have proposed modifying the map and place&route algorithms to provide power aware implementation. This related work is targeted towards FPGA manufacturers and tool designers to adopt in new platforms and design environments. On the other hand, a user level approach is proposed in. A dynamic voltage scaling strategy for commercial FPGAs that aims to minimise power consumption for a giving task is presented in their work. In this methodology, the voltage of the FPGA is controlled by a power supply that can vary the internal voltage of the FPGAs.

A dynamic voltage scaling strategy is proposed to minimise energy consumption of an FPGA based processing ele-ment, by adjusting first the voltage, then searching for a suitable frequency at which to operate. Significant savings in power and energy are measured as voltage is scaled from its nominal value of 1.2 V down to its limit of 0.9 V. In this paper we present the application of in-situ detectors to commercial FPGAs that deploy arbitrary user designs.. During testing, devices that can maintain nomi-nal performance at 0.9 V are programmed with the voltage identification bit set to 1. A board capable of using this feature can read the voltage identification bit and if active can lower the supply to 0.9 V reducing power by around 30 percent.

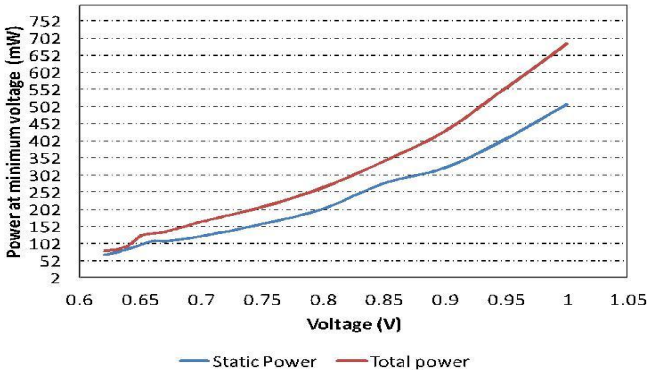
BLOCK DIAGRAM



DC can be used to give the input voltage and the FPGA is used to allocate the required voltage for the correspondent process.This FPGA says the required voltage to embedded processor.Using of fuzzy is an closed loop logic and it allocates the power and it gives to the power control unit. Power control unit is to reduce the voltage and gave the voltage to FPGA. FUZZY can check the allocating voltage by feedback signal. In this the selection process is ultrasonic sonar here piezo crystal is used to produce the ultra sonic waves to the object and it reflect to the sonar and reflection distance is detect by sensor.

FUZZY LOGIC

Fuzzy logic is a superset of conventional (Boolean) logic that has been extended to handle the concept of partial truth – truth values between"completely true" and "completely false". In fuzzy logic the truth of any statement becomes a matter of degree.fuzzy logic is adopted because of its easily modeling and calculating.



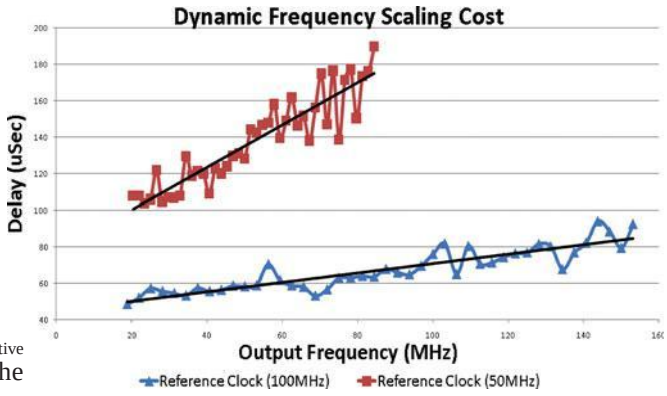
Notice that we need to consider this division between T_{active} and T_{total} because if we simply consider that energy is the multiplication of total time by power we will be assuming that a system using a faster clock will use zero power once the computation completes and static power or leakage is reduced to zero. For example a working frequency of 91 MHz requires 0.8 volts and T_{active} is 10.9 ms at which point only static power remains until the total time of 26.3 ms is reached.

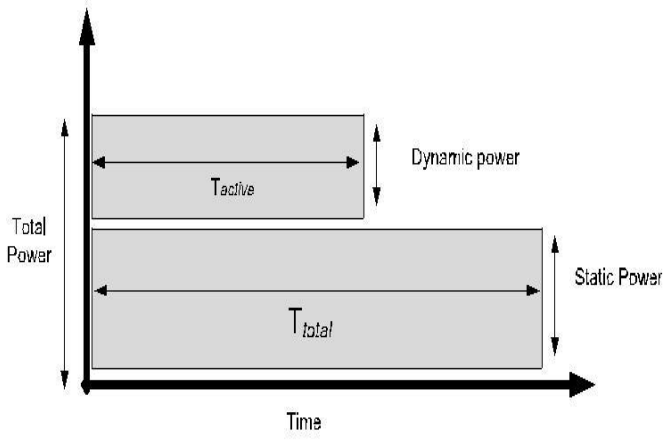
IN-SITU DETECTION LOGIC

In-situ detector is used to produce new adaptive netlist.

ENERGY ANALYSIS

The paper has shown the important reduction of power that can be achieved with the power adaptive flow. An important consideration is how this relates to energy savings. Energy reductions will not be achieved if power reduction implies an equivalent increase in computational time. It is energy that limits battery run time or increases the running costs of a high performance computing centre so energy analysis is required to validate the potential of the proposed techniques. For this experiment we have assumed a task that needs 10^6 cycles to complete and which at the minimum valid frequency of 38 MHz will need 26.3 ms to complete. As the frequency and voltage increases the active computation time defined by T_{active} decreases.





Power distribution for energy analysis.

Freq	Original Energy	Elongate Energy	Description
40 MHz	15.05 mJ	2.24 mJ	Highest energy efficient point
80 MHz	14.92 mJ	4.85 mJ	Nominal performance point
145 MHz	N/A	14.63 mJ	Highest performance

CONCLUSION

This paper has presented a closed-loop variation-aware adaptive voltage scaling in commercial FPGAs. The integration of in-situ detectors coupled to the critical paths of the design creates a robust architecture. Although the FPGA devices employed have not been validated by the manufacturer at below nominal voltage operational points, the investigation shows that savings approaching one order of magnitude are possible by exploiting the margins and overheads available in the devices. The savings in energy are comparable to those observed in power with above 85 percent less energy at the highest energy efficient point This should generate a new design in the form of adaptive voltage scaling (AVS) that can help address the energy and power challenges that current and future chips face.

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