# Driver Configurations for Low-Power and High-Speed Applications

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***Abstract:The increasing prominence of portable systems and the need to limit power consumption (and hence, heat dissipation) inveryhigh density ULSI chips have led to rapid and innovative developments in low-power design during the recent years.In most of the cases, therequirements of low power consumption must be met along with equally demanding goals of high chip density and high throughput. The BiCMOS technology that combines the low-power consumption and high packing density of CMOS with high- speed and high- output drive of bipolar devices has proven to be excellent for portable and non- portable applications. This paper states the driver configurations for low-power, high-speed and high driving capability applications.***

## 1. INTRODUCTION

Due to the advancement in technology in terms of achieving high packing density, CMOS technology is preferred than Bipolar technology. But this suffers from output current levelsin turn affecting thedriving capability. The driving capability plays an important role in driving more number of devices without degrading the logic levels.In characterizing digital circuits, fan out is an important electrical parameteralong with propagation delay, power dissipation, riseand fall times. The driving capability can be achieved only with bipolar devices. If the whole design isimplemented with bipolar technology, we can achieve high driving capability but at the cost of power dissipation. Hence, Bipolar-CMOS circuits are designed to fill the performance gap between CMOS and bipolar circuits merging CMOS and bipolar devices on a single monolithic structure to meet the demand of high- drive capability and low-power dissipation.The methodologies which are used to achieve low power consumption in digital systems span a wide range, from device/process level to algorithm level. Some of the techniques to achieve low-power and high speed arediscussed in the next section.

## 2. DRIVER CONFIGURATIONS

There are three generic types of drivers in the Bi-CMOS logic circuit family –the common emitter (CE), the gated-diode (GD), and the emitter-follower (EF). Each of these drivers uses a fully ComplementaryBi-CMOS technology, with the existence of both the types of bipolar transistors.

*Problems with the existing driver configurations:*

Common Emitter configuration suffers from additional delays and static power dissipation.Gated Diode offersrestriction of the output voltage swing from ($V_{DD}$-$V_{BE}$) to $V_{BE,}$ lack of symmetry between rise time and fall times.Emitter Follower provides partial output voltage swing.

*Full swing with shunting devices*

Bi-CMOS digital circuits exhibit partial output voltage swing. Gated diode and emitter follower suffer from this short coming so we go for shunting techniques, which uses shunting networks such as a simple resistor, a MOSFET or a CMOS positive feedback circuitry. These techniques introduces a cross over current which leads to power dissipation as well as slow down the pull up or pull down transient response and finally reduces the speed of the circuit. These problems can be solved by increasing the resistance value at the expense of a longer time to achieve a full output voltage swing.

Limitations of Full swing Complementary MOS/Bipolar logic circuit are degradation of system performance, slower switching period and charge sharing problem. Full swing Complementary MOS/Bipolar logic circuit with feedback suffers from overall circuit delay because of its bulk circuitry.

## 3.ADVANCED DRIVER CONFIGURATIONS

This section introduces the novel BiCMOS circuit which involves merging of Bipolar and CMOS devices to achieve enhanced speed performance by reducing the area occupied by the device and a BiCMOS circuit which uses bootstrapping to achieve a fast rail-to-rail output swing. First, we present a qualitative description of the merged BiCMOS driver circuit operation during low-to-high and high-to-low transition. Second, we describe the bootstrap circuit model.

### MERGED BiCMOS INVERTER

The conventional BiCMOS circuit and advancedMBiCMOScircuit are shown in fig. 1(a) and 1(b) respectively. The MBiCMOSuses a merged PMOS/NPN device, where the PMOS and NPN devices for both the pull-up and pull-down networks are merged together. It operates at a power supply-voltage of $V_{DD}$=3.0V and $V_{CC}$=3.3V.

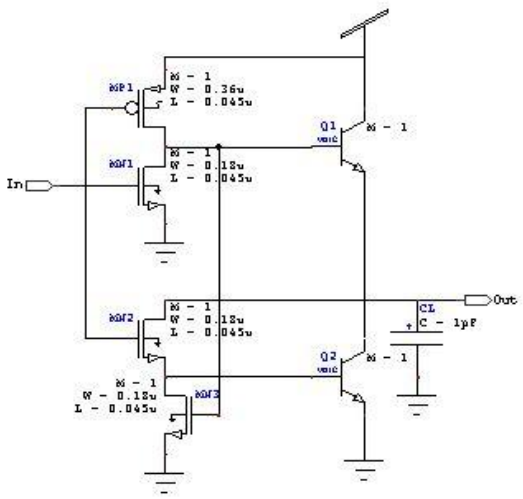


Fig. 1(a) Schematics of conventional BiCMOS design

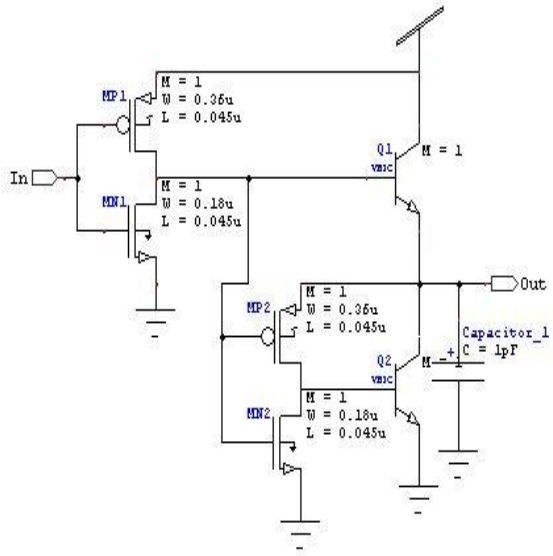


Fig. 1(b) Schematics of MergedBiCMOS circuit

When there is a high to low transition (pull-up) at the input, transistor MP1 turns on and MN1 turns off. At the same time, the drain current from MP1charges up the node B1 to $V_{DD}$ and biases Q1 into active region; hence the output node is pulled up to ($V_{DD}$-$V_{BEon}$). In addition a high voltage at node B1 leads to the conduction of MN3 and turns off MP2 in the pull-down network, thereby forcing Q2into its cut-off state.

Now consider that the input transition is from low to high (pull-down) which triggers MN1 into its on-state and MP1 into its off-state and hence B1 will be at ground potential. Consequently, transistor MP2 conducts, thereby biasing Q2 into its active region. Hence the output node will be pulled down to a low level. The merged BiCMOS has symmetrical pull-up and pull-down sections, thus it gives equal rise and fall times.

## BOOTSTRAPPED BiCMOS INVERTER

The bootstrapped BiCMOS inverter (BS-BiCMOS) had shown in the fig.1(c) uses the bootstrapping technique to pull up the output voltage to $V_{DD}$ and the transient saturation technique to pull down the output voltage to ground. It operates at a power-supply voltage of 1.5V and gives a transient voltage swing of 1.1V.

When the input voltage changes from low-to-high (pull-down), Pbs turns on and charges up Cbs to $V_{DD}$. The transistor Pb1 is off while Nb1 conducts and depletes the base charge of Q1. Meanwhile transistor Pb2 turns on, but Nb2 turns off. Since the output is initially high, Pb3 remains on, while Nb3 remains off for a while. Hence current flows through transistors Pb2 and Pb3 into the base of Q2, causing it to saturate until the output voltage is pulled down to a low value.When this occurs Pb3 turns off via the feedback inverter.

Now, consider the high-to-low transition (pull-up), Pb1 turns on and Nb1 turns off. The base of Q1 is bootstrapped to a value above $V_{DD}$through the bootstrapping capacitance Cbs. The output voltage is subsequently charged up to a value greater than the ($V_{DD}$-$V_{BE\,(Q1)}$) and gradually pulled up to $V_{DD}$ via Pfb.

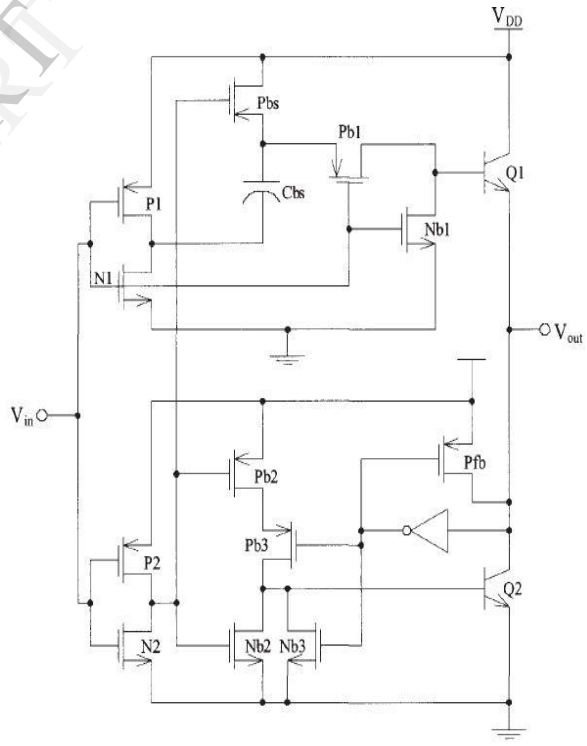


Fig.1 (c) BS-BiCMOS Inverter

## 4. PERFORMANCE RESULTS

In this section, we validate the performance of the advancedBiCMOS circuits through HSPICE simulation and compare their performance with previous circuits. We compare the average power dissipation, delay performance and fan-outof Merged BiCMOS inverter with the

conventional BiCMOSinverter. All the simulations use BJT and MOS transistor parameters of TSMC45nm process technology. The MOS transistors are all the same size except the PMOS pull-up is twice as large the NMOS pull-down i.e. $w_p$=0.36□m, $w_n$=0.18□m and for bootstrapped BiCMOS the size of PMOS and NMOS devices is same i.e. $w_p$=$w_n$=1□m .

The merged BiCMOS inverter is simulated using transient analysis to verify the $V_{OH}$ value with $V_{DD}$= 3.3V and $V_{CC}$=3.0V.The comparison table for the various driver configurations is shown in Table 1.

Table 1:Comparison of different driver configuration with 45nm technology

| TYPE OF CIRCUIT | DELAY (ns) | AVG. POWER (□W) | FANOUT | VOLTAGE SWING(V) |
|---|---|---|---|---|
| CONVENTIONAL BiCMOS | 3.4528 | 1080 | 40 | 1.36 |
| FS-BiCMOS | 2.304 | 17.89 | 89 | 2.32 |
| MBiCMOS | 2.845 | 7.812 | 31 | 1.22 |
| FS-MBiCMOS | 3.279 | 50.54 | 38 | 1.73 |
| BOOTSTRAPPED BiCMOS | 0.3914 | 36.07 | 21 | 1.11 |

We compare the delay performance of our circuit at $V_{DD}$=3.0V and $V_{CC}$=3.3V to the conventional BiCMOS inverter with the load capacitance of 1pf. From the table shown above, it is clear that the merged BiCMOS exhibits better delay performance than the conventional BiCMOS inverter operating at the same power supply voltage.

A 1.5V full-swing BiCMOS circuit using bootstrapping technique enhances the circuit performance. It is observed that the BS-BiCMOS is much faster configuration with a smaller delay due to the presence of the bootstrapping capacitor Cbs. It has an overall propagation delay of approximately 0.3914ns. It is also observed that the bootstrapped BiCMOS circuit operating at 1.5V supply voltage produces a full voltage swing of approximately 1.11V. Hence it is useful for the applications requiring full output voltage swing.

The average power has been simulated at 0.5MHz frequency with a load capacitance of 1pF for supply voltage of 3V. Out of all the driver configurations the MBiCMOS has the lowest power dissipation which is approximately 7.812□W.

The output driving capability(Fan out) is measured by taking into account a two input NAND gate operating at a supply-voltage of 3.0V. The input gate current of this gate is 6.546□A. After measuring the output currents of all the driver configurations it is found that the FS-BiCMOS circuit is the best suitable for the applications requiring high driving capability.

## 5. SUMMARY

BiCMOS merged the low power dissipation and high packing density features of MOS devices with the high drive capability of bipolar devices. One problem with the BiCMOS is the limitation of output voltage swing. In this paper we presented a novel BiCMOS circuit which is suitable for obtaining full swing at the output. All the performance comparisons are done at power supply voltages of 3.0V. Hence for low-power applications Merged BiCMOS offers a better performance than any other circuit, whereas for high speed applications the Bootstrapped BiCMOS is the best driver configuration. The FS-BiCMOS has the high driving capability. The simulation waveforms for the advanced driver configurations were shown in Fig .5(a) and Fig. 5(b) respectively.

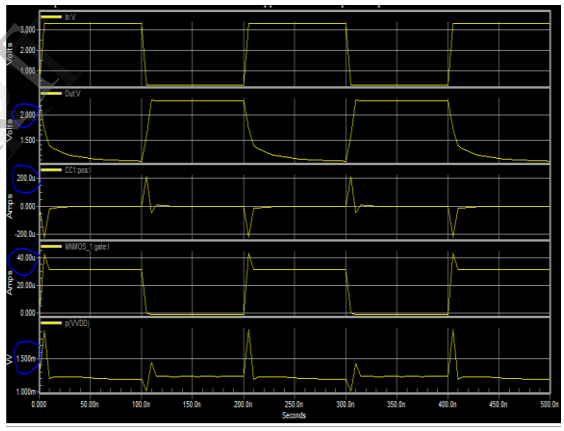

Fig. 5(a) Simulation waveforms for merged BiCMOS inverter

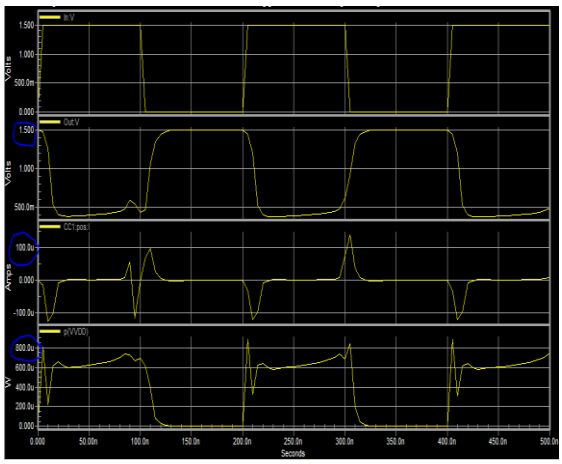

Fig.5 (b) Simulation waveforms for BS-BiCMOS

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