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# Double Gate Tunnel Field Effect Transistor: Review Paper

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***Abstract :-*** **Over the last three decades, Complementary metal oxide semiconductor (CMOS) technology developed at unprecedented speed towards a point such that nobody in developed countries can live without that technology. The main building block of CMOS technology is metal oxide semiconductor field effect transistor (MOSFET). To get the low power and high speed technology, device dimension was required to reduce and it was possible. As a result packaging density was increasing and was satisfying the Moore's statement. But now the trend of decreasing the dimension has reached to its limit. The further reduction of dimension is increasing leakage current. So to combat with these limitations researchers are forced to investigate innovative devices for future technology.**

***Keyword:- Complementary metal oxide semiconductor (CMOS), Short Channel Effects (SCE), metal oxide semiconductor field effect transistor (MOSFET), Double gate tunnel Field effect transistor (DGTFET).***

## 1.1 INTRODUCTION

Over the last three decades, Complementary metal oxide semiconductor (CMOS) technology developed at unprecedented speed towards a point such that nobody in developed countries can live without that technology. To get higher speed and packaging density short channel length was required and it was possible. But recently, shorter channel length is posing different kind of undesired effects like drain induced barrier lowering and $V_T$ roll-off. To avoid this Short Channel Effects (SCE) and to maintain constant electric field in the oxide, the gate oxide thickness is scaled in proportion to channel length (*L)* and width (*W)*. However as oxide is scaled, tunneling leakage currents through the oxide starts to increase. LO et al. [1] showed that the silicon oxide can be thinned down to slightly below 2 nm before the leakage current becomes large enough to be unacceptable. Since the tunneling takes place not only in the inversion layer, but also in the accumulation region where the gate overlaps the source and drain, this later component too becomes significant as the devices are scaled down. By using physically thicker gate insulating material with dielectric constant, κ, higher than that of silicon-oxide has been suggested as a possible solution to reduce the direct tunneling through the insulator [2-3]. However, the thickness cannot grow unlimited as 2D effects in the thicker insulator start to interface with scaling. The short channel performance degraded due to the fringing fields from the source drain regions which become non-negligible as the thickness-to-length aspect ratio increases [4-5].

## 2 TUNNEL DEVICES

Device based on tunneling mechanism is not a new concept. For several years many researchers are trying to make technologically suitable the tunneling devices. Since the probability of tunneling depends on tunneling barrier height and width, this devices show a nearly temperature independent I-V characteristics which allow reliable operation of devices at both low and high temperatures. Thus three terminal band-to-band tunneling transistors based on gate induced drain leakage current resulting from tunneling in gate-source overlap regions [11, 12] and tunneling from schottky barriers have been proposed. While the former failed to meet the International Technology Roadmap for Semiconductor (ITRS) requirement in term of $I_{ON}$ , the later has high leakage current. Gate controlled negative differential resistance (NDR) was further observed in gated p-n junctions in silicon-on-insulator based on forward biased Esaki tunneling. Then Vertical tunnel field effect transistor is demonstrated by Bhuwalka and shows its utility as a Nano scale alternative device . Double gate tunnel Field effect transistor (DGTFET) is considered to increase the tunneling current as two tunneling junctions are formed. Low sub threshold swing and high $\frac{I_{ON}}{I_{OFF}}$ current ratio makes DGTFET suitable for low power application but the low driving current is still an obstacle for the success of the device.

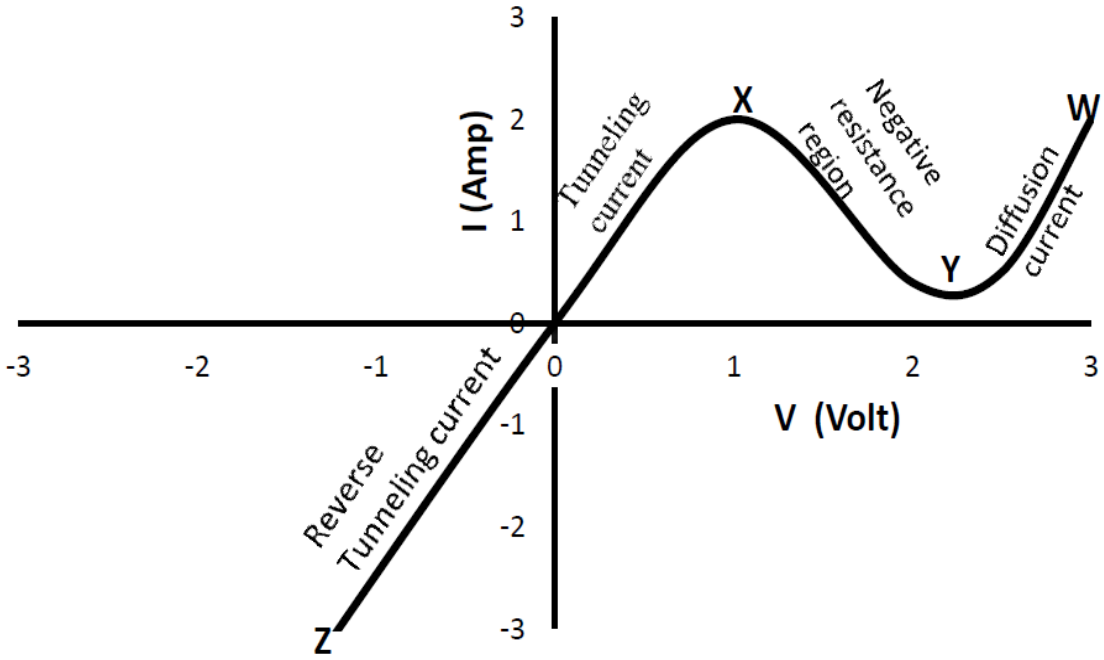



Figure 1 I-V Characteristic of P-N Junction with Tunneling Operation.

## 3 TUNNELING OPERATION

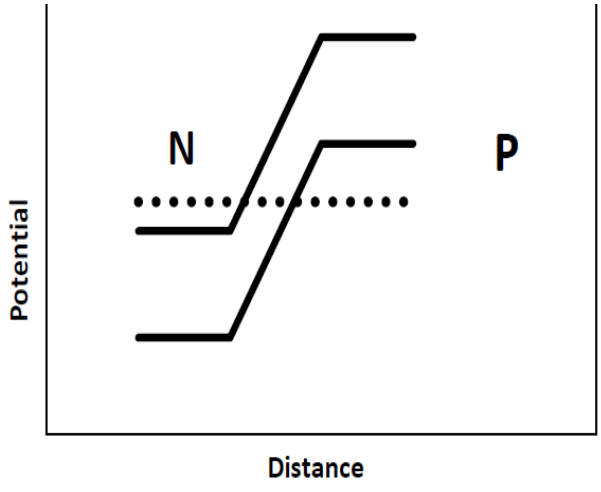
In this section by band diagram, tunneling mechanism in simple p-n junction is explained. We know that in degenerately doped semiconductors, the Fermi level is in the conduction band of a degenerately doped n-type material and in valance band of a degenerately doped p-type material. Thus even at T=0 K electrons will exist in the conduction band of n-type material and holes will exists in the p-type material. The depletion region decreases as the doping increases and may be in the order of approximately 100 Å. The potential barrier is considered as triangular and it exists across the depletion region. Barrier width is small and electric field in the space charge region is large, thus a finite probability exists that an electron may tunnel through the forbidden band from one side of the junction to other.

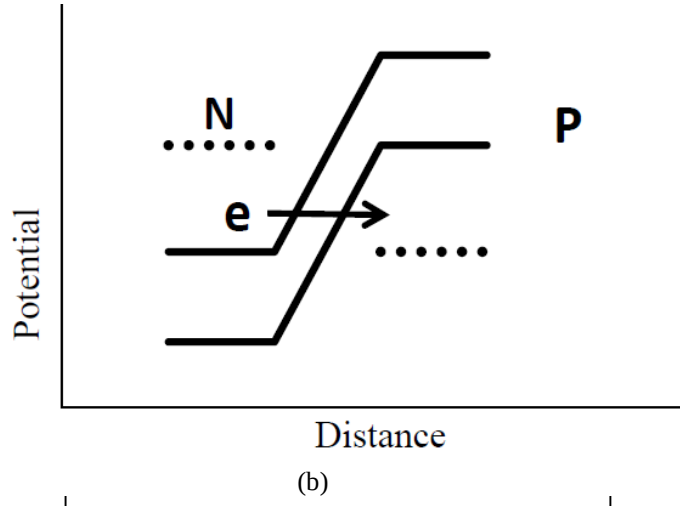
In Figure1, the I-V characteristic of degenerately doped p-n junction is shown in forward bias as well as in reverse bias condition. Different region of working is labeled in the characteristic.

Now we will explain the current-voltage characteristic of the degenerately doped p-n junction by considering the band diagrams in Figure 2. Figure 2 (a) Shows the energy band diagram at zero bias, which produces zero current on the I-V diagram. Figure 2 (b) Shows the situation when a small forward bias voltage is applied to the junction. Electrons in the conduction band of the n region are opposite to the empty states in the valance band of the p region. There is a finite probability that some of these electron will tunnel directly in the empty states and producing a forward bias tunneling current corresponding to O-X region in I-V characteristic. The point X in characteristic is the peak point of tunneling current when the Fermi levels are aligned with conduction and valance band. Then maximum no of electron in the n region will be opposite the maximum number of empty states in the p region; this will produce maximum tunneling current.

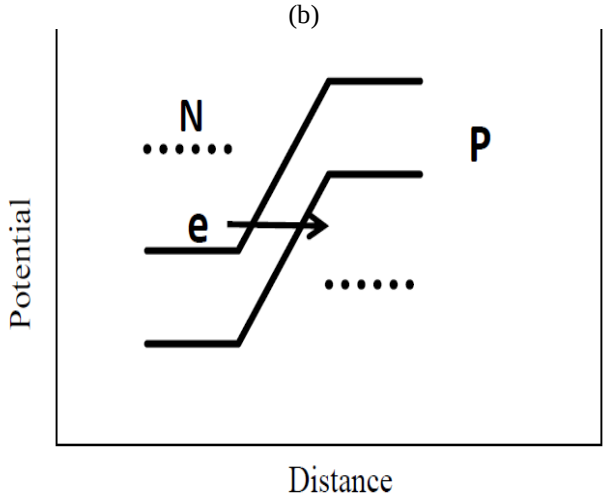
As the forward bias voltage continues to increase, the number of electrons on the n side directly opposite empty states on the p side decreases, as in Figure 2 (c) and corresponding current of region X-Y in characteristic will decrease. This portion of I-V characteristic is known as differential negative resistance region as current decreases with an increase in voltage. The range of voltage and current for this region is quite small, thus any power generated from an oscillator using this negative resistance property would also be fairly small. In Figure 3 (a), there are no electrons on the n side directly opposite available empty states o the p side. For this forward bias, tunneling current will be zero and the normal diffusion current will exist as shown in the portion Y-W of current-voltage characteristics.

The energy band diagram of the tunnel diode with an applied reverse bias voltage is shown in Figure 3 (b). Electrons in the valance band on the p side are directly opposite





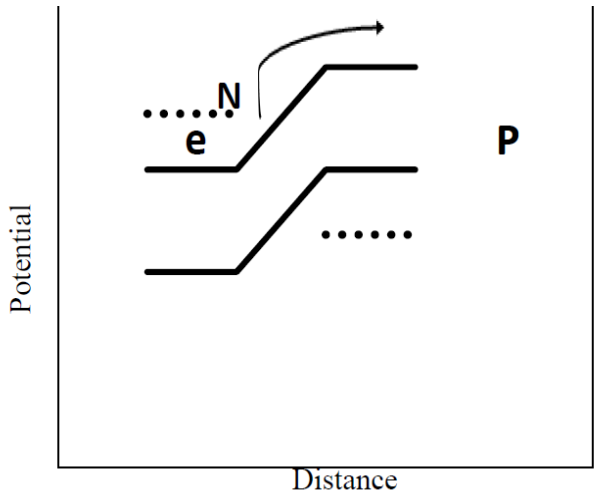

(b)



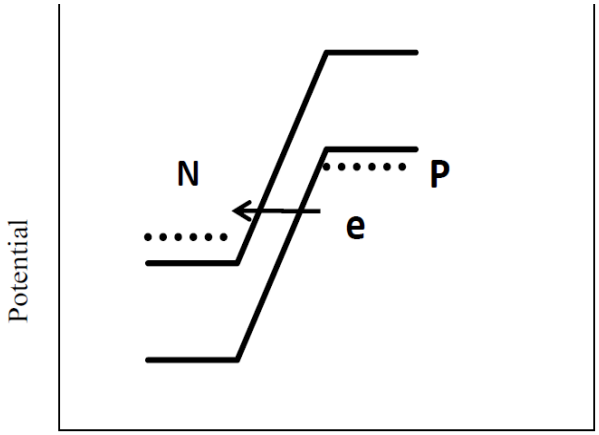

(c)

Figure 2 Simplified Band diagram at (a) Zero bias (b) a forward bias producing tunneling current (c) a higher forward bias less tunneling current.

empty states in the conduction band on the n side; electron can tunnel directly from p region to n region, resulting in a large reverse bias tunneling current. This reverse current will increase monotonically and rapidly with reverse bias voltage.




(a)




(b)

Figure 3 Energy band diagram at (a) a forward bias for which diffusion current dominates (b) reverse bias tunneling current.

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