Diagnosis of Resistive open Fault using Scan Based Techniques

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***Abstract*: Resistive open fault is a partial open failure which occurs during manufacturing process. Due to the presence of resistive open fault the electrical behavior alters. Resistive open fault is tedious to found comparing strong open in the circuit. Delay test is used to identify the presence of resistive open defect, that test further increasing the delay and decreases the test speed.The goal of this project is to demonstrate that physical defects, inducing delay faults in critical paths or in short paths (small-delay defects), can be detected using a classic BIST architecture. Performance violations for different VDD values are captured in digital signatures, which significantly differ from the fault free signature. As both the circuit under test and the BIST circuitry are under VDD variations, corrupted signatures may emerge due to abnormal behaviour from these two sources. The scan based BIST select the particular test pattern which is suitable for identifying the defect. These techniques the improvement of the test speed without affecting the defect coverage is done. Thus Scan based techniques enhance the fault distinction.**

Index Terms: ***Small Delay fault, Resistive open fault (ROFs), BIST, Scan based dynamic BIST, Delay fault testing.***

I. INTRODUCTION AND BACKGROUND

The main objective of testing at the gate level is to verify that each logic gate in the circuit is functioning properly and the interconnections are good. Resistive opens are common manufacturing failures that induce voltage-dependent delay faults and pose potential reliability risks due to their break- like nature. The effect of this fault is distributed and it refers to permanent faults. Differentiating delay failures induced by resistive open faults (ROFs) from those induced by other mechanisms is important in reducing failures. These techniques give an empirical observation of delay pattern versus VDD for resistive opens compared to other fault mechanisms. The detectability and behavior of ROFs depend on the technological and electrical characteristics of the design and test conditions, as well as the supply voltage. Given such dependencies, comprehensive modeling of the fault behavior and detectability becomes challenging. Sometimes the delay fault detectability may be sensitive to the speed of the test

II. OVERVIEW OF BIST ARCHITECTURE

Built in Self Test (BIST) is the capability of the circuit to test itself. It is used to generate the test sequence and those test sequences are applied to the circuit. The output response from the circuit is compared to stored response from the comparator. Based the comparator result the faulty and fault free circuit are identified.

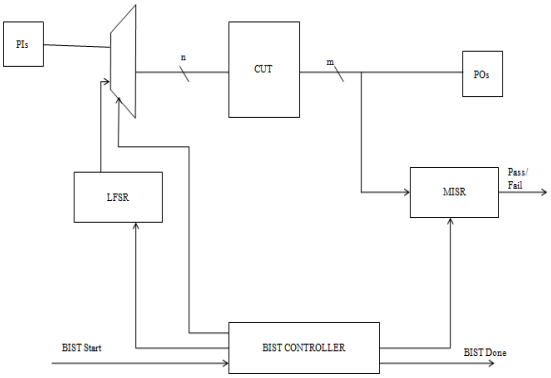


Fig 1. BIST Block Diagram

BIST architecture having main components of LFSR, MISR, CUT, BIST Controller During its lifetime, a digital system is tested on numerous occasions. Test and diagnosis must be fast (low TL) and lead to high fault coverage. With self-test, test is specified as part of the system functionality. BIST methodology incorporates test pattern generation and output response analysis capabilities on chip.

The basic BIST architecture is shown in Figure 1. This architecture is very efficient when the CUT is combinational. If the CUT is a sequential circuit, it is necessary to partition it in a combinational CUT, and one or more scan chains in self-test mode, in order to increase the observability to the internal nodes. The two most common BIST approaches are the Random Logic BIST (also known as Scan BIST) and the Memory BIST. The first one is based on the addition of a Pseudo- Random Pattern Generator (PRPG) to the primary and to the scan inputs and the addition of a Multiple Input Signature Register (MISR) to the primary and scan outputs. Usually the PRPG is implemented using a Linear Feedback Shift Register (LFSR). The BIST Controller generates the necessary clock pulses to load the pseudo-random patterns into the scan chain. All the responses are captured by the MISR, which compacts the circuit responses into a signature. Any signature (a specific digital word) different from the one of the good machine indicates a faulty circuit.

The integration of BIST also requires additional I/O pins for activating the BIST sequence (the BIST Start), for reporting the results (the Pass/Fail) and an optional indication that the BIST session is complete and that the results are valid (the BIST done).

A.Scan BIST Architecture and Operation

The goal of creating a BIST architecture based on the scan design is to incorporate a TPG in the form of an LFSR in the Scan In input of the scan chain and an ORA in the form of a MISR in the Scan Out output of the scan chain. For this scan-based architecture system input isolation is required, as well as the capacity of applying test patterns to the primary inputs and data compaction to the primary outputs. That function is guaranteed by the BIST Controller, which provides the Scan Mode control to switch the scan flip-flops between system mode (to apply test patterns and recover the output responses) and shift mode (to shift in the test patterns from the LFSR, and shift out the response to the MISR). At the same time, this must disable the output response compaction until valid output responses are available in the primary outputs and in the Scan Out output

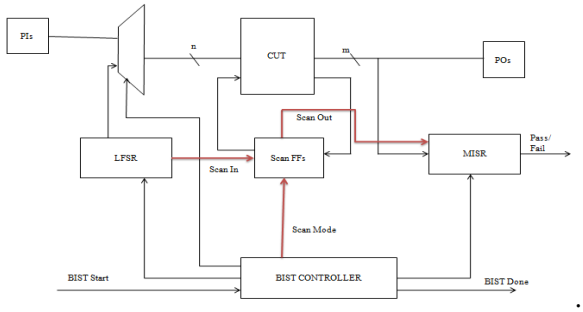


Fig 2. Scan Based BIST Block Diagram

As a traditional BIST approach, the scan BIST sessions begins with the activation of the BIST Start. At this instant, the BIST Controller initializes the LFSR and the MISR. After that the LFSR begins to generate pseudo-random test patterns that are shifted into the scan chain. When this chain is totally filled, the BIST Controller changes the control of the scan chain to system mode during a clock cycle to apply the test patterns to the CUT. At the same time, the test patterns are applied to the primary inputs by the LFSR. The CUT responses are clocked into the scan chain during this clock cycle. After that, the BIST Controller enables the MISR to start output response compaction and switches back the scan chain to shift mode. As the output responses is loaded back into the scan chain and shifted out for compaction, the next pattern is shifted into the scan chain. That process is repeated until the end of the BIST sequence. When this is completed, the MISR is disabled until the resultant signature can be read for pass/fail determination of BIST.

B. LFSR (Linear Feedback Shift Register)

One of most important components in a BIST structure is the TPG. The fault coverage obtained is a direct function of the test patterns generated by the TPG. There are several types of test patterns that can be used in BIST. One of the reasons LFSR to be the most ordinarily used TPG is that requires less combinational logic per flip-flop.

There are two basic types of LFSR implementations: an external or linear LFSR and an internal or modular LFSR.

The modular LFSR provides the implementation with the highest maximum operating frequency, due to the fact that it has, at most, one exclusive-OR gate in any path between flip-flops. On the other hand, linear LFSR, that has two exclusive-OR gates, in the worst case, between the output of the last flip-flop and the input of the first one, has the benefit of the uniformity of the shift register. One common way of generating test patterns is to apply at primitive polynomials (there are polynomials that result in a maximum length sequence). In an LFSR with N registers, if it implements a primitive polynomial, it is able to generate a sequence of (2N-1) test vectors. For example, for N=20, an extremely long sequence is generated.

C. Signature Analysis

During BIST, it is necessary to reduce the enormous number of circuit responses. In most ORA techniques those responses are compacted into a signature that is compared with the expected signature for the fault-free circuit. The Signature Analysis is the most commonly used technique for ORA in BIST implementations. This method uses an LFSR as the basic component. This LFSR is different from the one used in TPG, since it needs an input data, which in this case is the output response of the CUT. That response can be represented by a polynomial. The basic idea is to divide that polynomial by the characteristic polynomial of the LFSR. The remainder of this division is the signature used to determine the status (faulty or not) of the CUT and the end of the BIST sequence. The solution used is referred as MISR because it can compact multiple outputs into a single LFSR.

D. Multiplexer

This component selects the inputs to be applied to the CUT during BIST:

- Normal operation the primary inputs are directly applied to the CUT
- In Shift operation the test patterns generated by the LFSR are applied to circuit.

E. BIST Controller

When the BIST Start is activated, the BIST Controller performs below steps:

- Initializes the LFSR and the MISR,
- Isolates the primary inputs by selecting the alternative inputs to the input isolation and multiplexers
- Drives the scan chain into the shift mode.

Every time the scan chain changes the operation mode, this is triggered by the BIST Controller. At the same time, all the MISR activity is also controlled by this FSM. To begin the output response compaction, the BIST Controller has to enable the MISR. When the BIST session is completed, the MISR is disabled and the BIST Done is activated.

III.SCAN-BASED DYNAMIC BIST

The proposed methodology for scan-based dynamic BIST merge the LOS and/or LOC techniques for delay testing, used in scan design with external test, with Built-In Self Test.This architecture exhibits some changes in comparison with the traditional Scan BIST approach. The visible and first difference is in the modules used and their interconnection. As shown in Figure 4.1, the architecture is composed of the CUT (reconfigured with scan flip-flops), a BIST Controller, a MISR, the input MUX and two LFSR. Due to fact that this new architecture will be used for at-speed test, some changes have to be made, especially in the BIST Controller (with different functionality) and in the TPG (using two LFSR).

As stated, in this paper use two linear LFSR, namely LFSR_PI and LFSR_SCAN. The first one is used to generate pseudo-random (PR) test patterns to be applied to the CUT's primary input in self-test mode. The second LFSR generates PR test patterns to be applied at the first flip- flop of the scan register (as the test_s_i signal). Although the proposed two-LFSR solution introduces an area penalty, I decided to implement this configuration because it can reduce the polynomial correlation and, as a result, it can increase delay fault coverage.

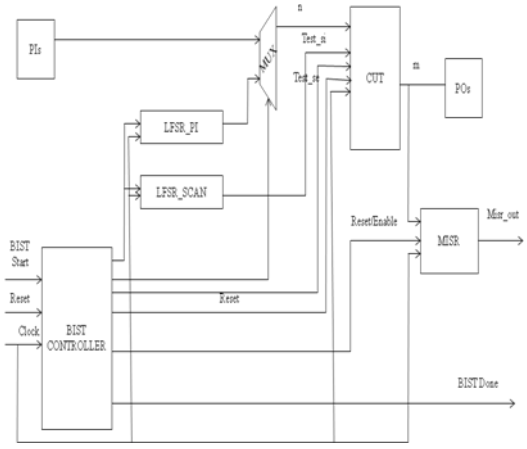


Fig 3. Scan-Based Dynamic BIST

The proposed methodology and its architecture can accommodate LOS, LOC or both. The difference among the three presented approaches is clustered in the BIST Controller functionality. This is the key module in the proposed architecture and one of the attractive features of the proposed methodology. Due to the fact that I have to implement different techniques to test delay faults and that the state of Scan Enable signal (defined as test_$s_e$signal in this work) is different in the LC of LOS and LOC, I have to add a new state at the module definition (referred as LAUNCH). That decision implies an increase area in the BIST Controller, as compared to the traditional module.

A.BIST controller for LOS

As is name indicates, this module is the most important in the dynamic scan BIST architecture because it controls all the other modules and operations. Figure 4.2 identifies all input and output signals of the module. In the outputs it is referred the module where each output signal will be the input.

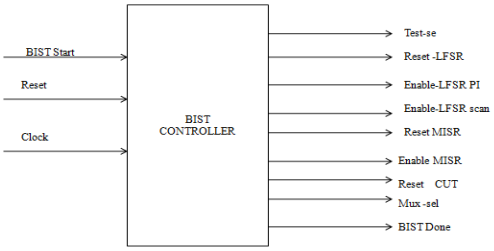


Fig 3. BIST Controller

In the proposed architecture, two counters are used for the BIST Controller: one counter (referred as the scan counter, C_SCAN) to count the number of flip-flops in the scan chain for shifting in the scan vectors and another counter (referred as the vector counter, C_VECT) to count the number of scan vectors applied to the CUT.

B. LFSR

In this work are used two LFSR: LFSR_PI and LFSR_SCAN. They are both depicted in Figure5, with the identification of the input and output signals of each one. Both are controlled by the BIST Controller that produces the Enable and Reset control signals.

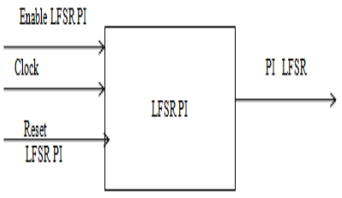


Fig 5.1. LFSRPI input/output signals

The LFSR generate the pseudo-random test patterns to be applied to the CUT as primary inputs (LFSR_PI) and to be applied and shifted in to the scan chain (LFSR_SCAN)

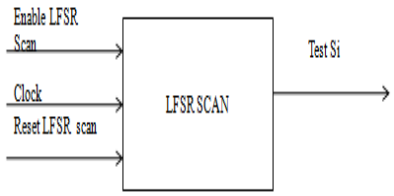


Fig 5.2. LFSRSCAN input/output signals

C.MISR

Again, the number of flip-flops of the Multiple Input Shift Register (MISR) depends on the number of PO of the CUT to be observed. In this work, to the MISR implementation it is used an LFSR with a degree of polynomial of 7. Note that the LFSR used as an Output Response Analyzer (ORA) needs input data, namely the output response of the CUT. That signal may have a different size from the primary outputs of CUT because it can changes from 1 to m (in the compaction process, one or more PO can be used as MISR input data).

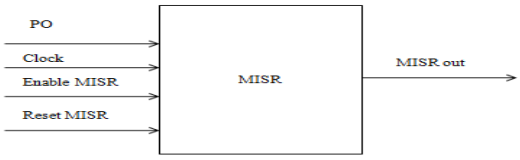


Fig 6. MISR input/output signals

D. Circuit Under Test (CUT)

The CUT used to test the proposed dynamic scan BIST methodology was the ITC'99 b06 benchmark, which is a sequential circuit. The benchmark circuit is previously synthesized and reconfigured for scan chain insertion. Before made this interconnection to other modules it was compiled to perform an area optimization.

E. Multiplexer

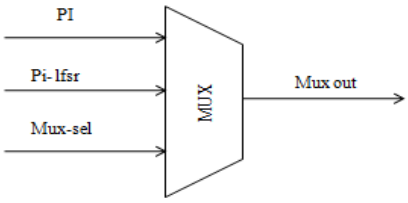
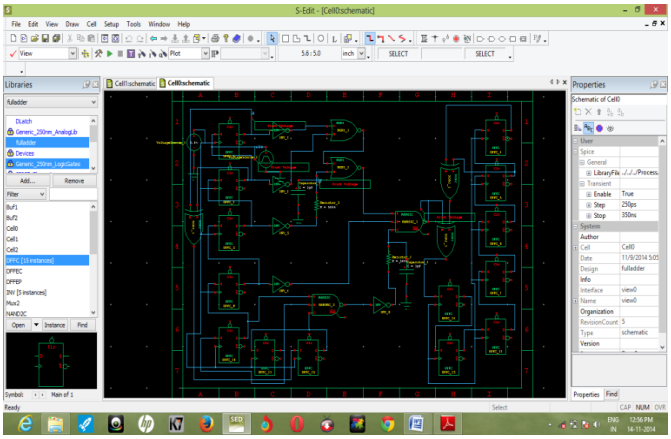


Fig 7. Multiplexer

The number of implemented multiplexers depends on the number of PI. It is necessary one MUX for each PI. The function of that component is to select if the primary input signals applied to CUT are the external ones, or the ones generated by LFSR_PI. When themux_sel signal is enabled, the PR test vectors are applied to the CUT, which happens in the self-test mode.

In the proposed dynamic scan BIST methodology is used two linear LFSR because they are easily implemented due to the uniformity of the scan register and for their suitability for scan design. The degree of the polynomial (i.e., the number of registers) depends on the CUT. In this work, I implemented two 7 bit LFSR generators (with a degree of polynomial = 7) mapping a primitive polynomial P(x) = x7 + x1+ 1. Hence, I implement an LFSR with 7 flip-flops and 1 exclusive OR gate (x1). Since the 7 registers LFSR is big to be drawn, in Figure 4.4 there is show a linear LFSR with 4 flip-flops and 1 exclusive OR gate, implementing also a primitive polynomial, P(x) = x4+ x+ 1.

SCHEMATIC VIEW OF CUT



IV. SIMULATION RESULTS

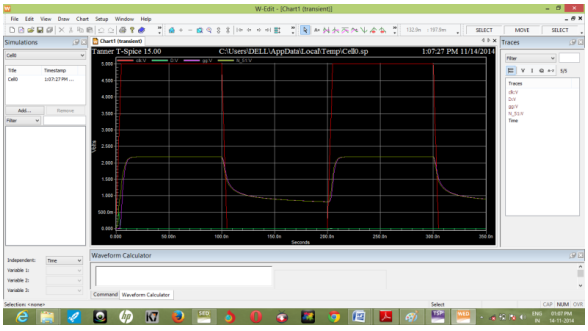


Fig 8.Fault Free Response

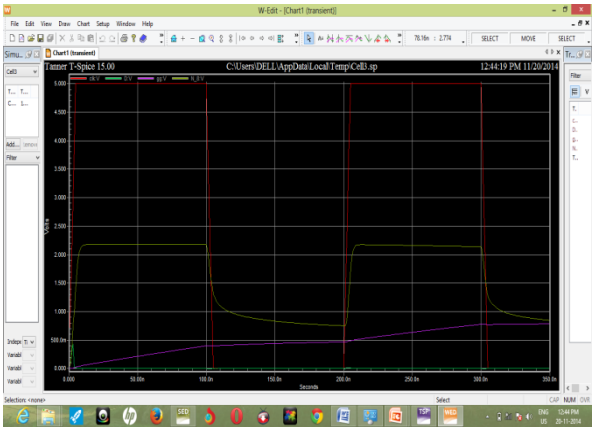
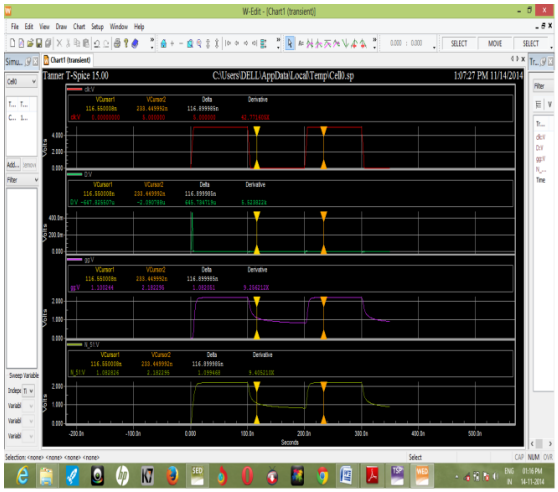


Fig 9. Faulty Response

Fig 10. Delay Measures of Circuit



OBSERVED DELAY

FAULT SIZE	10KΩ	100KΩ	500KΩ
FAULT A	162.288ps	777.944ps	180.957ps
FAULT B	1.6091ns	2.7141ns	7.2263ns
ORIGINAL DELAY : 1.4335ns			
VOLTAGE :1.2V			

V. CONCLUSION AND FUTURE WORK

The behavior and detectability of ROF were analyzed as a function of rising and falling edges of delay in the circuit. Simulations showed that the behavior of an ROF is a function of the resistance and the detectable resistance range varies with VDD. Fault simulation results to compute the fault coverage results for static faults must be carried out. An additional line of work could be to use the deterministic scan BIST solutions available (in terms of the definition of the hybrid test sets), and evaluate the coverage of dynamic faults. If needed, a small subset of additional test vector pairs would then be generated and added. More accurate results can be obtained if the fault simulation process uses post-layout information, namely the capacitive effects that induce time delays.

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