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Development of Verification Infrastructure to Validate RAM Low Power Features at Unit Level

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***Abstract*—Various low power techniques incorporated in low-power design, particularly in GPU with multiple power islands or voltage islands. The different industrial standard tools and languages that are used in the design process are spoken about, and the design methodology is elaborately explained. RAM power gating at unit level is discussed in detail. A reduction in leakage currents was noticed when standard low power cells are inserted correctly. This is evident from the reduction of leakage current in percentage for sleep mode 98 % of leakage reduction is present and in retention mode depending on the technology node used there is 80 % of leakage reduction. There is also a significant improvement in the CPU time and simulation time and maximum memory utilized.**

Keywords*—Low power methodology, power gating, SRAM, low power verification.

I. INTRODUCTION

These days, consumers demand for devices to pack more features and greater performance but also want the device to have a long battery life, have a convenient form factor and produce less heat. Hence, we require low power methodologies to optimize and improve the efficiency of devices. Devices consume power when in use. But for a given application, the entire device may not be in use. Device power is hence being wasted if these unused regions are being powered. This is especially important in battery-operated devices. Therefore, we can reduce power consumption by turning off the parts of the design that are not being used. Power gating is a technique used in VLSI circuit design wherein we can reduce power consumption by turning off parts of the design that are not being used. Techniques like power gating are used in RAM's to save RAM leakage power. The goal of low power design is to reduce the individual components of power as much as possible, thereby reducing the overall power consumption. The power equation contains components for dynamic and static power. Dynamic power is comprised of switching and short-circuit power; whereas static power is comprised of leakage, or current that flows through the transistor when there is no activity. In practically every area, the world demography has experienced extraordinary increase. Energy use has grown to be a big concern throughout time. Aside from environmental issues, a consumer space's energy use is becoming a deciding aspect of choice.

Identifying all the RAM related low power issues at full chip level is extremely challenging. It requires exhaustive test plan and patterns, achieving coverage at complete level is difficult. Turn-around time of catching the issues, fixing them and re verifying the design is very costly. Simulation run time is huge. Full chip level simulations take about 2-3 days. If simulation issues are hit at final stages of the simulations or verification, design changes cannot be made, which can increase the PG (power gating) cost. Hence, development of a unit level verification infrastructure to catch all RAM related low power issues faster and in a more efficient way is required. The objectives of the project are: To have exhaustive low power verification coverage at unit level. To catch issues at pre-silicon environment at early stages. To optimize turn around time of identifying ad fixing issues at unit level. To develop a robust flow which can catch such issues in ongoing and future projects.

II. METHODOLOGY

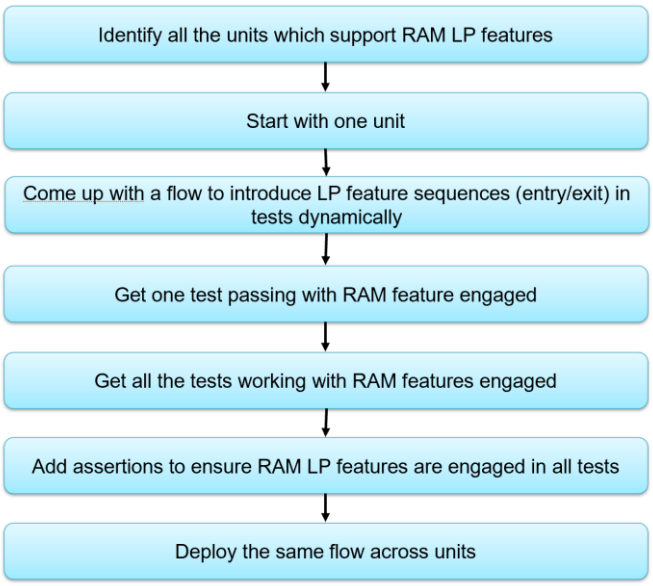

Fig. 1. Flowchart describing methodology.

A. Brief methodology

Brief methodology of the project is explained in the form of a flow chart in the below *Fig. 1*. First and foremost, step in the methodology is to identify all the units of GPU which supports RAM low power features. Some units of the GPU might be supporting low power features at logic level but not at RAM level. Next is to select a unit, and come up with a flow or sequence to introduce low power features, i.e., safe entry and exit in the tests dynamically. Entering the low power state and making sure that the contents of the RAM is

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intact is to be ensured. In any regression-based test, it contains multiple tests at a single level. Aim is to get at-least one test passing with RAM low power features engaged along with other low power features engaged. Both Sleep and Retention low power modes should be passing at one level. Next would be to get all tests at one level passing for both Sleep and Retention low power modes. Addition of assertions to ensure that RAM low power features are engaged in all the tests and the test is not skipping the complete sleep and retention mode and the result is a false pass. Addition of debug registers to enable easy debugging. To understand easy workflow of the algorithm.

B. Power Gating

Multiple low power methodologies are used in the industry, but power gating is mainly used in order to reduce leakage power. The basic strategy of power gating is to provide two power modes:

• Low power mode
• Active mode

The main goal of power gating is to switch between these modes at the appropriate time and in the appropriate manner in order to maximize power savings while minimizing it's impact on performance of the IP. It is a slightly expensive method to reduce leakage power. *Fig. 2* represents the generalized block diagram of the power gating strategy. It includes a power gating controller which sends in signals to control the isolation cells and the retention registers. Also, the power gating controller sends in control signals to the power switch network which is in turn connected to the power gated domain or logic [1]. The header or footer switches used in power gating are controlled by the signals sent from the power gating controller. To avoid corruption of the always ON domain of the IP from the power gated domain, isolation cells are added. The O/P signal coming from the power gated domain is stored in the isolation cell and not passed on to the always ON domain. The isolation control EN signal is also obtained from the power gating controller. Power switch network is situated between the VDD and VSS rails. Retention registers are to used to retain the data or valid O/P of the power gated logic just before power down. [2]

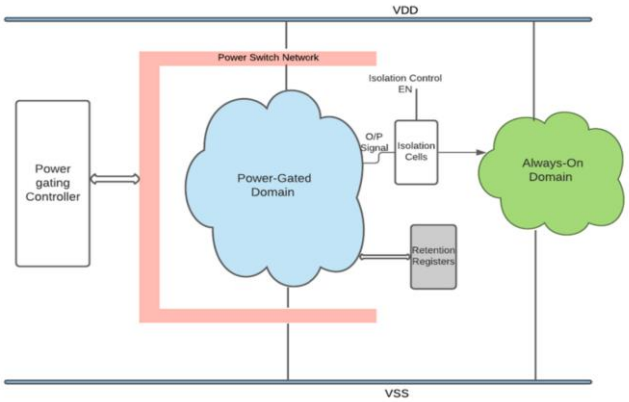

Fig. 2. Block diagram of power gating.

III. DESIGN OF POWER GATING IN RAM

A. SRAM Architecture

Data must be able to be read, written, and stored in an SRAM cell throughout the duration of power application.[3] This criterion may be satisfied by a regular flip-flop, but they are fairly huge. A typical 6-transistor (6T) SRAM cell, which may be an order of magnitude smaller than a flip-flop, is depicted in *Fig 3*. The 6T cell's compactness is achieved at the cost of more intricate peripheral circuitry for reading and writing cells.6tsram In big RAM arrays, where memory cells predominate, this is a good tradeoff. Shorter wires are another benefit of the reduced cell size, which results in less dynamic power usage.

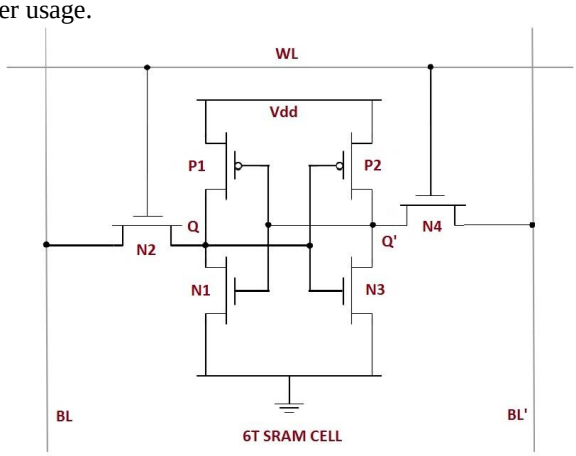

Fig. 3. 6T SRAM schematic

SRAM mainly operates in three modes, they are:

i. Hold mode
ii. Read mode
iii. Write mode

B. Power Gating of Single Rail SRAM

Single rail RAM suggests that there is only one VDD line powering the entire RAM. By including integrated power-gaters, compiled RAMs can be put into one of two power saving modes: retention and sleep. In retention mode, the bitcell array remains powered up (at VDD voltage supply), while the peripheral logic is de-powered, thus allowing the RAM state to be retained. In sleep mode, the entire RAM is de-powered which causes all state to be lost, but with the benefit of additional power savings. An area penalty is incurred when including integrated power-gaters. Waking-up from a sleep or retention mode is done in a controlled manner in order to clamp in-rush current to an acceptable level.[2]

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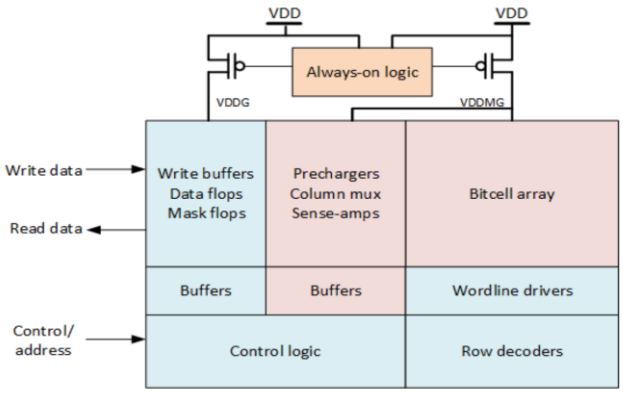

Fig. 4. Single Rail SRAM

Single rail SRAM architecture is described in the above *Fig. 4* SRAM consists of two parts to it, i.e., the SRAM bit cell array and SRAM periphery. Their block diagrams along with power modes will be discussed in the below sections. SRAM periphery consists of the logic and design in blue color, they are write buffers, data flops, mask flops, buffers, control logic, row decoders, pre-chargers, column MUX, sense amplifiers and worldline drivers. SRAM bit cell array holds the data stored in the SRAM. Its contents are stored in terms of O's or 1's. There is also a always ON logic in the single rail SRAM architecture which has the control logic to power the header sleep FET's. Always ON logic is connected to VDD. VDDG and VDDMG are virtual VDD which is available to the SRAM when it is not gated. The Always ON logic consists of a combinational circuit which handles the sleep FETs (PMOS), it provides either logic 0 or 1 depending on if the PMOS must be turned ON or OFF. VDDG is connected to the periphery logic, i.e., the write buffers, data flops, mask flops, buffers, control logic, row decoders and word line drivers. VDDMG is connected to the bit cell array, pre-chargers, sense amplifiers and buffers. Write data is signal is sent from outside logic to write buffers, data flops and mask flops. Read data is collected from the buffers present in the SRAM periphery. Control and address signals are sent to the control logic, row decoders and word line drivers present in the SRAM.

C. Low Power Modes in SRAM

When power-gating is used, compiled RAMs can be placed into one of two power saving modes: retention and sleep as shown in *Fig. 5.*

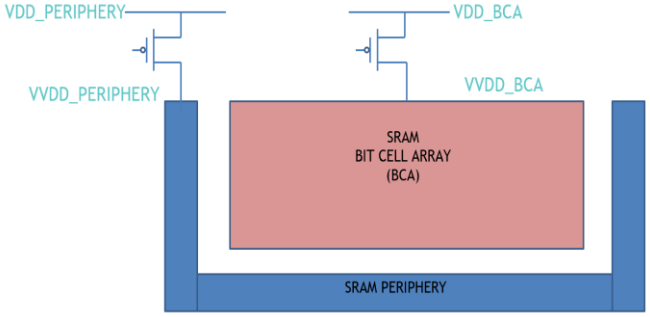

Fig. 5. Structure of SRAM.

1) SLEEP MODE

In sleep mode the power-gaters for the VDDMG, VDDG domains are shut off completely causing all data in the bit cell array to be lost. Sleep mode provides greater leakage power reduction than retention mode. When any power-gated RAM is in sleep mode, the RD outputs will be actively driven to ground.

- The virtual power rails are obtained after passing through the PMOS sleep FET.
- In the sleep mode of SRAM, both the bit cell array as well as the SRAM periphery are both power gated.
- That means that VVDD PERIPHERY and VVDD BCA is equal to 0. At the gate terminal of the PMOS 1 is given to turn is OFF.
- The data contents of the bit cell array is lost when power gated.
- To retrieve the data in the bit cell array, the data first has to be stored in an external DRAM and then restored once the power is backed up.
- Sleep mode is suggested only when there is high time latency.
- Power savings is higher in the sleep mode as the complete SRAM is turned OFF

2) RETENTION MODE

In retention mode the bit cell array supply (VDDMG) is left powered-on, which pre serves the contents of the bit cell array, while the word-line driver supply (VDDG) and the peripheral logic supply (VDDG) is power-gated. This means that the VDDMG domain remains powered-on, i.e., it is powered by the regular VDDMG PFET power-gaters. Output clamping during retention mode, due to difference in implementations, is different between DP and PDP/SP RAMs. Specifically: For all PDP and SP RAMs, their RD* outputs will be actively driven to ground. For all DP RAMs, their RD* outputs are not clamped during retention. So, they will remain at their previous value before enter retention mode, due to the existence of "Fast Wake-up" feature. The SRAM periphery is powered by VVDD PERIPHERY and SRAM bit cell array is powered by VVDD BCA. The VVDD PERIPHERY and VVDD BCA is the virtual power rails. VDD PERIPHERY and the VDD BCA are the original power rail.

- VVDD BCA is turned ON and VVDD PERIPHERY is turned OFF.
- SRAM bit cell array is kept intact, and SRAM periphery is power gated by VVDD PERIPHERY.
- The gate terminal of sleep FET on the bit cell array is given logic 0, to keep it ON.
- The gate terminal of sleep FET above SRAM periphery is given logic 1, to keep it OFF.
- Retention mode is utilized when there is less time latency.
- As soon as the power is backed up, the bit cell array is still intact and there is no requirement for data restoration.

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IV. IMPLEMENTATION OF VERIFICATION INFRASTRUCTURE FOR RAM POWER GATING

A. *Sequence for logic power gating*

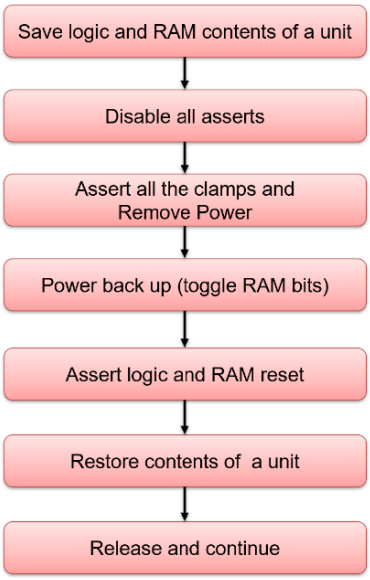

Fig. 6. Flowchart for logic power gating.

Fig. 6 explains sequence for logic power gating. First step is to save all the logic and RAM contents of a selected unit. All the asserts must be disabled, to make sure once the power is removed, the asserts must not be corrupted. Next step before power gating is to assert clamps, to isolate the always ON logic from the power gated domain. Removal of power and power back is based on the main line power. Logic and RAM reset is asserted, as logic power gating focuses on RAM and logic registers. Restore the contents of the unit, both logic and RAM. Release and continue.

B. *Sequence for RAM power gating*

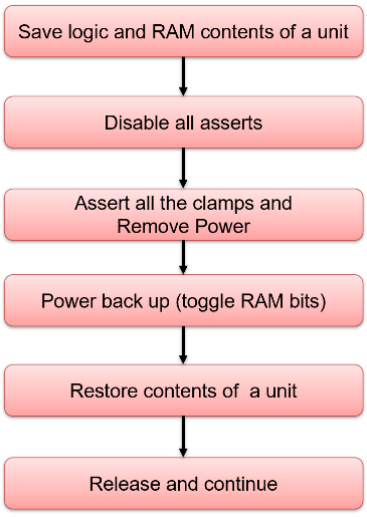

Fig. 7. Flowchart for RAM power gating.

Fig. 7 represents the flow diagram for implementing the sequence for RAM power gating.[4] First step is to save all the logic and RAM contents of a selected unit. All the asserts must be disabled, to make sure once the power is removed, the asserts must not be corrupted. Next step before power gating is to assert clamps, to isolate the always ON logic from the power gated domain. Remove the power. Power can be asserted and deasserted by toggling the bits of pwrbus ram pd. After the power is restored, restoring the contents of the unit. Release and continue.

V. RESULTS AND DISCUSSION

A. *Logic power gating*

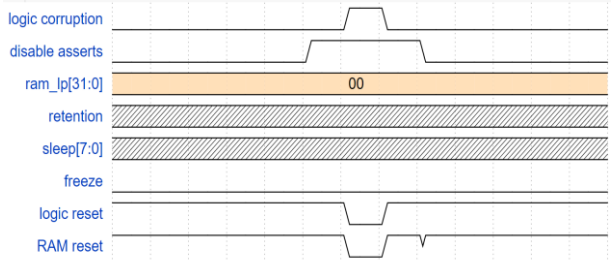

Fig. 8. Logic power gating waveform.

B. *RAM power gating*

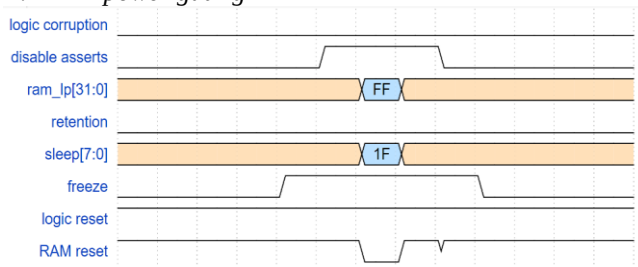

Fig. 9. RAM power gating waveform.

C. *RAM power gating (SLEEP mode)*

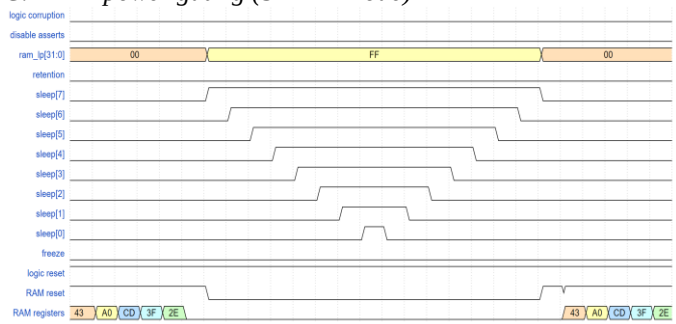

Fig. 10. Waveform for SLEEP mode.

RAM power gating (RETENTION mode)

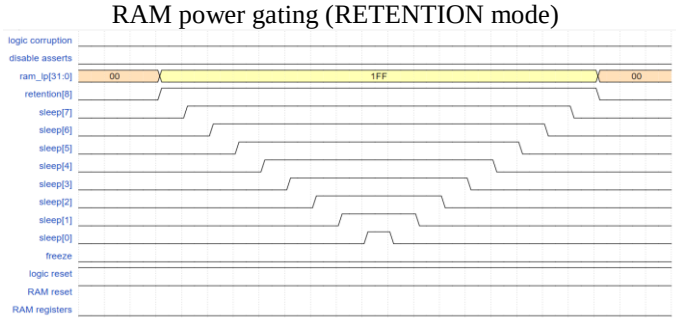

Fig. 11. Waveform for RETENTION mode.

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Fig. 8, Fig. 9, Fig. 10, Fig. 11 are the waveforms explaining logic power gating, RAM power gating, Sleep mode and retention modes.

TABLE I. COMPARISION BETWEEN LEAKAGE REDUCTION

Mode	Leakage reduction	RAM Content
RETENTION	80 %	Alive
SLEEP	98 %	Destroyed

The leakage reduction percentage values for the retention mode is approximately 80%. The leakage power reduction for sleep mode is observed to be 98% as the whole system is powered off is described in Table 1.

VI. CONCLUSION

The experimental demonstration of the workflow discussed in this project found favorable results. A reduction in leakage currents was noticed when standard low power cells are inserted correctly. This is evident from the reduction of leakage current in percentage for sleep mode 98% of leakage reduction is present and in retention mode depending on the technology node used there is 80% of leakage reduction. There is also a significant improvement in the CPU time and simulation time and maximum memory utilized.

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