

Development of S-Band Dual Digital Transmit Receive Unit for Air Surveillance Application

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Abstract—Dual Digital Transmit Receive Unit(DDTRU) is an integrated module based on T/R module concept. The advantages of using T/R module concept are scalability, graceful degradation, adaptability, higher MTBF, transmitter power controlling. DDTRU unit consists of a T/R module, Analog Receiver, Digital receiver and a Power supply unit. T/R module is a Dual channel Transmitter and receiver based on GaN technology. Analog Receiver module takes the received RF (3.1 GHz to 3.5 GHz) from the Antenna and down converts to IF (60 MHz) through 2 stages of Analog Down conversion. IF is fed to Digital Receiver module which uses DDC digital down conversion techniques to extract the Baseband from IF, digitize the Baseband, convert to I and Q data, multiplex data of both channels and send out the I,Q data through an optical channel. Digital Phase shifters and attenuators present in T/R module and Analog receiver are controlled from Digital receiver.

Index Terms—Radar, DDTRU, GaN technology, DC, Baseband.

I. INTRODUCTION

T/R Modules are building blocks of Active Electronically Scanned Array (AESA) Antenna systems as they are configured for mounting directly behind the antenna element, thereby minimizing losses and adding redundancy as compared to Passive Phased Array Antenna Systems. This paper presents the development of S-band Dual Digital Transmit Receive Unit for Air surveillance Application.

The phased array antenna 32 rows are powered by 32 Dual Digital Transmit Receive Unit (DDTRU). The DDTRU amplifies the carrier signal and provides to the antenna array for transmission. The unit receives the echoes from the targets, digitizes and generates I and Q data and sends to Digital Beam Former (DBF).

II. TRANSMIT RECEIVE MODULE

The module consists of transmit channel and receive channel in a single package with only one input and dual output. Transmit part of the system amplifies the 0dBm input signal to +56dBm through a series of power amplifier modules. The Transmit chain is realized by power amplifier modules based on GaN technology. The comparisons of characteristics of GaN and silicon carbide are shown in the table 1.

Table 1

| SUBSTANCE | SiC | GaN |
|------------------------------|-----|------|
| Band gap | 3.3 | 3.4 |
| Electron mobility | 700 | 1500 |
| Electric field for breakdown | 3.0 | 3.3 |
| Figure of merit | 440 | 1130 |

From the table, it is clear that GaN has high breakdown voltage, high heat resistance and high switching speed. Therefore, GaN device has been selected for power amplifier.

There will be two T/R modules in one DDTRU. In the transmit mode the RF input is passed through 6 bit digital attenuator, 6 bit digital phase shifter, switch, buffer amplifier, High Power amplifier (HPA), circulator, bi directional coupler through connector to antenna. The coupled RF sample pulse can be measured / detected for reporting the health of the RF amplification circuit.

On receive mode from antenna the RF flows through bi-directional coupler, receiver protector switch, limiter, LNA, band pass filter, amplifier, switch, digital phase shifter, digital attenuator to T/R switching unit, which in turn routes to First down convertor. The digital attenuator, digital phase shifter, switch and receiver protector switch will be controlled during transmit and receive mode as required by DRx through parallel lines.

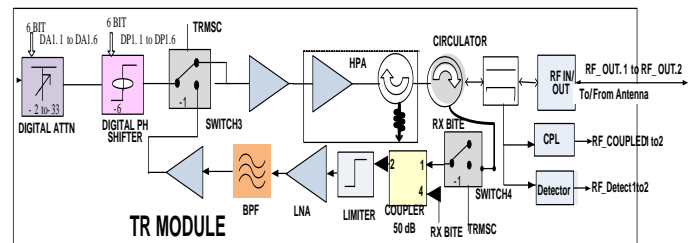


Fig 1

In this T/R module the HPA is GaN based amplifier which generates heat and requires liquid cooling provision (external) to extract the heat out. To extract heat out it is essential to mount the GaN device closer to the chassis or on the chassis which can be mounted on cold plate.

The second most important device is LNA. The overall noise figure (NF) of 3.5dB of the receiver chain is defined by the selection of the LNA's gain and noise figure. Also the 1dB compression point (-5dBm) of the LNA defines the maximum input handling capacity of the receive chain. In turn both NF and 1dB compression point defines receiver dynamic range.

III. ANALOG RECEIVER UNIT

Analog Receiver Unit down converts the received RF (3.1-3.5 GHz) to IF (60 MHz). This is achieved through 2 stages of down conversion.

First down converter chain comprises of 6 bit digital attenuator as MSTC, amplifier, coupler, 6 bit digital attenuator as AMSTC, RF Band Pass filter, matching circuit, Mixer-I followed by First IF band pass filter. There is two numbers of first down converters in a DTRU.

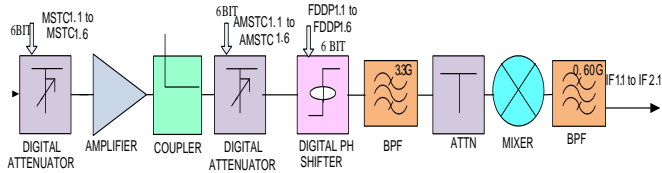


Fig 2

Second down converter comprises of Coupler, Mixer –II, Second IF Band Pass Filter, IF amplifier, Digital attenuator (Fast AGC), Amplifier, Limiter, followed by 2 IF filter banks (one selectable) and coupler, through which it is fed to Digital Receiver. The bandwidths for IF filter banks are 5MHz and 2.5MHz. One of the IF filter banks will be selected by RF switches operating in tandem, depending upon the operating pulse width.

All the control signals namely Fast AGC for IF Gain Control, IF Filter switch controls are provided by Digital Receiver. LO2 input is fed by LO2 buffer module. The output of the second down converter is fed to DRx. There will be two such Second down converters in one DTRU.

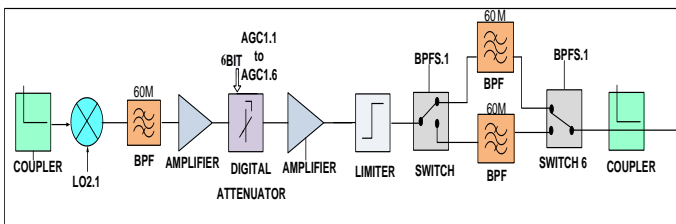


Fig 3

IV. DIGITAL RECEIVER UNIT

The S-Band Digital Receiver (DRx) is based on Xilinx Artix FPGA. Major functions of the DRx are Digitization of 2 IF signals, 2-Channel Digital down Conversion and high speed serial communication with DBF unit. Two 16-bit ADCs are used for sampling the two IF channels with isolation of 60dB and sampling clock used is 50MHz.

The phase detector module decomposes the incoming 16 bit data from the digitization module into in-phase and Quadrature-phase components and mixes the data with 10MHz sine and cosine samples generated by an NCO at a sampling rate of 50MHz. The output of this stage is 16 bit I and Q data for each channel for filtering and decimation.

The sampled quadrature output stream is at 5/2.5MSPs depending on the bandwidth selection. Finally the baseband signal is passed through a Low Pass Filter and decimation filter to get the signal of interest. The filter cut-off is selected so as to allow maximum signal of interest. The output of the

anti-aliasing filter and decimation module are 16 bit I and 16 Bit Q samples available at 5MHz/2.5MHz.

Simulation plots:

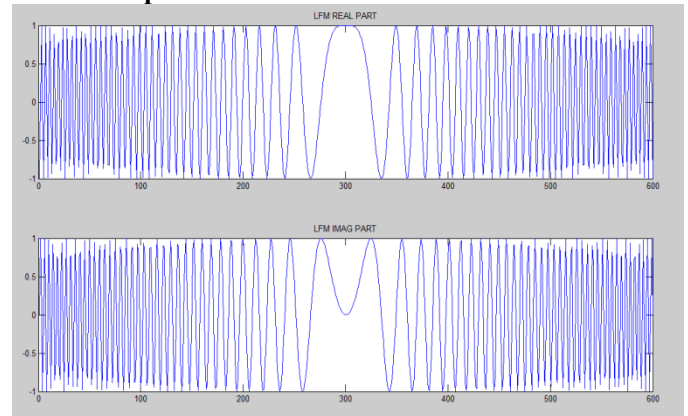


Fig 4: Simulated DDC output for 60µs LFM and BW 2.5MHz

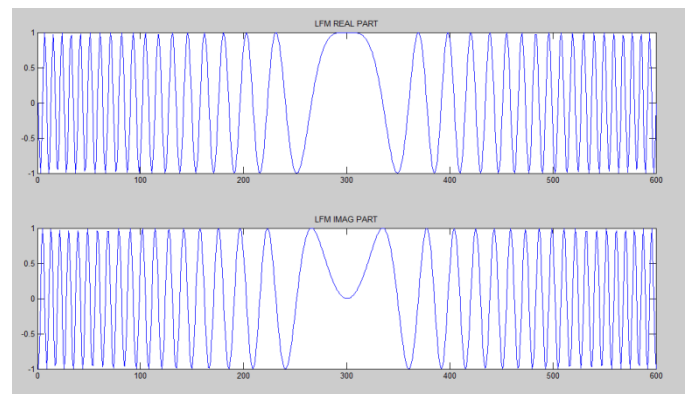


Fig 5: Simulated DDC output for 60µs LFM and BW 5MHz

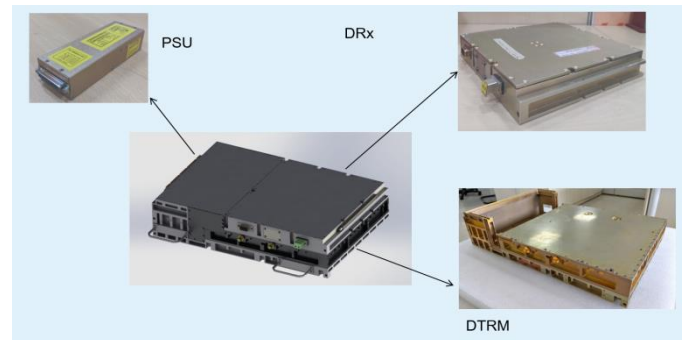


Fig 6:Realized DDTRU

Table 2: Receiver Gain

| Freq(GHz) | CH1(dB) | CH2(dB) |
|-----------|---------|---------|
| 3.1 | 62.3 | 57.0 |
| 3.2 | 60.0 | 57.0 |
| 3.3 | 59.0 | 55.5 |
| 3.4 | 58.0 | 56.0 |
| 3.5 | 57.0 | 55.8 |

Table 3: Receiver Noise Figure

| Freq(GHz) | CH1(dB) | CH2(dB) |
|-----------|---------|---------|
| 3.1 | 2.5 | 2.8 |
| 3.2 | 2.6 | 2.9 |
| 3.3 | 2.8 | 2.9 |
| 3.4 | 3.0 | 2.8 |
| 3.5 | 3.1 | 3.1 |

Table 4: Transmit Output Power

| Freq(GHz) | CH1(dBm) | CH2(dBm) |
|-----------|----------|----------|
| 3.1 | 56.7 | 57.6 |
| 3.2 | 56.4 | 57.7 |
| 3.3 | 57.5 | 57.7 |
| 3.4 | 57.3 | 57.8 |
| 3.5 | 57 | 57.6 |

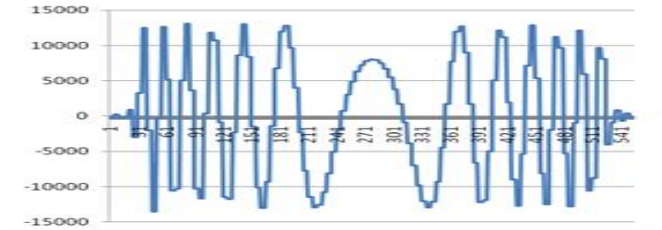


Fig 7: DRx Output-In Phase channel 1

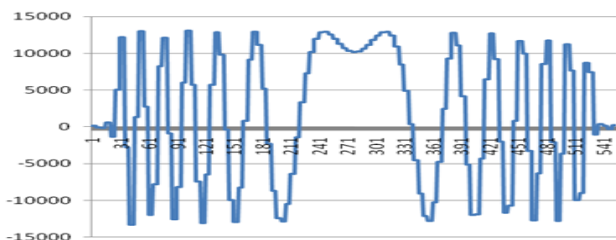


Fig 8: DRx Output- Q phase channel 1

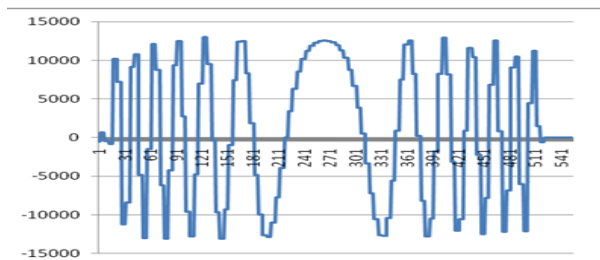


Fig 9: DRx Output- In phase channel 2

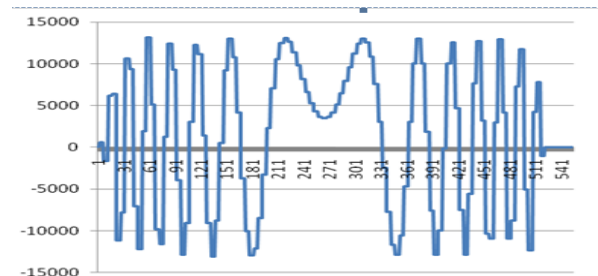


Fig 10: DRx Output- Q Phase channel 2

V. CONCLUSION

Dual Digital Transmit Receive prototype unit has been developed. Set of tests are carried out to evaluate the performance of DDTRU and found satisfactory, complying with the requirements.

VI. ACKNOWLEDGMENT

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VII. REFERENCES

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