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Determination of Thermal Induced Stresses in Semiconductor Chip Package by using Finite Element Analysis: A Brief Review

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***Abstract*— In todays advanced electrical technology, it becomes necessity to use compact semiconductor chips in variety of areas like computers, electrical appliances, automotive etc., clearly the need of more and more sophisticated packages is increasing. As the need of faster computer increases design of denser and more complicated packages becomes unavoidable, more complicated packages means that, the size of chip more or less remains same, but it has more electronic circuitry per unit surface area, this, of course increases the temperature of packages and causes thermal expansion due to change in coefficient of thermal expansion of the constituent materials. Thermal stresses ultimately cause the failure of the device. An IC package mainly consist of four parts, silicon die (chip), polymeric substrate, plastic molding compound and connectivity parts, lead frames and bond wires. The silicon chip is assembled on a polymeric substrate, plastic molding compound surrounding both parts, lead frames and bond wires provide electrical connectivity between the package and board on which assembly is made. The complicated geometrical structure and different material properties as well as the loading conditions made it almost impossible to study the mechanical behavior of semiconductor package analytically; therefore the finite element method has become a useful tool for evaluation of problems encountered in this area.**

Keywords*— *Semiconductor Chips, Thermal Analysis, FE Analysis, Temperature Of Package

I. INTRODUCTION

The objective of the review is to carry out a number of finite element (FE) analyses to predict thermal and mechanical stresses in the semiconductor package and optimize its shape. The interfacial integrity of an integrated circuit (IC) is a very significant reliability issue for service life performances. Any sort of interface degradation can cause failure of chip or if not, affects its efficiency resulting in substandard operations.in addition to delamination failure modes. Other structural failure includes, metal line deformation, passive cracking, dielectric cracking, wire bond shear and epoxy molding compound cracking. The thermal stresses in semiconductor packages are caused by thermal expansion (contraction), mismatch of dissimilar materials and/or non-uniform temperature distribution within the package and may result in failure of the package. The normal stresses in a bi-material assembly are an important aspect in studying the thermal stresses induced in the semiconductor die substrate assembly. Multicolored, multilayered structures are needed for IC's, MCM and PCB system, due to important effect on the transmission of high speed signals. Also the transmission lines effects on the IC interconnects becomes extremely important for the transmission behavior of interconnects lines on silicon oxide-silicon semiconducting substrate. The conducting silicon substrate causes capacitive and inductive coupling effect in the structure. For advanced IC's, the packaging technology mainly based on the area-array packages or the flip-chip solder interconnects. This type of package connects the active device side of the silicon die face via solder balls on a multilayered wiring substrate .A new design of Flip-Chip Ball grid array (FCBGA) package is shown in the Fig.1 shows the detailed construction of FCBGA.

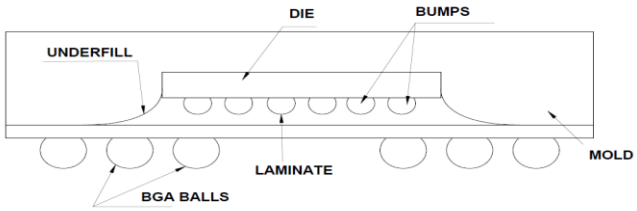

Fig. 1. Flip-Chip ball grade array construction

II. INTRODUCTION TO FINITE ELEMENT METHOD

The Finite element method (FEM) has devloped in to a key, indispnsable technology in the modelling and simulation of advanced engineering syatems in various fields like transportation, communication and building and so on [1]. This techinque has been applied over many years to solve problem of thermal analysis, structural analysis, fluid mechanics analysis ,electromagnetic analysis and many others. This strong and promising technique plays an important role in manufacturing processes of advanced engineering systems. Modelling and simulation of engineering system based on finite element method are two sophisticated processes which engineer go through the fabrication of final product. At the moment a large number of simulation software packages like Abaqus, Ansys, Adina, COMSOL etc. that implement finite element method are available. Engineers across the world use these simulation software packages to provide solution for many complicate design egineering problems that would otherwise be extremely difficult to obtain. The FEM is a numerical method seeking an approximate solution of distribution of field variables like the dispaclement in stress analysis or the

temperature in thermal analysis in the problem domain that is difficult to obtain analytically [2].

The basic steps involved in any finite element analysis consist of following:

1. Preprocessing Phase

a. Create and discretize the geometry or the solution domain into finite element, that is subdivide the problem into nodes and elements. Discretization of the problem domain into small elements is called meshing.
b. Assume a shape function to represent the the physical behavoiur of an element; that is an approximate continuous function is assumed to represent the solution of the elment.
c. Develope an equation for an element.
d. Assemble the elements to present the entire problem. Construct the globle stifness matrix.
e. Apply boundry conditions, initial conditions of loading

2. Solution Phase

a. Solve the set of linear or non-linear algebric equestions simulteneously to obtain nodal results, such as displacement values at different nodes or temperature values at different nodes in heat transfer problem

3. Processing Phase

a. Obtain other important information. At this point you may be interested in values of principle stresses, heat flux etc.

IV. Functions of Integreted Circuits

The function of an IC(Integrated circuits) chip is to replace many separate electronic components which could possibly have been used to build a perticular electronic circuit. Most of those separate components are replaced by just one tiny IC chip that has been manufactured to include extremely miniature circuits which imitate the behaviour of all those separate components. The main functions of IC are as follows:

1. Cost of manufacture: Using an IC saves the labour of soldering together all the separate components to make the equivalent circuit
2. Space: Using an IC saves the huge amount of space that the circuit would take up if it were built using separate components
3. Energy: Using an IC saves a lot of electrical energy compared to the same circuit built using separate components
4. Speed: Using an IC makes the circuit work much faster than it could ever do if it were built using separate component

III. Literature Survey on Flip Chip Ball Grid Array

A Flip Chip Ball Grade Array (FCBGA) is an electronic package formed by attaching the integrated circuit (IC) to the substrate. It is a special type of BGA package where the die is flipped in order to provide the shortest possible chip-to-package interconnection distance. This improves the electrical performance because it minimizes impedance, resistance and parasiting inductance. The functions of an FCBGA, like the function of any IC package are to protect power and cool the microelectronic device and to provide electrical and mechanical connections between the device and the outside world.

Paper 3 helped to study the electrical and mechanical connections between an IC and a substrate typically involving solder interconnections, although alternate material system can also be used. During the manufacturing of an FCBGA, materials are bonded at an elevated temperature and then the assembly is cooled back to room temperature because the material involved have different thermo mechanical properties. The bonding process introduces stresses and deformation in FCBGA Package as shown in Fig.1. A flip-chip package is directly attached to the substrate with solder pumps located between them. The severe thermal expansion mismatch between the silicon die and the substrate will introduce significant thermal stresses in the package, especially in small solder bumps. Under fill is usually used to fill the gap between solder bumps, hence improve the solder bumps reliability. Thermal stress-induced delamination along these interfaces could occur during thermal cycling. Thermal deformation of the package is directly related to its geometry and the material used in the package. Moiré interferometry is a whole-field optical interference technique with high resolution and high sensitivity for measuring the in-plane displacement and strain fields [3]. Recently, this method is successfully used to measure the thermal-mechanical deformation of electronic package with the objective to study the package reliability. Experimental results are also used for deciding the reliability of the package.

Paper 4 studied the commonly observed factors to limit model size. A two dimensional finite element model was built for a single unit in a Thermal Electric (TE) device. Such a model is justified as the thermal stresses are primarily planner. TE device future and thermal loadings were defined as model parameters in ANSYS so that sensitivity of thermal stresses to these design parameters can be investigated systematically with the aim to minimize the thermal stresses and maximize mechanical integrity. Additional model parameters include mesh densities which allows accurate capture of thermal stress when model dimensions and thermal loadings are varied. The actual values of these parameters are not all defined from the literature, especially material properties. Properties of the bonding and diffusion layers are not known and they were estimated based on given composition using rules of mixture. The elastic properties of the TE material are not known either and estimated crudely. The finite element model (FEM) is one of the most popular methods for engineering stress analysis. Following steps are used in the finite element analysis of the semiconductor diode:

1. Geometry
2. Elements , mesh and re-meshing
3. Material properties
4. Mechanical initial and boundary conditions
5. Thermal initial and boundary conditions
6. Analysis using ANSYS

Modern day requirement for high density packaging has led to a reduction in the package size. The main requirement is to have a greater number of I/O in a small area. This has led to the transition from peripheral to area array packages as shown in Fig.2. Examples of such area array packages are ball grid array (BGA), Flip Chip (FC) and chip scale packages (CSP). Here the package to board interconnections

is achieved by an area array of solder balls or columns using surface mount technology. This method of interconnection is generally used for package to board attachments. However the same method can also be used for forming interconnection between die and the substrate, which is a part of the package. This replaces the more conventional method of wire bonding and is used in flip chip BGA packages. One way to improve the performance of such packages to thermal loading (Cyclic/non-cyclic) is to have an epoxy under fill between the die and BT substrate, in the space between the solder balls. This under fill then acts as a thermal stress absorber around the solder balls, thereby reducing stress on the solder joints and improving fatigue life. The problem with this is that they most under fill materials have a tendency to absorb moisture the problem with this is that most under fill materials have a tendency to absorb moisture during pre-conditioning/storage[4]. Thermal Stresses are induced in electronic packages during various stages of their lifecycle. They can be due to manufacturing processes like solder reflow or thermal fluctuations during storage /Shipping or heat generation during use. Of these, the magnitude of the stress generated during the solder reflow process is very high, and the same in conjunction with vapor pressure often lead to package failure during the production phase. The shift in the electronic packaging industry towards lead free assembly methods due to environmental concerns has also contributed to this. It is because the peak reflows temperatures for lead free solder alloys are generally higher (approx. 250°C) than that for eutectic Pb-Sn solder (approx. 220°C). The following figure describes the three dimensional directional deformation of IC chip package for the thermal stresses induced in it. Fig.2 shows the total maximum deformation of stress in red color.

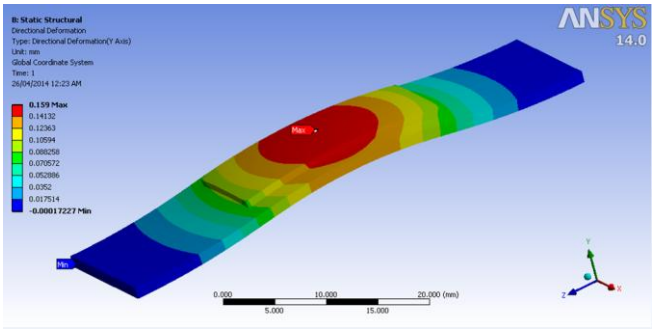

Fig. 2. Static Directional Deformation of IC Chip Package

Paper 5 studied that the recent advancement in high performance semiconductor packages has been driven by the need for higher pin count and superior heat dissipation. A one piece cavity lid flip chip BGA package with high pin count and targeted reliability has recently been developed by UTAC. The flip Chip technology can accommodate I/O count of more than five hundreds, and the die junction temperature can be reduced to a minimum level by metal heat spreader attachment. To design joints in engineering structures, it is necessary to be able to analyses them. This means to determine stresses and strains under the given loading, and to predict the probable points of failure .During the last two decades many of the existing adhesive bonding processes, as well as soldering and brazing have been simulated by numerical methods, especially by finite element methods. The finite element method, this day a commonly used method, is well suited to the estimation of stresses in joint of almost any geometrical shape. A numerical simulation of adhesive bonding, soldering or brazing is not easy, it is a complex process involving the interaction of thermal, mechanical and metallurgical phenomena the mechanics of material interfaces is still a challenge to researches working in the field of mechanics of solids. This paper gives a review of published papers dealing with the finite element methods applied in the areas of adhesion bonding.it also includes the fundamentals and review of adhesion bonding relationship between adhesion and mechanical properties, the mechanics of bonded joints 2D and 3D linear and non-linear finite element analysis material and geometrical nonlinear analysis also viscoelastic and viscoplastic analysis creep analysis, dynamic response of bonded joints ,adhesive contact problem with debonding, stress distribution in an adhesive layer ,design of bonded joints.

Paper 6 studied that the silicon substrate has a significant effect on the inductance parameter of a lossy interconnect line on integrated circuit .It is essential to take this into account in determining the transmission line electrical parameters. This paper specifically illustrate the electrostatic modeling of single and coupled interconnected lines on a silicon-silicon oxide substrate .Also we determine the quassi-static substrate spectral for the potential distribution of the Silicon-integrated circuit. Due to complexity of electromagnetic modeling, researchers and scientist always look for development of accurate and fast method to extract the parameters of electronic interconnects and packages structure. Also this paper investigates thermal stress in a multi-layered thermal electric device for power generation where high temperature gradient is expected. A parametric 2D plane strain finite element model was built with different thermal and elastic properties in each layer .Thermal boundary conditions were imposed on the finite element model to mimic thermal loading in actual applications. The predicted temperature field was fed into a stress finite element model to derive the thermal stress distribution which was then compared against material strength. For determining the material strength the thermal conductivity of the material is main important factor. Following table describes the thermal conductivity of the various materials which are used as the semiconductor or insulator in IC chip package.

Table 1;ROOM TEMPERATURE THERMAL CONDUCTIVITY OF SEMICONDUCTORS AND INSULATORS

Material	Thermal Conductivity (W/m.k)
Silicon(Bulk)	148
Germanium(Bulk)	60
Silicon (74NM)	47
Silicon(10NM)	13
Sio2(Bulk)	1.38
SiO2(100 nm)	0.95

III. DISCUSSION

This paper presents the detailed discussion between the low thermal conductivity of TE materials and high thermal conductivity of the rest of a TE device results in a fairly uniform temperature distribution outside the TE material but the sharp temperature gradient through the TE material. The analysis performed in this work provides an insight on the order and distribution of stresses encountered in FC package due to hygroswelling and solder reflow. Also the use of flip chip solder bumps interconnect has shortened the electrical path between the silicon chip and the chip carrier significantly in addition the FCBGA package is able to exhibit high heat dissipation capability with low thermal resisitance.with the over modeled structure which increases the rigidity during process handling, the core substrate can be used for improved electrical performances. Further developments of FCBGA package design include expanding to different package sizes and thickness, and the evaluation of the new design as a multi-chip module. This paper provides a list of literature references on finite element applications in adhesive bonding, soldering and brazing. The emphasis of this paper is to list, first of all, papers published in the various international journals and discuss them in the manner of use of advance technology in the IC chip packaging in details.

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