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Designing Of Current Mode Instrumentation Amplifier For Bio-Signal Using 180nm CMOS Technology

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Abstract

This paper describes the design of current mode instrumentation amplifier (CMIA) for bio-signal Acquisition system. The CMIA topology is based on voltage mode operational amplifier (op amp) power supply current sensing technique. Op amp mismatch and precise current mirrors are two design challenges of this topology. A new low-voltage single-power high CMRR and PSRR instrumentation amplifier is developed for biomedical applications. The proposed circuit uses a new structure to solve the conventional circuits problems. The overall proposed circuits by virtuoso 6.1.5 using UMC 0.18um CMOS technology achieve a very high CMRR 130dB up to 87 HZ and higher than 100dB up to 10k Hz and PSRR 110 dB up to 1k Hz and 39 dB closed loop gain at 1.8V single power supply.

Index Terms—*Analog integrated circuits, bio signal amplifier, Low noise, low-power circuit design, CMRR, PSRR.*

I. Introduction

Recording the biomedical electronics is one of the challenges in a biomedical electronics detection system because the biomedical signal has a very weak amplitude and low frequency, usually of few Millis - volts or less and the Frequency below 1 KHz [4]. The biomedical electronics detecting system is shown in Fig. 1.which consists of electrodes, amplifier, LPF, Sample and hold (S/H) and ADC Meanwhile the recording electrodes might pick up many others unneeded interferences or artifact signals. However, the biomedical electronics is too weak to detect, therefore, we need a high gain, accurate, and high CMRR amplifier to reduce the common mode noise and to amplify the biomedical signal only. Then, the signal is passed through LPF, S/H and ADC to become a digital signal. After that, these digital data will be processed in

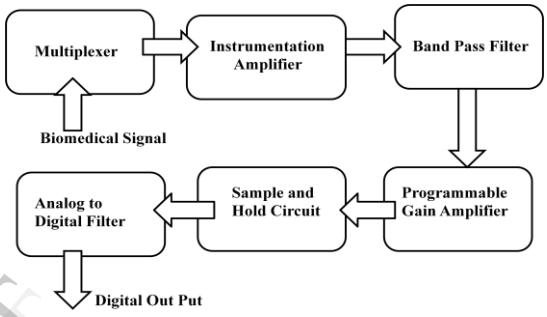

Figure1. The Biomedical Electronics Detecting System Blocks

PCs or microprocessors In order to extract the small low frequency differential Signals out from large common mode interference of human body, a well designed instrumentation amplifier (IA) is essential. The IA should issue low input noise, high power supply rejection ratio, controllable voltage gain and high common mode rejection ratio [5]. Hence, the circuit is expected to be implemented in a modern integrated circuit technology. Current mode instrumentation amplifier (CMIA) has many advantages compared with traditional voltage mode one, such as no complex resistor network, gain bandwidth product(GBW) independent voltage gain and high CMRR which is independent of differential gain.

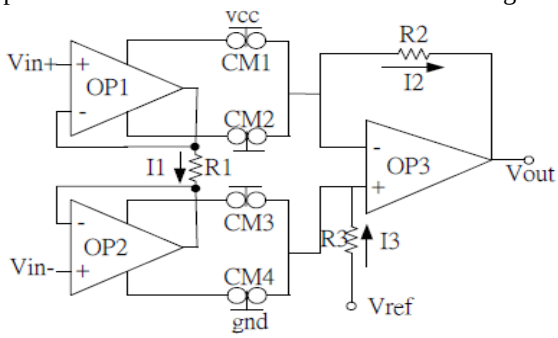

Figure 2.Current mode instrumentation amplifier topology

The CMIA topology involves operational amplifier (op amp) power supply current sensing technique is first reported by B. Wilson as a second generation current conveyor (CCII) in 1984 and then developed as a current mode amplifier and an instrumentation amplifier in 1989. Later and recently, this CMIA is further developed and reported by many works [1]-[3].A comprehensive and detailed analysis of this CMIA is given in [4]. However it only concerns effect on CMRR due to input op amp mismatch and gives measurement results of discrete circuit implementation. There is still lack of detailed design using this circuit topology. This paper describes the design of such a CMIA in a CMOS 0.18µm technology.

II. Instrumentation Amplifier

The instrumentation amplifier is used in many electrical systems where there is a need for the amplification of small differential sensor voltages. However, the differential sensor signal is often accompanied by interference in the form of common-mode voltages at the inputs [2].An Amplifier with high CMRR is suitable for such applications. Such amplifier with programmable gain and high input impedance is an instrumentation amplifier [1, 2, 3].The most common instance is the three-op-amp differential amplifier with resistive feedback. A serious drawback of such configuration is that a good CMRR performance is related to resistors matching. Some resistors must be trimmed accurately to reduce the common-mode gain, hence increasing the cost of the IA.

III. The Proposed Instrumentation Amplifier

To solve the problems in resistors network matching of a conventional IA, the number of resistors must be reduced first [2, 3]. So we propose a new IA circuit structure to improve the problems of a conventional IA. The proposed IA consists of three OP-AMPs, current mirrors and few resistors as shown in Fig. 2.which is the schematic of the proposed CMIA topology. This CMIA consists of two input op amps A1 and A2 and a resistor R1 as the differential input stage. A1 and A2 are connected as unit gain buffers to convey the input voltages on resistor R1. Since common mode voltages at the two terminals of R1 is expected to be equal to each other, only differential current $I_1 = \frac{V_{in+} - V_{in-}}{R_1}$ flows through. Current mirrors CM1 and CM2 will copy a Current (I2) as accurate as (I1) through R2.therefore, we will get I1 = I2 = -I3. The output voltage is to spread out in Eq.1 with the schematic of the proposed IA shown in Fig. 3

$$V_{out} = -2\,[(\,V_{in+}) - (V_{in-})]\frac{R_2}{R_1} \qquad (1)$$

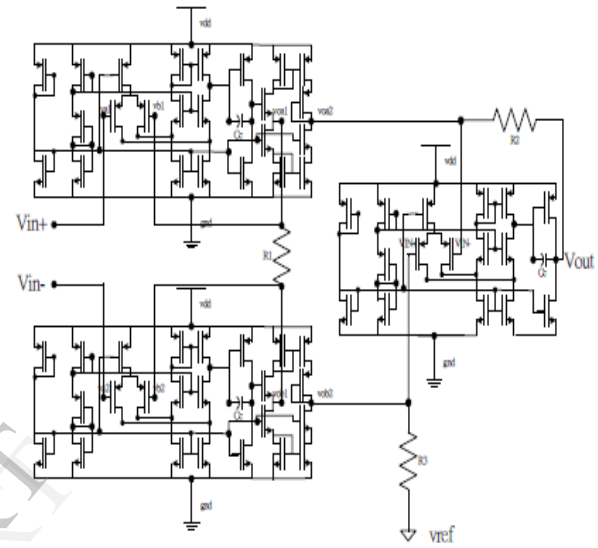

Figure3. Schematic of the proposed Instrumentation amplifier

The overall CMRR of instrumentation amplifier is give by a following equation.2

$$CMRR = \frac{A_D}{A_{CM}} = \frac{A_{OL1} * A_{OL2}}{A_{OL1} - A_{OL2}} \qquad (2)$$

If the open loop-gains of the input op-amps are different, a finite CMRR will result. The magnitude can be approximated by Equation (2).To achieve a high CMRR, either very high open-loop gains must be achieved, or the open-loop gains must be tightly matched. Since extremely high open-loop gains are difficult to achieve in low-voltage CMOS processes, the open-loop gains of input op-amp must be tightly matched. In order to obtain two identical op-amps, a great deal of time and effort was spent in the layout phase of design.

The input referred noise must be very small for efficient acquisition of the signal which traditionally asks for larger power consumption [7,8]. Typically the cortical ECG magnitude varies from 20 µV to 5 mV. Noise of such amplifiers must be sufficiently lower than smallest input signal. However these systems are really limited by the background noise. Power savings

can be achieved if input referred noise of the amplifier can be based on the background noise. The schematic of the OPAMP is shown in Fig. 4. PMOS with large gate area is used as the differential input pair to reduce flicker noise contribution by them. The low noise design needs careful sizing and biasing of the input transistors and the load. The noise contribution of different transistors [9] can be reduced by referring to Eqn. 3, Eqn. 4 and table 1.

$$Thermal\ Noise\ PSD = i_{n,th}^2 = 4 * k_B * T * \gamma * g_m \quad (3)$$

$$Flicker\ Noise\ PDS = i_{n,1/f}^2 = \frac{K}{C_{ox} * W * L} * g_m^2 * \frac{1}{f} \quad (4)$$

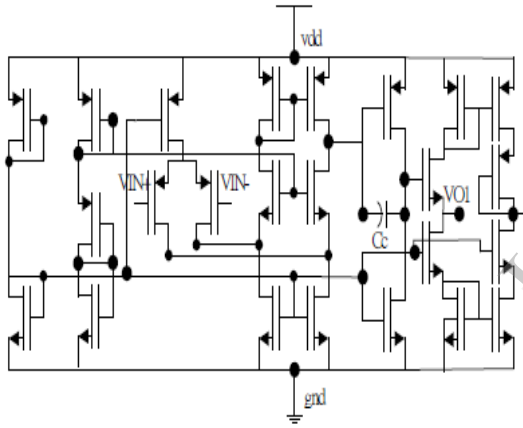

Figure 4. Schematic of the proposed input Amp of Instrumentation amplifier

Flicker noise is caused mainly due to the interface trap density in NMOS and mobility fluctuations in PMOS. It is a major concern when designing low frequency circuitry .PMOS is the preferred choice for the input transistors as flicker noise is found at least one order lower than that of NMOS [7]. Flicker noise can be reduced by increasing the active area of the transistors and by decreasing $g_{m,load}/g_{m,in}$ ratio for load transistor. The input transconductance has to be maximized (large W/L) to achieve this, for a given current. Flicker noise can also be reduced using circuit techniques as correlated double sampling, chopper stabilization switched biasing etc. But they complicate the architecture and cause additional power consumption. Flicker noise contribution of input transistor pair can only be reduced by increasing the gate area (Table. I).

Table 1
Input referred noise optimization

Input Referred Noise	Input	Load
Thermal Noise $v_{n,in}^2$	$\alpha \frac{1}{g_{m,in}}$	$\alpha \frac{g_{m,load}}{g_{m,in}^2}$
Flicker Noise $v_{n,in}^2$	$\alpha \frac{1}{w_{in} * L_{in}}$	$\alpha \frac{g_{m,load}^2}{g_{m,in}^2} * \frac{1}{w_{load} * L_{load}}$

Hence (Win * Lin) product and (Win /Lin) ratio of input pair has to be increased. The noise from other transistors is reduced mainly by decreasing their transconductance with respect to the input transconductance. Traditionally it is done by decreasing their W/L ratio and giving more overdrive voltage for a given bias current. But a limit is superimposed on this method by the output swing, especially for submicron CMOS technologies. In our noise reduction technique, we have further reduced the transconductance of load transistors by reducing bias current through them.

The voltage-in and current-out of the proposed OP-AMP construction is shown in Fig.4[6] which is composed of four stages, the first stage is a bias circuit and the differential PMOS is used for the input of the second stage. The differential stage is designed by a folded cascade configuration to increase the open loop gain and to adjust the input common mode voltage of OPAMP easily [6]. The third stage provides a high gain stage. Finally, the last stage of the output stage has VO1 and VO2 as outputs .The specifications of the proposed OP-AMP is shown in table2

Table.2 Simulation results of the input CMOS op-amp

Parameters	Results achieved
Technology	0.18µ
Supply voltage	1.8 v
Bandwidth	184HZ
Power consumption	50µ W
Open loop Gain(dB)	75.39dB
Phase margin	66˚
CMRR	93.3dB
PSSR	100dB
Input referred noise	5.6µv/sqrt (Hz)
Unity gain bandwidth	1.004MHZ
Gain margin	17dB

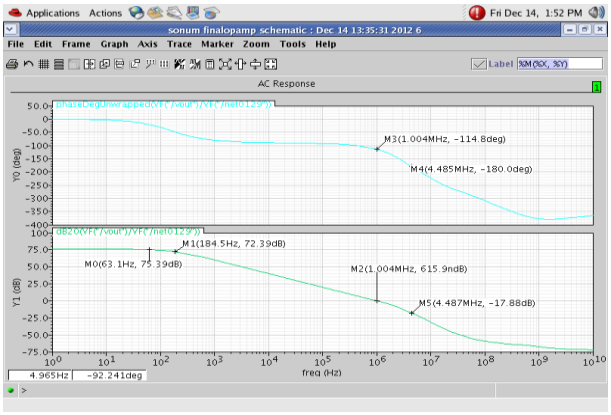

Fig.5 Frequency response of input op - amp .

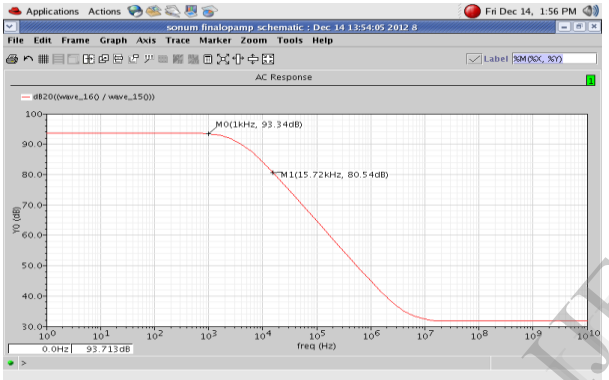

Fig. 6 CMRR frequency response of input op-amp.

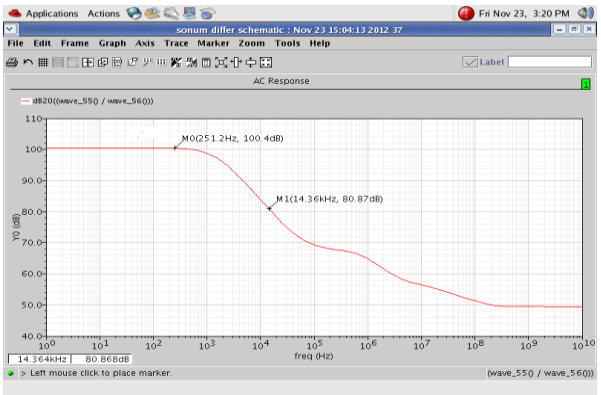

Fig. 7 PSRR frequency response of input op- amp.

IV. Simulation Results of Instrumentation Amplifier

The instrumentation amplifier is designed with the CMOS 0.18 µm technology. Fig. 5 contains the open-loop gain of op-amp1 (op-amp2) which is 75dB.The simulations are performed with Spectre in analog environment. Fig.8 is the frequency response of instrumentation amplifier which has close loop gain close to 40 dB and the unity gain bandwidth is around 15.5MHz.The CMIA keeps a CMRR (Fig.9) 130dB up to 87 Hz and higher than 100dB up to 10k Hz which satisfies the basic standard of medical instruments. Fig 10 shows CMIA holds PSRR higher than 100dB up to 10k Hz. Fig. 11 shows the noise performance. For those applications concerning the signal band lower than 0.1 Hz, the chopping technique is required to further reduce the noise within this frequency band. The result of the transient IA simulation is shown in Fig.12 the input is a pulse wave signal with 100Hz frequency and 1mV amplitude. Table 3 gives a summary of the simulation Results.

Table.3 Simulation result of the CMOS instrumentation amplifier

Parameters	Results achieved
Technology	0.18µ
Supply voltage	1.8 v
Bandwidth	453k HZ
Power consumption	355µ W
Closed loop Gain(dB)	39. 06dB
Phase margin	51˚
Gain margin	16˚
Unity gain bandwidth	15.28M Hz
CMRR(from 1m Hz to 87Hz)	130 dB
CMRR(from 87 Hz to 10kHz)	>100dB
PSSR	110 dB
Input referred noise@1Hz	2.314µv/sqrt(Hz)
Input referred noise@10k	57nv/sqrt(Hz)
Slew Rate	+0.8v/µs, -0.8v/µs
Settling time	500ns

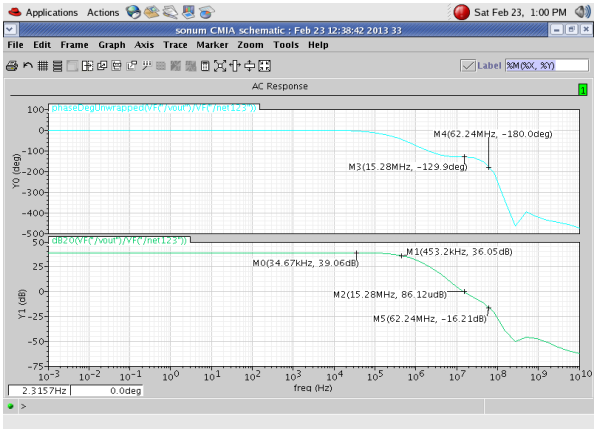

Fig.8 Frequency response of instrumentation amplifier

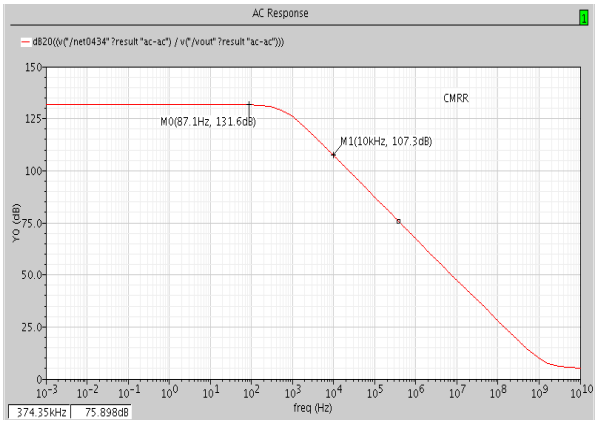

Fig.9 CMRR Frequency response of instrumentation amplifier

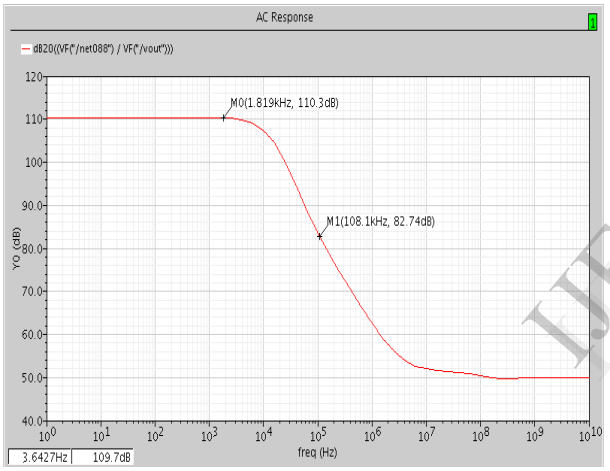

Fig.10 PSRR frequency response of instrumentation amplifier

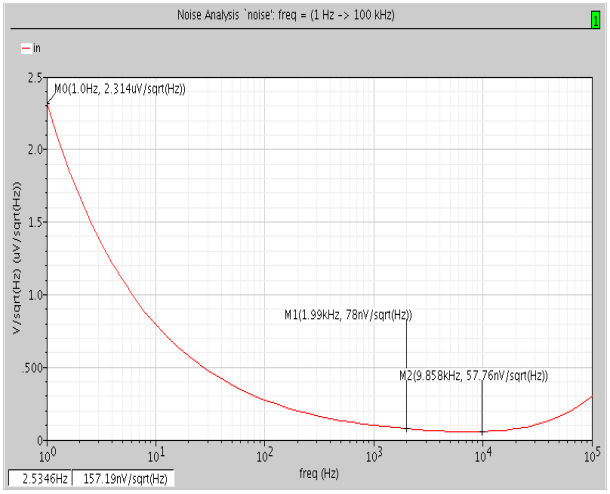

Fig. 11 Equivalent input noise voltage of instrumentation amplifier

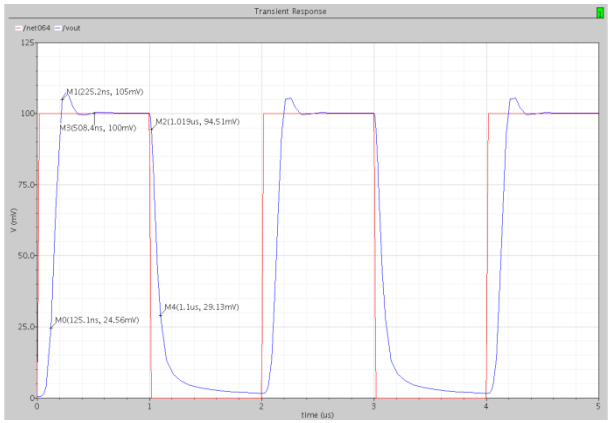

Fig. 12 Transient response of instrumentation amplifier

V. Conclusion

A current mode instrumentation amplifier using op amp power supply current sensing technique for bio-signal acquisition system is implemented and analyzed in a CMOS 0.18µm technology. The proposed circuits combine current mirrors that can deal with the problem of resistors matching as in the conventional instrumentation amplifier circuits. Simulation results show that the CMIA demonstrates continuous GBW-independent gain adjustment function and good signal distortion performance. The circuit has 130 dB CMRR up to 87 Hz and keeps a value higher than 100 dB up to 10k Hz and Input noise voltage is 57nv/$\sqrt{HZ}$at 10k Chopping technique is required to further Reduce input noise voltage lower than 0.1 Hz. The CMIA consumes only 355 µ W under a 1.8 V dc supply voltage which is suitable for bio-signal application .The circuit does not require advanced op amp design but the matching between op amps plays an important role in layout phase. The accurate current mirror is the main challenge in schematic phase for higher CMRR and better signal quality.

VI. Acknowledgement

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