Designing and Implementation of Low Power SPI-Switch Interface on FPGA

Sukhwinder Kaur Student, Deptt. Of ECE Amritsar College of Engg. & Technology Amritsar, Punjab ,India

Abstract— This paper describes an approach for reducing the dynamic power consumption of SPI-4-port switch interface by using RTL clock gating technique and analyzing the performance parameters of the interface on different Lattice FPGA families. The SPI is a full duplex serial data communication protocol (designed by Motorola) which uses four wires i.e. MOSI, MISO, SS and SCLK for establishing a communication between host processors and its peripherals. It operates either as a master or a slave. The master provides the clock signal and determines the status of the slave select signal to communicate with the other devices. A four port switch is used for programming the SPI control registers. The architecture consists of a 4-port switch having registers, single port RAM, SPI, SPI clock generator, Data selector and gated clock block. The RTL code and test-bench verification are carried out on Modelsim Altera v6.3 and performance analysis is carried out on Lattice Diamond XP2 FPGA families i.e. LFXP2-5E,8E,17E AND 30E.

Keywords—SPI, I2C, ICG, FPGA

I. INTRODUCTION

The physical transfer of data over a point-to-point or point to point multipoint communication channel is called as data communication. For example computer buses, storage media etc. [1]. On the basis of signals data can be analog (continuous) or digital (discrete).

Data transmission can be carried out in two ways either parallel or serial. In case of serial data transmission data is transmitted one bit at a time, using a clock to maintain integrity between words. For eg SPI, I2C, UART, RS-232 etc. In case of parallel data transmission data is sent parallel. For eg. Printer communication, ISA, IDE, SCSI etc. Serial data transfer is quite advantageous as compared to parallel data transfer. In serial communication wiring is simpler and there is less interaction between the conductors of serial cables [2].

II. SERIAL PERIPHERAL INTERFACE

A. Operation

Serial peripheral interface (SPI) is a serial bus standard protocol designed by Motorola (also known as microwire). SPI is a synchronous serial data link protocol that operates in full duplex mode and is available on popular communication processors and microcontrollers. The SPI bus is a 3+N wire interface where N is the number of devices connected to a single master on the bus. Only one master can be on the bus. Fig 1 shows SPI master –slave communication [3][4].

Narinder Sharma Head of Department. Deptt. Of ECE and EE Amritsar College of Engg. & Technology Amritsar, Punjab ,India

SPI operates in two modes: master and slave. To begin a communication SPI-master first generates SCLK. according to the baud rate register. The master then pulls SS (Slave Select) low for the desired chip. SS is an active low signal.

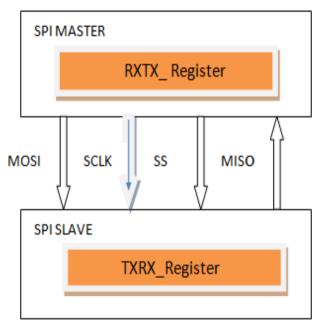


Figure 1 SPI master-slave communications

Transmission normally involve two shift registers of some given word size(eight bits), one in the master and one in the slave i.e. TXRX_register and RXTX_register notations used in RTL code. [1]. Data is usually shifted out with the MSB first, while shifting a new LSB into the same register. After that register has been shifted out, the master and slave have exchanged register values. Then each device takes that value and write it to memory. Transmissions may involve any number of clock cycles. Transmissions often consist of 8-bit words, and a master can initiate multiple such transmissions if it is required. [5] [6].

There are 2 types of SPI configurations i.e. Independent slave configuration and daisy chain configuration. In the independent slave configuration, an independent slave select line is available for each slave. This is the way in which the SPI is normally used. Since the MISO pins of the slaves are connected together, they are required to be tri-state pins. Whereas in daisy chain configuration the whole chain act as a SPI communication shift register. Such a feature only requires a single SS line from the master rather than a separate SS line [12].

III. RTL CLOCK GATING

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The RTL clock gating is a technique which is used to control power dissipated by clock net. In digital synchronous circuits clock (net) is the main factor for dynamic power dissipation. RTL clock gating reduces the unwanted switching on the parts of clock net by disabling the clock [7].

Clock gating works by taking the enable conditions attached to the registers and uses them to gate the clocks. Hence it is required that a design must contain these enable conditions in order to use clock gating. This clock gating process can also save significant die area as well as dynamic power, since it removes large numbers of multiplexers and replaces them with clock gating logic. This clock gating logic is generally in the form of "Integrated clock gating" (ICG) cells. [8][9].

RTL Clock gating logic can be added into a design in a variety of ways:

- 1. RTL coding: Can be coded into the RTL code as enable conditions that can be automatically translated into clock gating logic by synthesis tools.
- 2. Manually inserting into the design by the designers (module level clock gating) by instantiating library specific ICG (Integrated Clock Gating) cells to gate the clocks of specific modules or registers.
- 3. Semi-automatically inserted into the RTL by automated clock gating tools. [10].

IV. SYSTEM INTERFACE

The Figure 2 shows the proposed system overview of SPI-Switch interface.

The system architecture consists of six blocks. The gated clock block is used for reducing the dynamic power consumption of the whole design. The data device selector is used to select either RAM or Switch at a time for communication with SPI. Switch is a 4-port device which is used to program the SPI control register. It consists of 3 registers. Destination address registers gives the information about the output ports of the switch.

There are 4 output ports of the switch. Last two bits of this registers decides the output port. Then comes control register which is used to control the 4-port switch operation and SPI control register having bits namely CPOL, CPHA, LSBFE and SPI-enable.

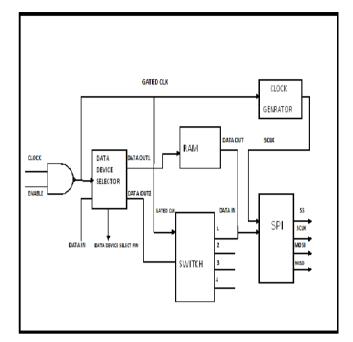


Figure 2 SPI-Switch block interface

RAM is used for storing the received and transmits data for SPI. Clock generator is used to generate the SPI clock according to the baud rate register and SPI is used for serial communication.

V. RESULTS AND SIMULATIONS

Figure 3 shows the hierarchal view of the SPI-Switch interface on Lattice Diamond FPGA.



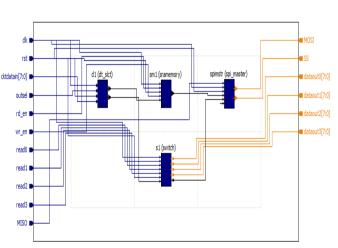


Figure 3 Hierarchal view of SPI-switch interface on XP2 FPGA

The whole design is synthesized on Lattice Diamond XP2 FPGA families i.e. LFXP2-5E, LFXP2-8E, LFXP2-17E and LFXP2-30E for the calculation of area, dynamic power, total dynamic power and power consumption by logic blocks.

The blue blocks are the main blocks i.e. data selector, SPI, Switch and RAM. The blue lines are the input ports and wires and orange lines are the output ports.

The Figures 4 shows the performance analysis of the non-gated architecture on LFXP2-5E.

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		Clocks I	I/O I/O Term E	lock RAM 1	DSP PLL DO	QSDLL Graph	Report			
evice						Environment				
iamily:	Lattice)/P2	•	Speed grade:	6	•			Them	al Profile	
evice:	LFXP2-SE	•	Operating conditions:	Commercial	•	Ambient Tempe	ient Temperature(°C): 25			
ackage type:	TQFP144	٠	Part Names:	LFXP2-SE-6T	N144C •	Effective Theta-JA:		13.76		
levice Power P	Parameters					Junction Temp	erature(°C):	27.00		
Process Type:	Typical	•	Power File Revision:	Final		Maximum Safe	Ambient(°C):	82.7		
Voltage/Dyna	mic Power Mult	pler	Current by Pow	er Supply		Power by Powe	r Supply		Power by Block (W)	Peak Startup (A)
-	Voltage	DPM	Static (A) D	ynamic (A)	Total (A)	Static (W)	Dynamic (W)	Total (W)	Logic Block	0,0071
Vcc	1.200	1.0	0 0.0143	0.0069	0.0212	0.0171	0.0083	0.0254	Clocks	0.0041
Vccio 3.3	3.300	1.0	0.0000 0	0.0000	0.0000	0.0000	0.0000	0.0000	VO	0.1041
Vccio 2.5	2.500	1.0	0 0.0109	0.0103	0.0212	0.0272	0.0258	0.0530	Block RAM	0.0007
Vccio 1.8	1.800	1.0	0.0000	0.0000	0.0000	0.0000	0.0000	0.0000	DSP	0.0002
Vccio 1.5	1.500	1.0	0.0000 0	0.0000	0.0000	0.000	0.0000	0.0000	PLL	0.0017
Vccio 1.2	1.200	1.0	0 0.0013	0.0000	0.0013	0.0016	0.0000	0.0016	DOSDLL	0.0000
Vccaux	3.300	1.0	0 0.0171	0.0017	0.0189	0.0566	0.0057	0.0623	Mise	0.0271
Vccpll	3.300	1.0	0 0.0005	0.0000	0.0005	0.0017	0.0000	0.0017	Total	0.1451
Vccj	1.200	1.0		0.0000	0.0010	0.0012	0.0001	0.0013		
			0.0451	0.0190	0.0641	0.1052	0.0399	0.1451		

OMBINATORIAL		AF (%)	#Logic LUTs	# Dist. RAM	#Ripple Slices	# Registers	Dyn. Pwr (W)
	175.0000	10.0000	145	0	0	0	0.0020
SCLK_c	50.0000	10.0000	6	0	0	18	0.0003
ck_c	100.0000	10.0000	46	24	8	62	0.0020

Figure 4 Performance analysis of non-gated architecture on LFXP2-5E device

Figure 5, 6 and 7 shows the performance analysis of nongated architecture on other XP2 FPGA families.

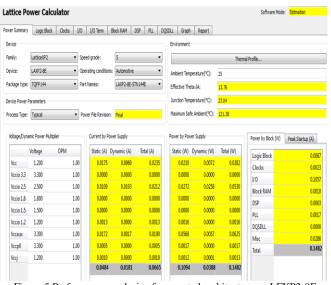


Figure 5 Performance analysis of non-gated architecture on LFXP2-8E device

tice Po		alacol							Sottware Mod	ie: Estimation
er Summary	Logic Block	Clocks I/C	I/O Term	Block RAM	DSP PLL (DQSDLL Grap	h Report			
vice			4			Environmen				
	Lattice)/P2			5						
mily:			peed grade:	_	•	Thermal Profile				
vice:	LAXP2-17E	Americ imperante(ru); 23								
ckage type:	pe: PQFP208 ▼ Part Names: LAXP2-17E-SQN208E ▼ Effective Theta-3A: 15.07							15.07		
vice Power P	arameters		27.47							
ocess Type:	Typical	•	Power File Revisi	no: Final		Maximum Si	afe Ambient(°C):	119.52		
iccas type.	Types:		oner ne neva	na <mark>ma</mark>						
bltage/Dyna	mic Power Multip	lier	Current by	Power Supply		Power by Po	wer Supply		Power by Block (W)	Peak Startup (A)
	Voltage	DPM	Static (A)	Dynamic (A)	Total (A)	Static (W)	Dynamic (W)	Total (W)		
Vec	1,200	1.00	0.024	2	0.0307	0.029	2	0.0368	Logic Block	0.013
Vccio 3.3	3,300	1.00	0.000	0.0000	0.000	0.0000	0.0000	0.0000	Clocks	0.003
1000 515	21244									
Veria 25	2 500		0.010	0.0102	0.0212			0.0000	1/0	0.10
	2,500	1.00	0.010		0.0212	0.0272	0.0258	0.0530	I/O Block RAM	
Vccio 1.8	1.800	1.00 1.00	0.000	0.0000	0.0000	0.0272	0.0258	0.0530		0.00
Vccio 1.8 Vccio 1.5	1.800 1.500	1.00 1.00 1.00	0000.0	0.0000	0.0000 0.0000	0.0272 0.0000 0.0000	0.0258	0.0530	Block RAM	0.00
Vccio 1.8 Vccio 1.5	1.800	1.00 1.00	0.000	0.0000	0.0000	0.0272	0.0258	0.0530	Block RAM DSP	0.00 0.00 0.00
Vccio 1.8 Vccio 1.5 Vccio 1.2	1.800 1.500	1.00 1.00 1.00	0000.0	0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.0000 0.000000	0.0000 0.0000	0.0272 0.0000 0.0000	0.0258 0.0000 0.0000 i 0.0000	0.0530	Block RAM DSP PLL	00.0 00.0 00.0 00.0
Vccio 2.5 Vccio 1.8 Vccio 1.5 Vccio 1.2 Vccaux Vccpll	1.800 1.500 1.200	1.00 1.00 1.00 1.00	0.000	0.0000 0.0000 0.0000 0.0000 0.0017	0.0000 0.0000 0.0013	0.0272 0.0000 0.0000 0.0016	2 0.0258 0.0000 0.0000 0.0000 0.0000	0.0530	Block RAM DSP PLL DQSDLL Misc	00.0 00.0 00.0 00.0 00.0 86.0
Vccio 1.8 Vccio 1.5 Vccio 1.2 Vccaux	1.800 1.500 1.200 3.300	1.00 1.00 1.00 1.00 1.00	0.000	0.0000 0.0000 0.0000 0.0000 0.0017 0.0000	0.0000 0.0000 0.0013 0.0205	0.0272 0.0000 0.0000 0.0016 0.0016	0.0258 0.0000 0.0000 0.0000 0.0000 0.0057 0.0000	0.0000 0.0000 0.0000 0.0016 0.0078	Block RAM DSP PLL DQSDLL	0105 0000 0000 0000 0000 0000 0000 0000

Figure 6 Performance analysis of non-gated architecture on LFXP2-17E device

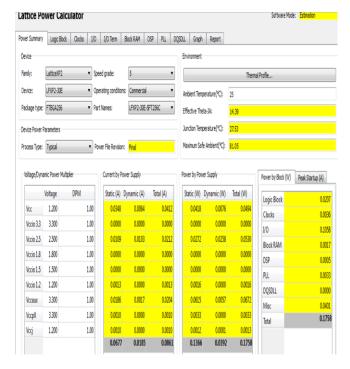


Figure 7 Performance analysis of non-gated architecture on LFXP2-30 E device

The performance parameters to be taken under observation are dynamic power (clock frequency, power supply and logic blocks) and area (number of LUTs). Similarly the performance analysis of the non-gated architecture is carried out on LFXP2-8E, 17E and 30 E.

Table 1 show the area and power calculation of the design on different logic families.

Lattice	Area(LUTs)	Dynamic	Total	Power
FPGA		Power (Dynamic	consumption
XP2		clock	power	(Logic blocks)
Family		frequency)	(Power	W
		mW	supply)	
			mW	
LFXP2-	197	4.2	39.9	0.1451
5E				
LAXP2-	197	3.7	38.8	0.1482
8E				
LAXP2-	197	3.7	39.0	0.1637
17E				
LFXP2-	197	3.7	39.2	0.1758
30E				

Table -1: Area and power calculation of non-gated design

Fig.8 shows the hierarchal view of gated SPI-Switch interface. The whole design is synthesized on Lattice Diamond XP2 FPGA families i.e. LFXP2-5E, LFXP2-8E, LFXP2-17E and LFXP2-30E for the calculation of area, dynamic power, total dynamic power and power consumption by logic block.

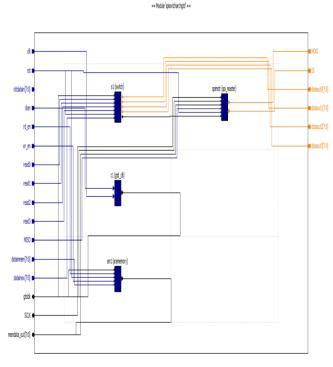


Figure 8 Hierarchal view of gated architetcure

In fig.8, blue blocks are the main blocks i.e. Gated clock, SPI, Switch and RAM. The blue lines are the input ports and wires and orange lines are the output ports.

The Figures 9 shows the performance analysis of the gated architecture on LFXP2-5E.

wer Summary	Logic Block	Clodis	0,1	I/O Term	Block RAM	DSP	PLL	DQSDL	. Graph	Report					
levice								8	nvironment						
amily:	Lattice)/P2		▼ Sp	eed grade:	6		ļ.	•			Therm	al Profile			
evice:	LFXP2-SE		• 0;	erating condition	s: Commerci	al			mhient Terro	erstire/91.	25				
ackage type:	TOFP144		▼ Pa	rt Names:	LFXP2-SE	-6TN 144	к		Ambient Temperature(°C): 25 Effective Theta-JA: 13.76						
-					(ACCESSION OF ACCESSION OF ACCE	(Dirents)									
levice Power P	arameters		_					_		erature(°C);	26.83				
rocess Type:	Typical		• Po	wer File Revision	: Final			Ņ	laximum Safe	Ambient(°C):	82.87				
Voltage/Dyna	mic Power Mult	pler		Current by Pi	wer Supply			PC	wer by Powe	er Supply		Power by Block (W)	Peak Startup (A)		
	Voltage	DPM		Static (A)	Dynamic (A	To	tal (A)	1	Static (W)	Dynamic (W)	Total (W)				
Vec	1.200		1.00	0.0142	0.005	2	0.019	¥	0.0171	0.0062	0.0233	Logic Block Clocks	0.0068		
Vccio 3.3	3.300		1.00	0.000	0.000)	0.000	0	0.0000	0.000	0.000	VO			
Vccio 2.5	2.500		1.00	0.0091	0.007	}	0.017	0	0.0227	0.0197	0.0424	Block RAM	0.0939 0.0007		
Vccio 1.8	1.800		1.00	0.000	0.000)	0.000	0	0.0000	0.0000	0.000	DSP	0.0002		
Vccio 1.5	1.500		1.00	0.000	0.000)	0.000	0	0.0000	0.0000	0.0000	PLL	0.0017		
Vccio 1.2	1,200		1.00	0.0026	0.000)	0.002	6	0.0031	0.0000	0.0031	DQSDLL	0.000		
Vccaux	3.300		1.00	0.0171	0.0014		0.018	5	0.0565	0.0045	0.0610	Misc	0.0271		
Vccpll	3.300		1.00	0.0005	0.000)	0.000	15	0.0017	0.000	0.0017	Total	0.1327		
Vccj	1.200		1.00	0.0010	0.000)	0.001	0	0.0012	0,0001	0.0013	To can			
				0.0445	0.014	4	0.05	90	0.1023	0.0304	0.1327				
	wer Calci												e: <mark>Calculation</mark>		

```
Power Summary Logic Block Clodes I/O I/O Term Block RAM DSP PLL DQSDLL Graph Report
```

Clock Name	Freq. (MHz)	AF (%)	#Logic LUTs	‡Dist. RAM	#Ripple Slices	#Registers	Dyn. Pwr (W)
COMBINATORIAL	175.0000	10.000	144	0	0	0	0.0022
SCLK_c	50.0000	10.000	б	0	0	18	0.0002
gtdclk_c	100.0000	10.000	29	24	8	46	0.0015
tal Dynamic Power (W						
Total Dyn. Pwr (W							
0,003							

Figure 9 Performance analysis of gated architecture on LFXP2-5E

Figure 10, 11 and 12 shows the performance analysis of gated architecture on other XP2 FPGA families.

The performance parameters to be taken under observation are dynamic power (clock frequency, power supply and logic blocks) and area (number of LUTs). Similarly the performance analysis of the gated architecture is carried out on LFXP2-8E, 17E and 30 E.

ttice Po	wer Calo	ulator										Software	Mode: Estimation	
ver Summary	Logic Block	Clocks	I/O	I/O Term	Block RAM	DSP	PLL	DQSDLL	Graph	Report				
evice								Envi	ronment					
miy:	LatticeXP2		Spee	d grade:	5						Them	al Profile		
evice:	LAXP2-8E		oper	ating conditions	Automoti	ie		Amb	Ambient Temperature(°C);		25			
eckage type:	TQFP144		• Parti	Names:	LAXP2-8E	E-STN144	E 1	Effe	Effective Theta-JA: 13		13.76			
evice Power P	Parameters							Jun	tion Temps	erature(°C):	26.89			
rocess Type:	Typical		• Pow	er File Revision:	Fnal			Max	inum Safe	Ambient(°C);	121.53			
••••	mic Power Mult			Current by Po			. 1785		r by Powe		T . 100	Power by Block (W) Peak Startup (A)	
	Voltage	DPM		Static (A) [tal (A)			Dynamic (W)	Total (W)	Logic Block	0.0083	
Vcc	1,200		.00	0.0175	0.005		0.0232		0.0210	0.0069	0.0279	Clocks	0.0023	
Vccio 3.3	3.300		.00	0.0000	0.000		0.0000		0.000	0.0000		1/0	0.0954	
Vccio 2.5	2,500	1	.00	0.0091	0.007	9	0.0170		0.0227	0.0197	0.0424	Block RAM	0.0010	
Vccio 1.8	1.800	1	.00	0.0000	0.000	0	0.0000		0.000	0.0000	0.0000	DSP	0.0003	
			0	0.000	0.000	0	0.0000		0.000	0.0000	0.0000	PLL	0.0017	
Vccio 1.5	1500	1	-						0.0031	0.000	0.0031			
Vccio 1.5 Vccio 1.2	1500 1.200		.00	0.0026	0.000	0	0.0026				010022	DOSDLL	0.000	
		1	_	0.0026 0.0172	0.000 0.001		0.0026		0.0568	0.0045	0.0613	DQSDLL Misc	0.0000	
Vccio 1.2	1.200	1	.00			4			0.0568		0.0613	Misc	0.0000 0.0286 0.1376	
Vccio 1.2 Vccaux	1.200 3.300	1	.00 .00	0.0172	0.001	4	0.0186			0.0045	0.0613		0.0286	

Figure 10 Performance analysis of gated architecture on LFXP2-8E

Software Mode:

Lattice Power Calculator

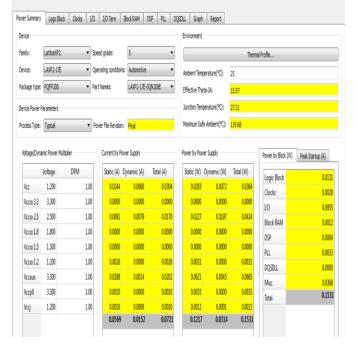


Figure 11 Performance analysis of gated architecture on LFXP2-17E

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		culator							Software M	ode: <mark>Estmation</mark>
er Summary	Logic Bloc	k Clocks I/O	I/O Term	Block RAM	DSP PLL D	QSDLL Graph	Report			
evice						Environment				
miy:	LatticeXP2	▼ Spe	ed grade:	5	•			Therm	al Profile	
evice:	LFXP2-30E	▼ Opi	erating condition	s: Connercial	•	Anbient Tercerature(°C): 25				
clage type: FTBGA256 🔹 Part Names: LFXP2-30E-SFT256C 🔹						Effective Theta-JA: 14,39				
evice Power P	Darametere					Junction Temp	erature(°C):	27.38		
ocess Type:		▼ Po	ver File Revisio	n: Final		Maximum Safe		81.2		
Voltage/Dyna	enic Power Mu	tpler	-Current by P	ower Supply		Power by Powe	r Supply		Power by Block (W	Peak Startup (A)
										/ concernance (rid
	Voltage	DPM	Static (A)	Dynamic (A)	Total (A)	Static (W)	Dynamic (W)	Total (W)		0.0204
Vec	Voltage 1.200	DPM 1.00	Static (A) 0.0347	Dynamic (A) 0.0061	Total (A) 0.0409	Static (W) 0,0417	Dynamic (W) 0.0074	Total (W) 0.0491	Logic Block Clocks	
	-				17		,		Logic Block	0.0204
Vcc	1.200	1.00	0.0347	0.0061	0,0409	0.0417	0.0074	0.0491	Logic Block Clocks	0.0204 0.0036
Vcc Vccio 3.3	1.200 3.300	1.00 1.00	0.0347 0.0000	0.0061	0.0409	0.0417 0.0000	0.0074	0.0491 0.0000	Logic Block Clocks 1/0	0.0204 0.0036 0.0955
Vcc Vccio 3.3 Vccio 2.5	1.200 3.300 2.500	1.00 1.00 1.00	0.0347 0.0000 0.0091	0.0061 0.0000 0.0079	0.0409 0.0000 0.0170	0.0417 0.0000 0.0227	0.0074 0.0000 0.0197	0.0491 0.0000 0.0424	Logic Block Clocks 1/0 Block RAM	0.0204 0.0036 0.0955 0.0017
Vcc Vccio 3.3 Vccio 2.5 Vccio 1.8	1.200 3.300 2.500 1.800	1.00 1.00 1.00 1.00	0.0347 0.0000 0.0091 0.0000	0.0061 0.0000 0.0079 0.0000	0.0409 0.0000 0.0170 0.0000	0.0417 0.000 0.0227 0.0000	0.0074 0.0000 0.0197 0.0000	0.0491 0.0000 0.0424 0.0000	Logic Block Clocks 1/0 Block RAM DSP	0.0204 0.0036 0.0955 0.0017 0.0005
Vcc Vccio 33 Vccio 25 Vccio 18 Vccio 15	1.200 3.300 2.500 1.800 1.500	1.00 1.00 1.00 1.00 1.00	0.0347 0.0000 0.0091 0.0000 0.0000	0.0001 0.0000 0.0079 0.0000 0.0000	0.0409 0.0000 0.0170 0.0000 0.0000	0.0417 0.0000 0.0227 0.0000 0.0000	0.0074 0.0000 0.0197 0.0000 0.0000	0.0491 0.0000 0.0424 0.0000 0.0000	Logic Block Clocks VO Block RAM DSP PLL	0.0204 0.0036 0.0955 0.0017 0.0005 0.0003
Vecio 33 Vecio 25 Vecio 18 Vecio 15 Vecio 12	1200 3300 2500 1.800 1.500 1.200	1.00 1.00 1.00 1.00 1.00 1.00	0.0347 0.0000 0.0091 0.0000 0.0000	0.0051 0.0000 0.0079 0.0000 0.0000	0,0409 0,0000 0,0000 0,0000 0,0000 0,0000	0.0417 0.0000 0.0227 0.0000 0.0000 0.0001	0.0074 0.0000 0.0197 0.0000 0.0000 0.0000	0,4491 0,0000 0,4424 0,0000 0,0000 0,0000	Logic Block Clocks VO Block RAM DSP PLL DQSDLL	0.0204 0.0036 0.0955 0.0017 0.0005 0.0005 0.0005 0.0000
Vcc Vccio 33 Vccio 25 Vccio 18 Vccio 15 Vccio 12 Vccio 12	1.200 3.300 2.500 1.800 1.500 1.200 3.300	100 100 100 100 100 100 100 100	0.0347 0.0000 0.0091 0.0000 0.0000 0.0005 0.0186	0.0051 0.0000 0.0079 0.0000 0.0000 0.0000	0,000 0,0000 0,000 0,000 0,000 0,000 0,000 0,000 0,000 0,000 0,000 0,000 0,000 0,000000	0.047 0.0000 0.0227 0.0000 0.0000 0.0001 0.0015	0.0074 0.0000 0.0197 0.0000 0.0000 0.0000 0.0000	0,0491 0,0000 0,0424 0,0000 0,0000 0,0000 0,0001 0,0660	Logic Block Clocks VO BlockRAM DSP PLL DQSDLL Misc	0.004 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.005 0.004 0.004

Figure 12 Performance analysis of gated architecture on LFXP2-30E

Table 2 shows the area and power calculation of the design on different logic families.

Lattice	Area(LUTs)	Dynamic	Total	Power
FPGA		Power (Dynamic	consumption
XP2		clock	power	(Logic blocks)
Family		frequency)	(Power	W
		mW	supply)	
			mW	
LFXP2-	179	3.9	30.4	0.1327
5E				
LAXP2-	197	3.4	31.1	0.1376
8E				
LAXP2-	197	3.4	31.4	0.1531
17E				
LFXP2-	179	3.4	31.6	0.1651
30E				

Table 2 Area and power calculation of gated design

VI. CONCLUSION

A practical comparative study of SPI-SWITCH interface has been discussed in this paper. This comparison is limited to the SPI-master-SWITCH interface with gated and non-gated architectures. The research work has shown up the results of FPGA implementation of gated and non-gated SPI- SWITCH interface. Total area and total dynamic power consumption (due to clock frequency, power supply and logic blocks) of gated SPI-Switch interface is less as compared to non-gated architecture. A difference of 9.9 mW in case of total dynamic power and 18 LUTs in case of area has been observed. Gated SPI-switch interface has shown up improvement in overall area and dynamic power consumption. So, overall the designing and implementation of low power SPI-SWITCH interface on FPGA XP2 is carried out successfully.

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