Designing a New Topology of Cascaded Multilevel Inverter for High Voltage Applications

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Abstract - ***In this paper a new topology of cascaded multilevel inverter is proposed. Function of the multi-level inverter is to synthesize a desired voltage wave shape from several levels of DC voltage. The proposed topology of cascaded multilevel inverter is based on sub multilevel converter unit and full-bridge inverter. The proposed topology significantly reduces the number of dc voltage sources, switches, IGBTs, and power diodes as the number of output voltage levels increases. Then, the structure of the proposed topology is optimized in order to utilize a minimum number of switches and dc voltage sources, and produce a high number of output voltage steps. The operation and performance of the proposed multilevel converter have been evaluated with the simulation results of a single-phase 62-level inverter using MATLAB simulink environment.***

I.INTRODUCTION

Multilevel inverters have been drawing growing attention in the recent years especially in the distributed energy resources area due to the fact that several batteries, fuel cells, solar cell, wind, and micro turbines can be connected through a multilevel inverter to feed a load or the ac grid without voltage balancing problems. Another major advantage of multilevel inverters is that their switching frequency is lower than a traditional inverter, which means they have reduced switching losses.

The multilevel inverters synthesize a desired stepped output voltage waveform by the proper arrangement of the power semiconductor devices from several lower dc voltage sources. The main advantage of multilevel inverters is the use of mature medium power semiconductor devices, which operate at reduced voltages. Also, the output voltage has small voltage steps, which results in good power quality, low-harmonic components, and better electromagnetic Compatibility.

There are three different basic multilevel inverter topologies: neutral point clamped (NPC) or diode clamped, flying capacitor (FC) or capacitor clamped, and cascaded H-bridge (CHB). The FC and NPC inverters require an excessive number of storage capacitors for a high number of voltage steps.

The CHB topologies are a good solution for high-voltage applications due to the modularity and the simplicity of control. But, in these topologies, a large number of separated voltage sources are required to supply each conversion cell. To reduce the number of separate dc voltage sources for high-voltage applications, new configurations have also been presented.

This paper presents a sixty two level cascaded H-bridge multilevel inverter based on Sub multilevel converter and a full bridge inverter. Compared with the existing cascaded multilevel inverters, the proposed cascaded multi level inverters can significantly reduce the switch count as well as the number of gate drivers as the number of voltage levels increases. Simulation results are included to

verify the operating principle of the proposed multilevel inverters.

II. PROPOSED CASCADED MULTI LEVEL INVERTER TOPOLOGY

As mentioned earlier, proposed topology involves sub multilevel and full bridge converters. Fig.1 shows the proposed topology for a sub multilevel converter, which consists of the basic unit and a full-bridge converter. The basic unit consists of *n* dc voltage sources. Each dc voltage source is connected to the output by two switches.

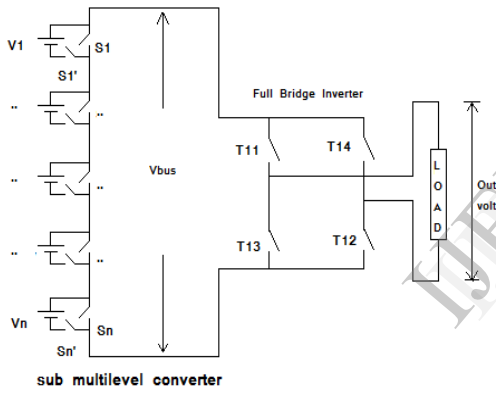

Fig 1: Proposed cascaded multilevel inverter

This basic unit can able to produce a zero or positive polarity voltage. As shown in Fig.1, each switch is composed of an insulated gate bipolar transistor (IGBT) with an anti parallel diode. Both switches, *Si* and *Si'* (for $i = 1, 2, \ldots, n$), are complementary controlled on the entire operation cycle. The basic unit produces a staircase voltage waveform with positive polarity. The output voltage of the basic unit can be equal to each dc voltage source or binary, ternary or *n*'nary combinations of the dc voltage sources.

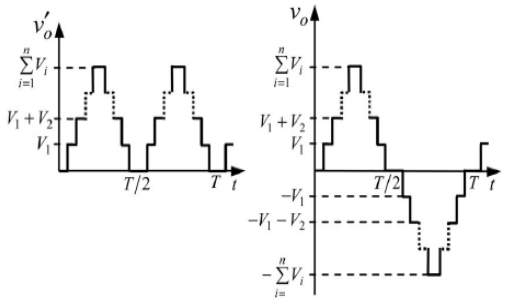

Fig 2: Output wave forms of basic circuit topology

Therefore, the maximum number of output voltage steps for *v'o* is equal to $2n - 1$. The output side of the basic unit is connected to a single-phase full-bridge converter, which alternates the input voltage polarity and provides a positive or negative staircase waveform at the output. The full-bridge switches, *T11*, *T12*, *T13* and *T14* are also complementary controlled.

By operating the sub multilevel converter switches in a proper sequence high number of output steps can be obtained. The typical output waveforms of *v'o* and *vo* are shown in Fig.2

A. MODIFIED SWITCHING SCHEME

The modified switching scheme can be best explained by an example. Consider a Cascaded MLI supplied by unequal but integer multiple sources. Let their magnitudes be 10 V, 20 V and 40 V, 80V, 160V respectively. In the modified switching scheme, the H-bridges are turned on and off to produce a 10 V step at each step of the produced staircase voltage. The magnitudes of the each cell are an arithmetic progression. The voltage source in the system with the smallest magnitude is the 10 V source. The voltages in the output of the MLI can be made equal at steps in the following way. The circuit diagram of the proposed model is shown in figure 3.

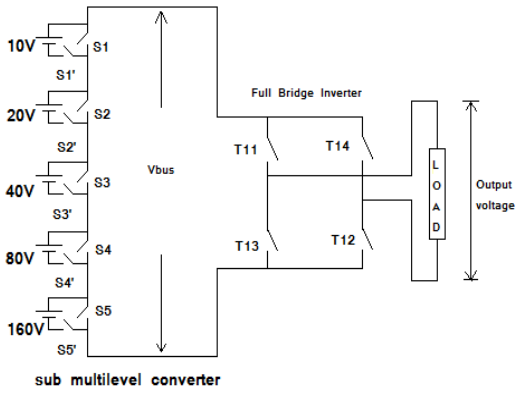

Fig 3: Proposed CMLI fed by unequal dc sources

B.SUB MULTILEVEL CONVERTER

Sub multilevel converter unit is formed by connecting a number of half-bridge cells in series with each cell having a voltage source controlled by two power semiconductor switches as shown in the Figure 4.

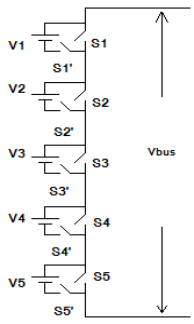

Fig 4: Sub multilevel Converter Unit

The two power semiconductor Switches will operate in a toggle fashion. Low on resistance and fast switching capability, low voltage power semiconductor are utilized in each cell source to reduce the inverter cost or to provide a high bandwidth sinusoidal output voltage. The power semiconductor switches are triggered by proper switching signals to produce multi level DC-link bus voltage which is indicated by V_{bus} in the circuit diagram.

The semiconductor switches are operated in a proper sequence to get the desired voltage. The first step in the voltage is zero volts, the second step is 10V, the third step is 20 V and the fourth is 30 V and increased linearly by 10V. The S series switches are used to short circuit the corresponding voltage source. Similarly the S' series switches are used to include the corresponding voltage source in the bus voltage. To obtain zero voltage at sub multilevel unit, the switches from S1-S5 are in working state. In this manner the 30V is obtained by operating the S1', S2', S3, S4, S5 in on state.

Various modes of switching sequence is given in the table 1 to produce DC bus voltage V_{bus} with the shape of stair case with steps, where n is the number of cell sources that is given to the Full bridge inverter. This table describes the working states of each power semiconductor switches for the various voltage levels.

SWITCH STATE

	SW NO / MODE	S1	S1'	S2	S2'	S3	S3'	S4	S4'	S5	S5'
0	I	1	0	1	0	1	0	1	0	1	0
0.00016	II	0	1	1	0	1	0	1	0	1	0
0.00032	III	1	0	0	1	1	0	1	0	1	0
0.00048	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....	.....
0.00952	VII	1	0	0	1	1	0	1	0	0	0
0.00968	VIII	0	1	1	0	1	0	1	0	1	0
0.00984	IX	1	0	1	0	1	0	1	0	1	0
0.01											

1 - ON
0 - OFF

Table 1: Modes of switching sequences to produce stair case output

From the different modes given in table 1 switching signals are generated for the switches in sub

multilevel converter. The switching pulses are shown in Figure 5.

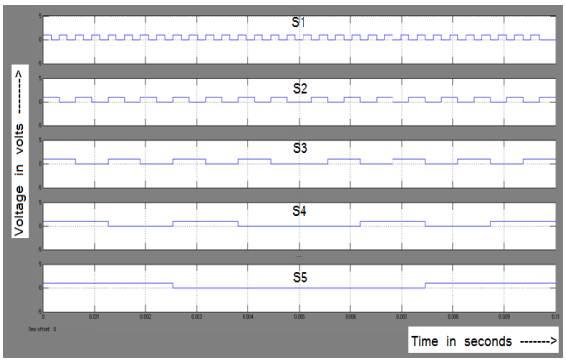

Fig 5: Switching signals for sub multilevel converter switches

C. FULL BRIDGE INVERTER

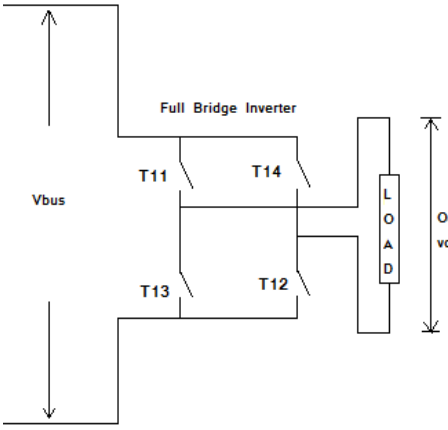

Fig 6: Full bridge inverter

The single phase full bridge (SPFB) inverter shown in Figure 6 consists of four power semiconductor switches T11-T14 which can switch at faster rates. The switches T11-T14 always work in pairs such that T11&T12 triggered for positive half cycle and T13&T14 will trigger with some delay to produce negative half cycle by operating the switches at the fundamental frequency of the output voltage (V_o).The switching signals for the full bridge inverter is shown in figure 7.

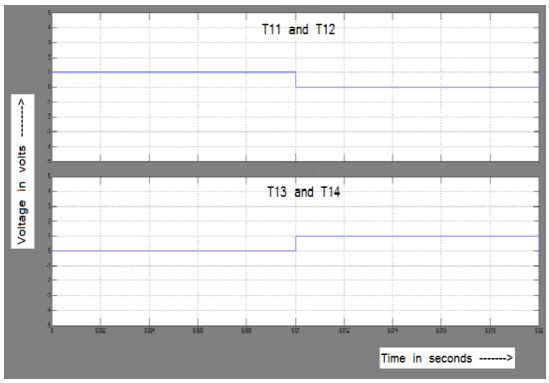

Fig 7: Switching signals for full bridge inverter

III.SIMULATION RESULTS

The operating principle of the proposed multilevel inverter was verified by conducting detailed simulation.

A. PROPOSED MULTILEVEL INVERTER FOR INDUCTIVE RESISTOR LOAD:

A single-phase 62-level cascaded H-bridge multilevel inverter simulation circuit for powering a inductive resistor load as shown in Figure 8. The load resistance is 107Ω and inductance is 55mh and the voltage of each DC source is set as per the circuit for an output frequency of 50Hz.

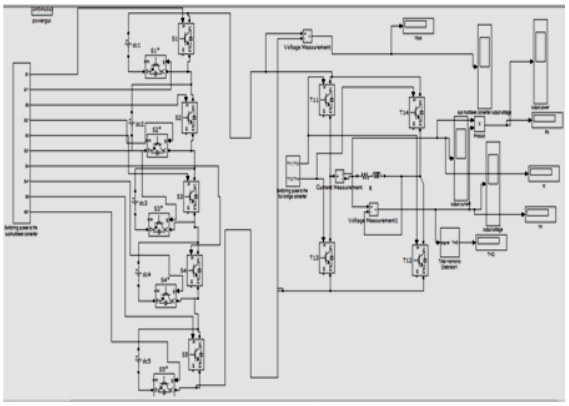

Fig 8: Simulation circuit of proposed multilevel inverter for resistive load

The simulated sub multilevel converter output voltage, AC output voltage of the inverter and AC output current are shown in Figures 8(a), 8(b) and 8(c) respectively.

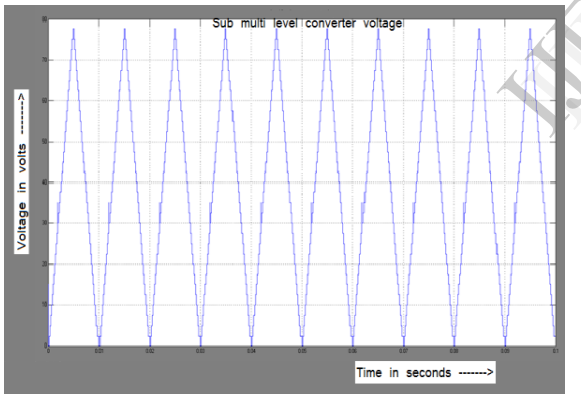

Fig 8(a): Sub multilevel converter output voltage for RL load.

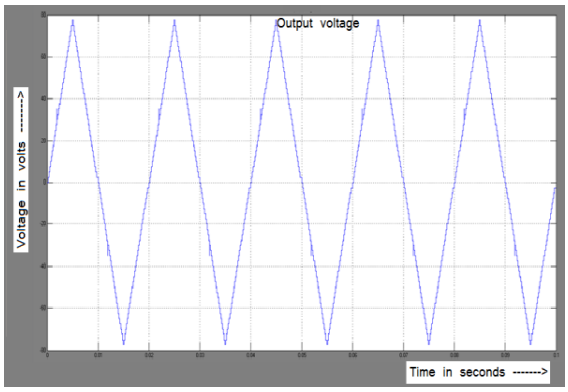

Fig 8(b): Proposed multilevel inverter output voltage for RL load.

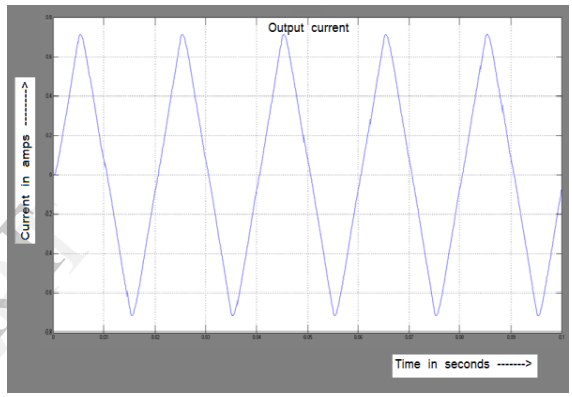

Fig 8(c): Proposed multilevel inverter output current for RL load.

B. COMPARISON WITH THE EXISTING SYSTEM:

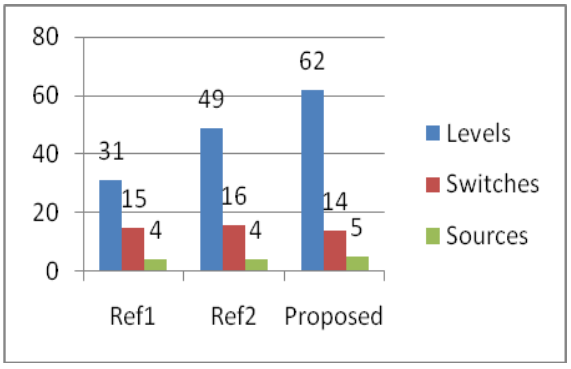

Fig 9: Comparison with existing systems

From the existing system, it is demonstrated that the proposed multilevel inverters can significantly reduce the component count with increased number of output level. Figure 9 plot a chart for comparison of the required number of switches, levels and sources between the proposed multilevel inverter with two existing systems.

IV. CONCLUSION

A new configuration for multilevel inverter has been proposed, which is based on the combination of sub multilevel converter and full bridge inverter. The proposed topology has been optimized in this paper for utilizing a minimum number of switches and voltage sources. It is shown that the proposed topology, not only has lower number of switches and components, compared to other topologies, but also the full-bridge converters operate at a lower voltage. The proposed topology can be a good solution for applications that require high power quality, or applications that have considerable numbers of dc voltage sources.

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