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Designing a 90nm CMOS OR Gate using Artificial Neural Networks (ANNs)

Jithendra Pulivarthi, Tammina Yasawini, Saipriya Nallamadugu
RM University,
AP

***Abstract*: Over the last few decades, this paper describes a method for simplifying electronic circuits by employing Complementary Metal Oxide Semiconductors (CMOS) transistors and mapping them to similar Artificial Neural Networks (ANNs). The implementation of such circuits in ANN results in software implementation of complicated circuits, which is less expensive than their hardware equivalent. In this research, a multiple layer ANN for the OR gate is utilized to control a previously constructed 90nm CMOS OR gate. Simple artificial neurons replace the transistors used in CMOS. The weights in this ANN are fixed, and negative weights are taken into account for the inverters.**

Keywords: Complementary Metal Oxide Semiconductors (CMOS), Artificial Neural Networks (ANNs), OR Gate

I. INTRODUCTION

In the recent forty years, Moore's law has been rapidly increasing VLSI arrangement through CMOS improvement scaling over the last forty years. Typically, the number of semiconductors in integrated circuits doubles after 18 to two years. This type of advanced scaling has worked well in the semiconductor sector, but in recent years, the speed of this scaling has slowed. Intelligent computing is becoming more prevalent in modern computing. Artificial Neural Networks (ANNs) are the greatest way to introduce intelligence into computers [1]. Research is being conducted to construct models that may be utilized in a wide range of applications such as medical informatics, handwriting recognition, speech recognition, and other pattern recognition applications [3]. By keeping the hardware basic, the creation of these models leads to the construction of more than 67 complicated circuits in software. These factors reduce the cost of these circuits. If ANNs are built in a way that is analogous to CMOS circuits, mapping ANNs to hardware circuits using CMOS becomes straightforward [5]. Forssell M has contributed to the field of hardware implementation of Artificial Neural Networks [1]. Some work has previously been done in this sector, including CMOS circuits that receive synaptic inputs and create a pulse width modulated output waveform of constant frequency based on activation level [2]. Based on supervised learning, logic gates were constructed in a single layer and a two-layer feed forward neural network [3]. Another technique employed Artificial Neural Network (ANN) to illustrate the manner in which the biological system was processed in the analogue domain by employing analogue components such as a Gilbert cell multiplier, an adder, and a neuron activation function for implementation [4]. Hui W et al worked on the use of artificial neural networks on segmented arc heather failure prediction [5].

II. CELL DESIGN

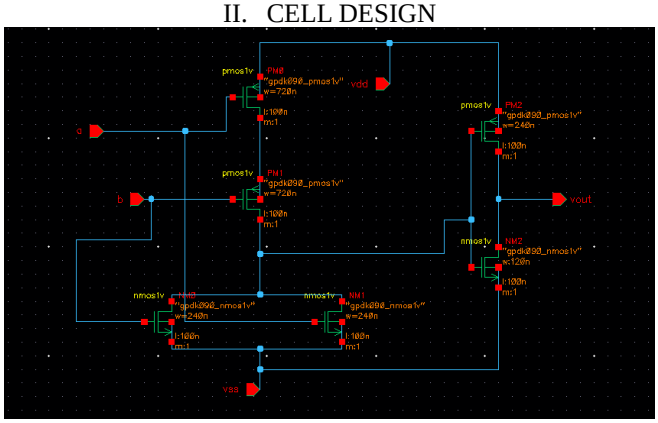

Fig.1.1 CMOS OR GATE Circuit Design

The CMOS OR gate is divided into two parts. The CMOS gate's top part is made up of two series-connected transistors. In the top section, P-MOS is employed. It is sometimes referred to as a pull up (PUN). A and B are the transistor's inputs, which are reversed before being linked to the transistor. The value of 'vdd' is always 1. The CMOS gate's bottom part is made up of two parallel-connected transistors. In the lower part, N-MOS is employed. It is sometimes referred to as pull down (PDN). The transistor inputs are A and B. The value of 'vss' is always 0. When A and B are both 0, the upper transistors in the series get inputs of 1.

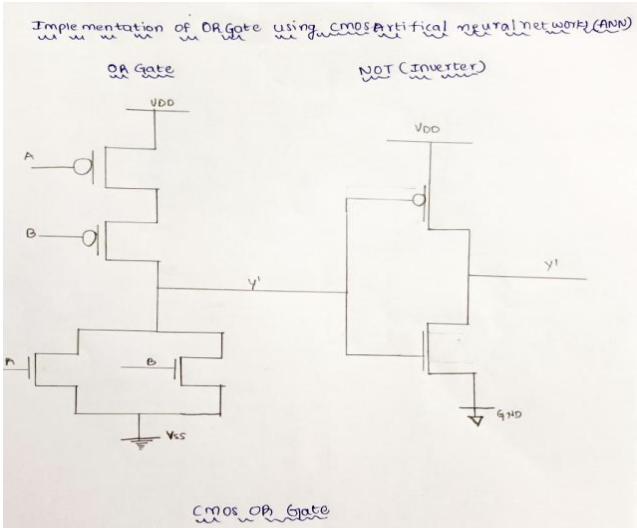

Fig.1.2 CMOS OR GATE

This frees up space for the 'vdd.' Because a NOT gate is linked further, the output will be 'vdd,' which is 1, and an inverted output will be generated.

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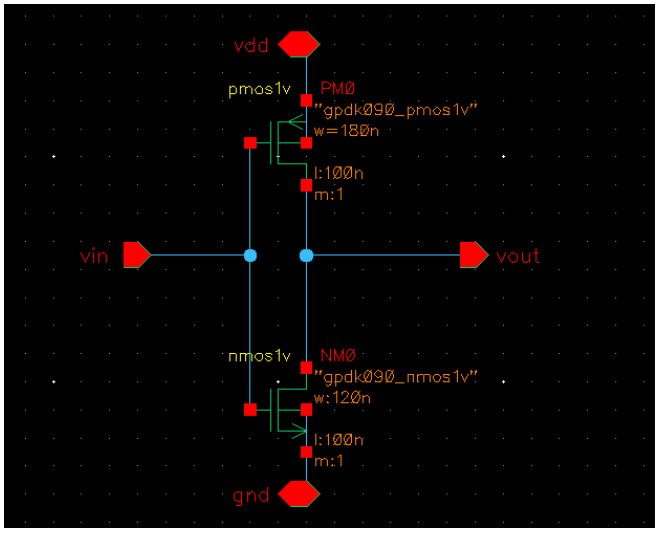


Fig.1.3 CMOS Not gate

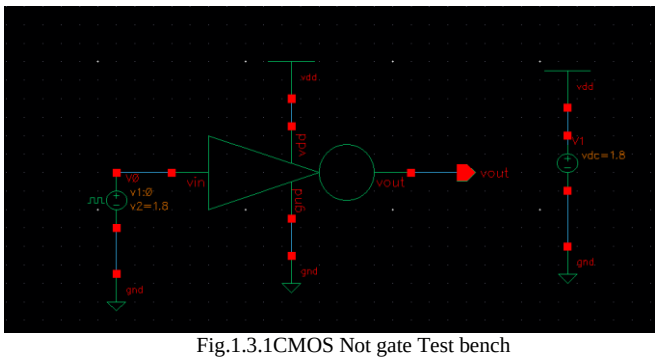
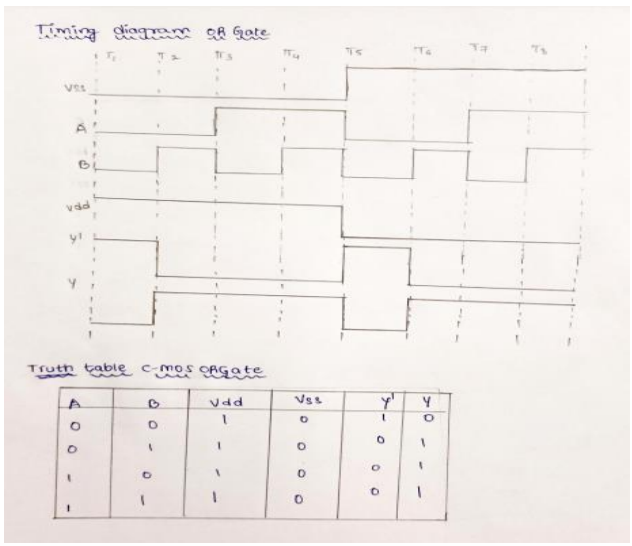


Fig.1.3.1CMOS Not gate Test bench

In the case of lower transistors, the 0 input in both parallel transistors prevent 'vss' from being used. When A=0 and B=1, the first higher transistor receives a 1 as input, while the second upper transistor receives a 0 as input and blocks the path for 'vdd' The first lower transistor receives a 0 and so blocks the path for 'vss.' The second lower transistor outputs 1 and makes room for 'vss.' The result will be 'vss' in this case. Similarly, as indicated in Fig.1.3, [5], the additional outputs received are the outputs of an OR gate.



A	B	Vdd	Vss	Y'	Y
0	0	1	0	1	0
0	1	1	0	0	1
1	0	1	0	0	1
1	1	1	0	0	1

Fig.1.4 Truth table and Timing diagram

III. PROPOSED WORK

In the case of an analogous ANN circuit, the OR gate already created using transistors and inverters is designed using a multiple layer Artificial Neural Network (ANN). Simple artificial neurons take the role of transistors. Negative weights are put on the links to replace the inverters. The ANN circuit is implemented using many layers of neurons. [5] OR gate.

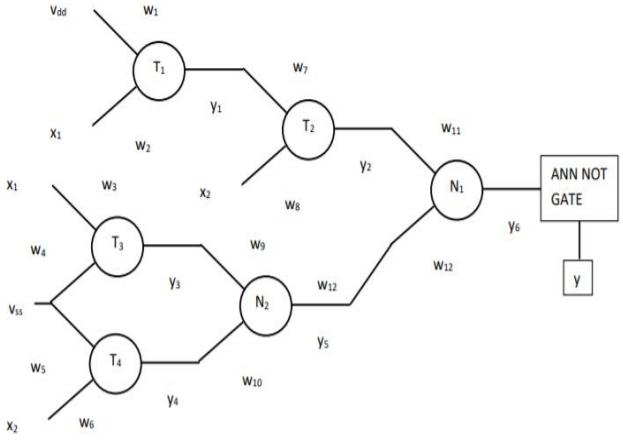


Fig.2.1 C-MOS OR Gate using multiple-layer ANN

Figure.2.1 depicts a multiple layer ANN, with T1 and T2 representing artificial neurons that represent two transistors linked in series. T3 and T4 are neurons that depict parallel-connected transistors. N1 and N2 are two straightforward neurons. A basic perceptron is one neuron, and a referee neuron is another. T1's weighted (w1 and w2) inputs are vdd and x1, with y1 as the output. T2's weighted (w7 and w8) inputs are y1 and x2, and its output is y2. T3's weighted (w3 and w4) inputs are x1 and vss, with y3 as the output. T4's weighted (w5 and w6) inputs and output are vss and x2, respectively [5].

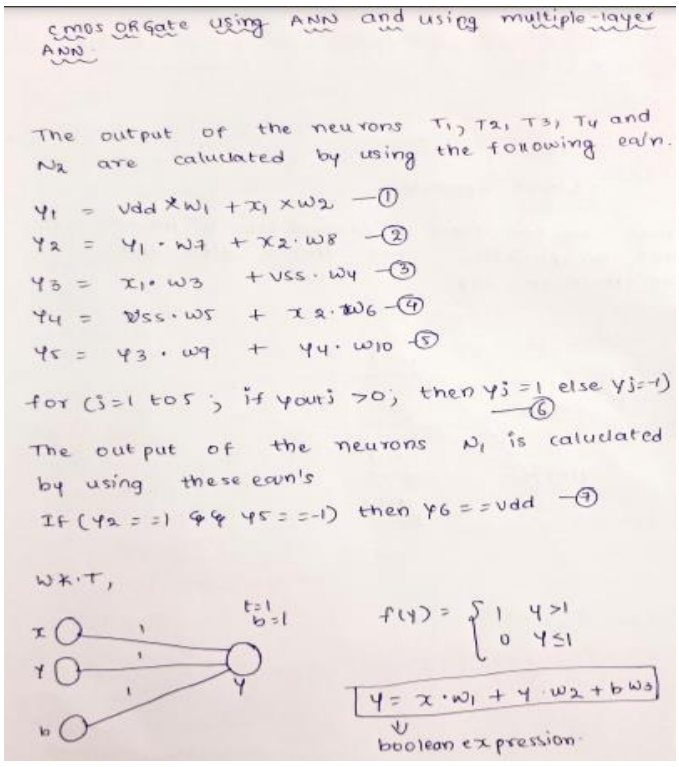


Fig 2.2 Methodology Multi-layer using ANN

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These ANNs are based on fundamental Self-Organizing Maps (SOMs), which use unsupervised learning. As a result, the synaptic weights are fixed in this location. When using inverted transistors, the weights are negative. Other weights are held constant at a positive value. As noted in the 75 introductions, work on this topic has already been done, however the work in this article is a method to creating extremely basic circuits. Simple circuits are easy to construct. This technology might be used in the future to simplify complex circuits for a number of applications.

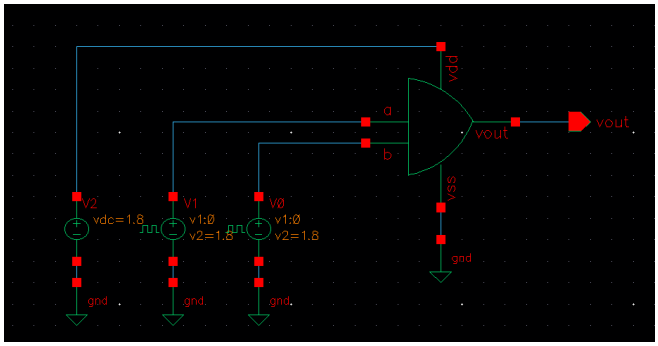

Fig.2.2.1 CMOS OR Gate Test bench

Only OR-Gate is covered here since the logic underlying OR-operation Gate's is mapped with CMOS OR-Gate, which is then mapped to a basic ANN; however, any sort of logic circuit may be mapped using ANN. The concepts of vdd and vss are discussed in detail here. As in CMOS OR-Gate, vdd is always binary '1' and vss is always binary '0'. With negative weight, the inverter function may be simply accomplished. Furthermore, focus is placed on mapping ANN circuits to replace complex electrical hardware circuits with ANN models that may be implemented in software.

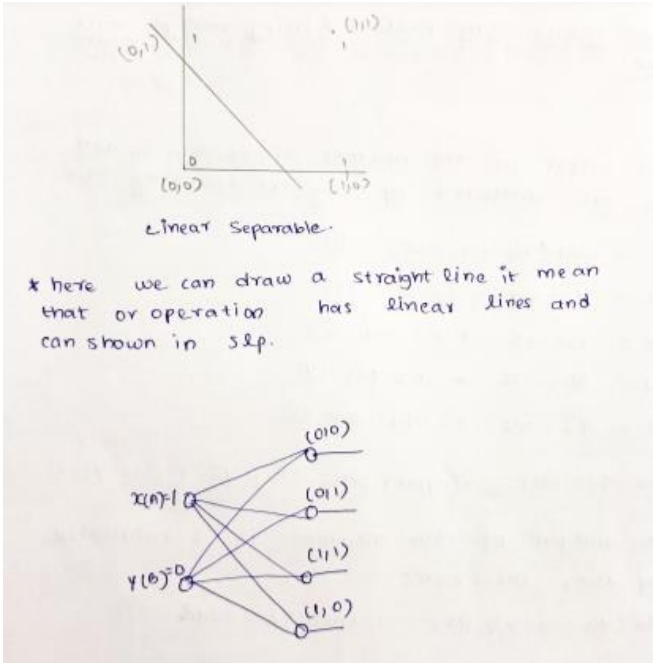

Fig.2.2.2 Methodology Multi-layer using ANN

Examples that calculate the inputs and outputs of the CMOS OR gate using ANN.

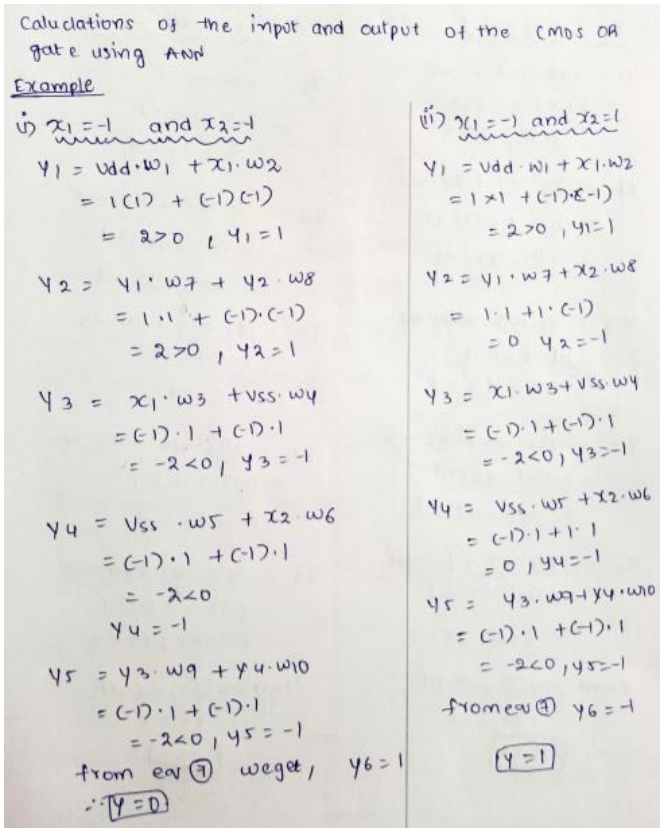

Fig.2.3 Examples

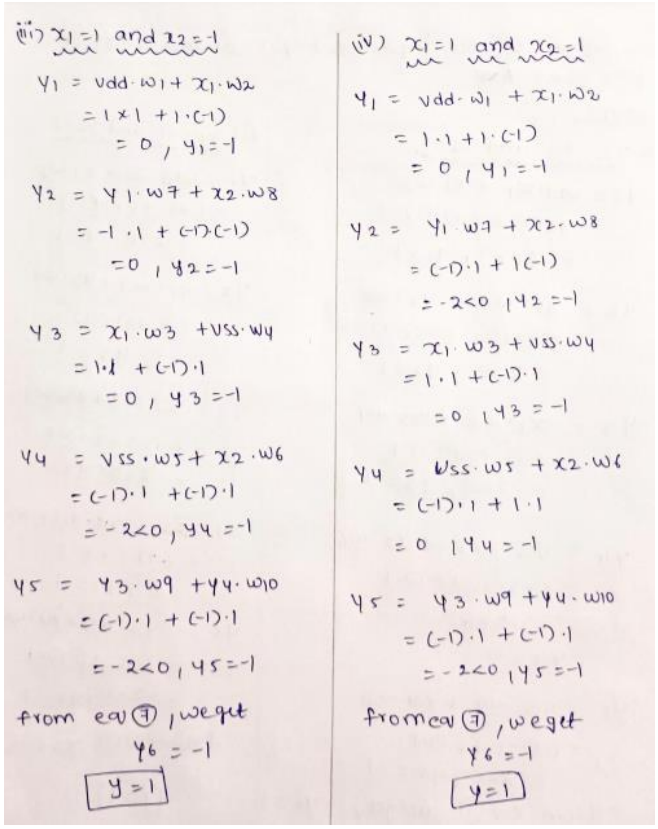

Fig.2.3.1 Examples

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IV. RESULTS

Various inputs to various artificial neurons utilized in the CMOS OR ANN, as well as the corresponding output 'A' and 'B' are the OR gate's inputs, while y is the binary output. However, the ANN works with bipolar inputs and outputs.

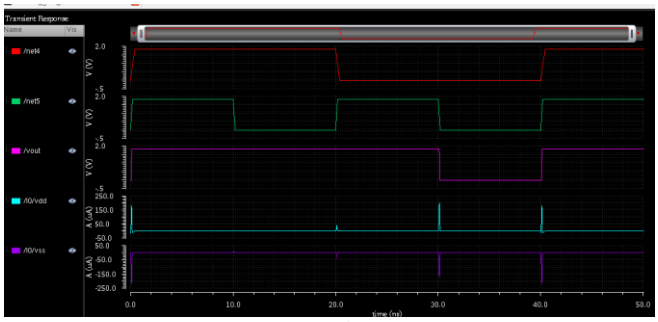

Fig.3.1 Transient response of CMOS OR gate

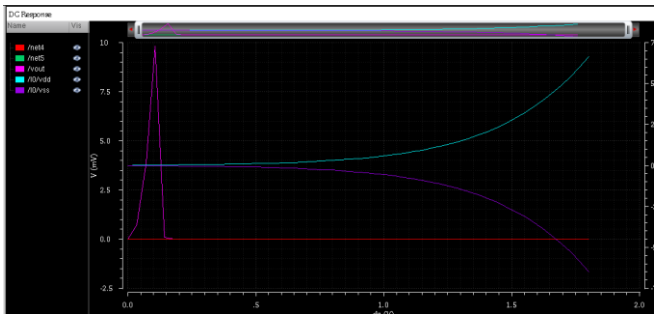

Fig.3.2 DC response of CMOS OR gate

A	B	x_1	x_2	v_{dd}	v_{ss}	y_1	y_2	y_3	y_4	y_5	y_6	y'	y
0	0	-1	-1	1	-1	1	-1	-1	-1	-1	1	-1	0
0	1	-1	1	1	-1	1	-1	-1	-1	-1	-1	1	1
1	0	1	-1	1	-1	-1	-1	-1	-1	-1	-1	1	1
1	1	1	1	1	-1	-1	-1	-1	-1	-1	-1	1	1

Fig.3.3 Input and Output of CMOS OR ANN

W_1	W_2	W_3	W_4	W_5	W_6	W_7	W_8	W_9	W_{10}	W_{11}	W_{12}
1	-1	1	1	1	1	1	-1	1	1	1	1

Fig.3.4 weights set used in the CMOS OR ANN

V. CONCLUSION

This study takes the method of designing simple circuits to construct fundamental logic gates using CMOS. CMOS circuits are presently employed in a wide range of products. ANNs are also getting increasingly popular these days. With the growth of this technology, this technique will lead to the construction of basic ANN circuits, as well as the hardware implementation of the ANN models.

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AUTHORS PROFILE

Jithendra Pulivarthi Department of Electronics and Communication Engineering SRM University Andhra Pradesh, India

Tammina Yasawini Department of Electronics and Communication Engineering SRM University Andhra Pradesh, India

Saipriya Nallamadugu Department of Electronics and Communication Engineering SRM University Andhra Pradesh, India