Design Tunable Adaptive Feedback Equalization Technique

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***Abstract*: Ultralow-power subthreshold logic circuits are becoming prominent in embedded applications with limited energy budgets. Minimum energy consumption of digital logic circuits can be obtained by operating in the sub threshold regime. A tunable adaptive feedback equalizer circuit that can be used with a sequential digital logic to mitigate the process variation effects and reduce the dominant leakage energy component in the sub threshold digital logic circuits. Sub threshold is the current between the source and drain of a MOSFET when the transistor is in sub threshold region, or weak-inversion region, that is, for gate-to source voltages below the threshold voltage. By using single feedback circuit, to reduce the power consumption &energy consumption.**

1.INTRODUCTION

The use of subthreshold digital CMOS logic circuits is becoming increasingly popular in energy-constrained applications where high performance is not required. The main idea here is that scaling down the supply voltage can significantly reduce the dynamic energy consumed by digital circuits. The supply voltage is scaled below the threshold voltage of the transistors, the propagation delay of the logic gates increases, which in turn increases the leakage energy of the transistors.We present a design technique for (near) subthreshold operation that achieves ultra low energy dissipation at throughputs of up to 100 MB/s suitable for digital consumer electronic applications. Our approach employs i) architecture-level parallelism to compensate throughput degradation, ii) a configurable VT balancer to mitigate the VT mismatch of nMOS and pMOS transistors operating in sub/near threshold, and iii) a fingered-structured parallel transistor that exploits VT mismatch to improve current drivability [1]. Body biasing [2] is often employed to mitigate global variations, for a microcontroller fully functional down to 160 mV (210 mV without body biasing). Achieving supply voltages of 85 mV for an FIR filter (160 mV without body biasing).[3] Flip-flop metastability is becoming an important consideration for designing reliable synchronous and asynchronous systems, especially in the sub-threshold region where it degrades exponentially with the reduction in supply voltage.[4] In this paper, detailed analysis is given on the design of metastable hardened flip-flops in the sub-threshold region[5]. Emerging biomedical and wireless applications would benefit from the availability of digital processors with substantially improved energy efficiency [6]. One approach to realize ultra-low energy processors is to scale the supply voltage aggressively to below the transistor threshold [7], yet the major increase in delay variability under process, voltage, and temperature (PVT) variations combined with the dominance of leakage power makes robust sub-threshold computations and further voltage scaling extremely challenging[8].

VLSI DESIGN AND PERFRMANCE

The proposed using an adaptive feedback equalizer circuit in the design of tunable sub threshold digital logic circuits. This adaptive feedback equalizer circuit can reduce energy consumption and improve performance of the sub threshold digital logic circuits. It enables post fabrication tuning of the digital logic block to overcome worse than expected process variations as well as lower energy and improve performance. SCL d(source couple logic) circuits have several advantages over traditional NCL (null combinational logic) circuits. Most of these advantages are the irect result of applying the sleep mechanism to the circuit. The first obvious advantage is reducing the static power consumption due to power-gating through high-Vth transistors. For a 64-bit adder example circuit, we show that compared with [2], the use of our proposed adaptive feedback equalizer circuit can reduce the energy-delay product (EDP) by 25.83% and also reduce the normalized variation ($3\sigma/\mu$) of the critical path delay from 16.1% to 11.4%. In addition, in case of worse than expected process variations, we show that the tuning capability of the equalizer circuit can be used post fabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy.

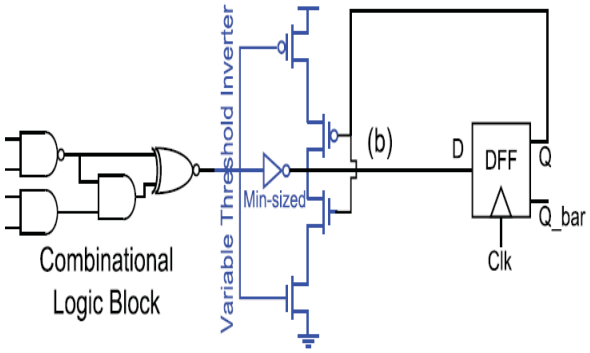
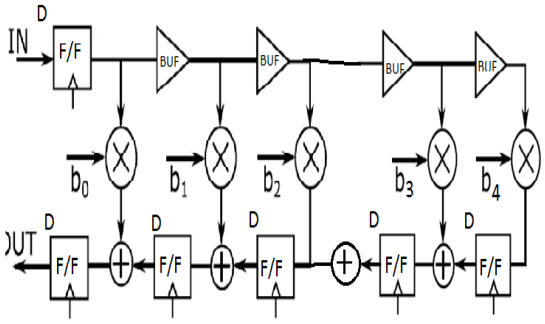


Figure (A)

The sampling of a glitch leads to the marginal increase in the dynamic energy of the sequential logic block (0.72% increase in the 64-bit adder), but it has a negligible impact

on the overall energy consumption as it is not the dominant energy component in the subthreshold regime. The feedback equalizer circuit also reduces the pulse width of the glitch (by 41%). This decreases the required guardband in the clock period to avoid sampling the glitch (and hence we can reduce the clock period), which ultimately reduces the dominant leakage energy component of the subthreshold logic block by 5.1% in the 64-bit adder at minimum-energy supply voltage. To avoid the metastability problem in the E-flipflop, both the setup time and hold time constraints should be satisfied. By using one feedback equalization cicuit to reduce the power and energy in the Digital Schematic Editor Tool and Microwind Tool



E-logic is 2.69% (on average) larger than the NE-logic. This is negligible compared with the 18.5% reduction in the leakage energy (on average) of the design. The feedback circuit drops the minimum energy supply voltage of the E-logic by 10 mV while maintaining the zero-error rate operation. If operated at the respective minimum energy supply voltage, the E-logic consumes 10.85% less total energy compared with the NE-logic and runs 8.04% faster. If both designs are operated at the minimum energy supply voltage of the NE-logic, the E-logic runs 19.1% faster and consumes close to 10% less energy.

$$y[n] = b_0 x[n] + b_1 x[n-1] + \cdots + b_N x[n-N] = \sum_{i=0}^{N} b_i \cdot x[n-i]$$

- x[n] is the input signal,
- y[n] is the output signal,
- N is the filter order; an Nth-order filter has (N+1) terms on the right-hand side
- bi is the value of the impulse response at the i'th instant for 0<=i<=N of an Nth-order FIR filter.
- If the filter is a direct form FIR filter then bi is also a coefficient of the filter
- This computation is also known as discrete convolution.

ONE FEEDBACK EQUALIZATION CIRCUIT:

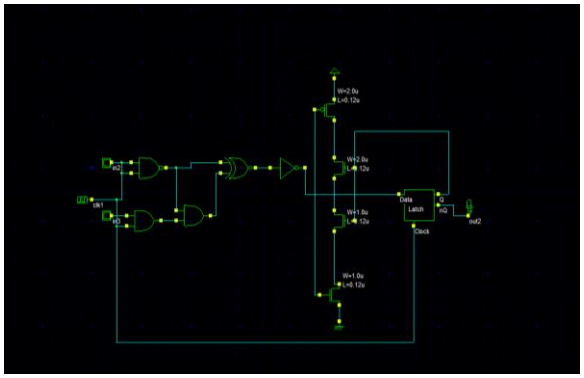


Fig1.1 (a)

OUTPUT OF ONE FEEDBACK IN DSCH:

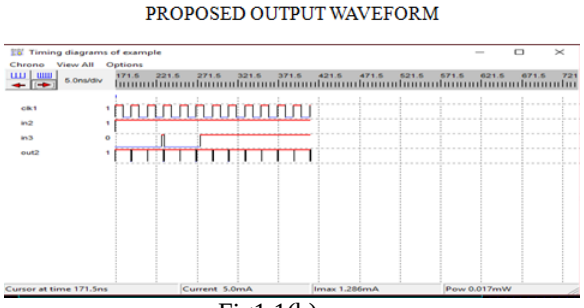


Fig1.1(b)

ONE FEEDBACK LAYOUT:

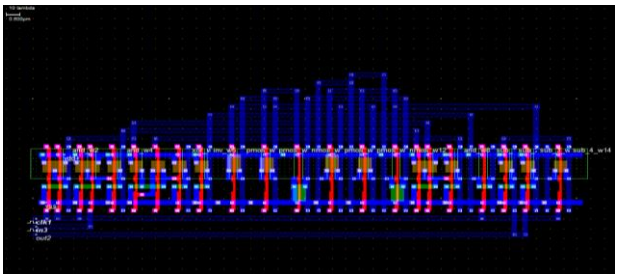


Fig1.2(a)

The figure1.1 are described about the one feedback equalization , inorder to reduce the power when compared to the two feedback equalization technique

ONE FEEDBACK OUTPUT IN MICROWIND:

Fig1.2(b)

The power and energy can be consumed & the power are calculate in the Microwind Tool

HALF ADDER CIRCUIT IN DSCH:

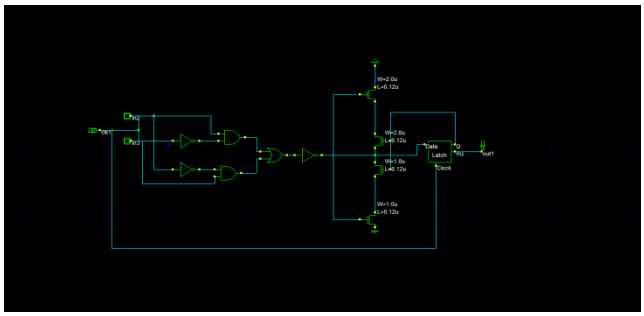


Fig2.1(a)

HALF ADDER DSCH OUTPUT:

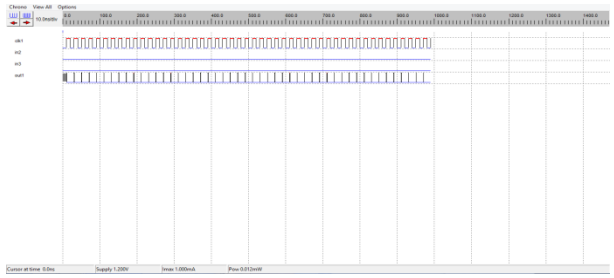


Fig2.1(b)

The figure 2.1 are represented the one feedback by using half adder circuit

HALF ADDER LAYOUT:

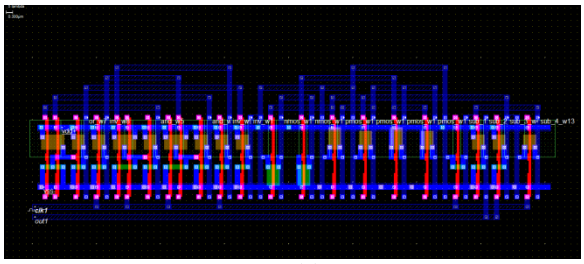


Fig2.2(a)

HALF ADDER OUTPUT IN MICROWIND TOOL:

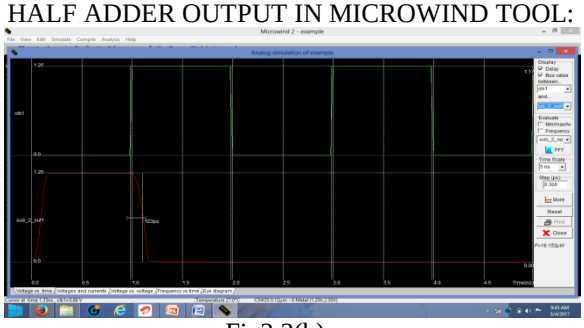


Fig2.2(b)

FULL ADDER CIRCUIT IN DSCH:

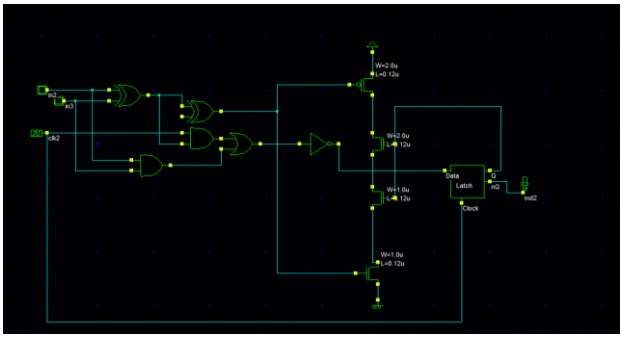


Fig3.1(a)

The figure 2.2 are described by the half adder circuit are implement with the one feedback equalization circuit. The power can be calculate in the Microwind tool

FULL ADDER OUTPUT IN DSCH:

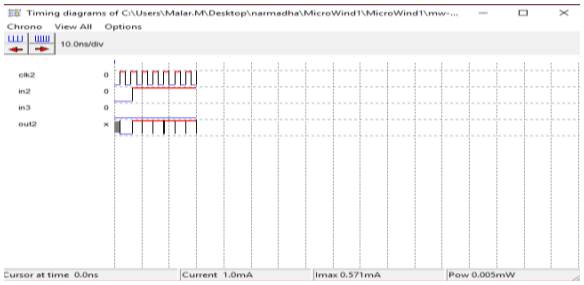


Fig3.1(b)

FULL ADDER LAYOUT:

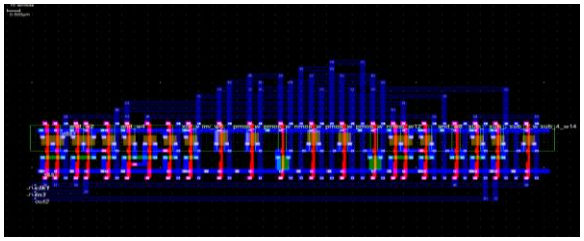


Fig3.2(a)

FULL ADDER OUTPUT IN MICROWIND TOOL:

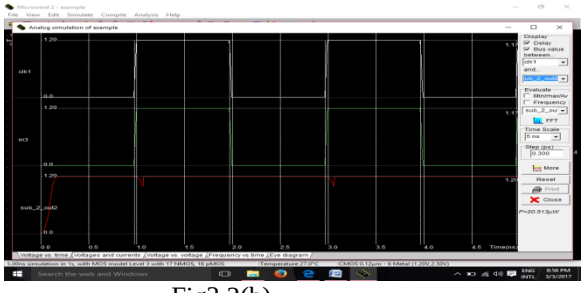


Fig3.2(b)

EXAMPLE OF PROPOSED CIRCUIT:

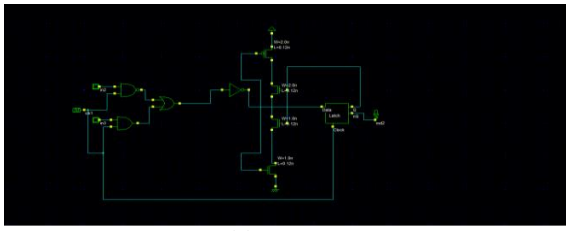


Fig4.1(a)

EXAMPLE OF PROPOSED SYSTEM OUTPUT IN DSCH:

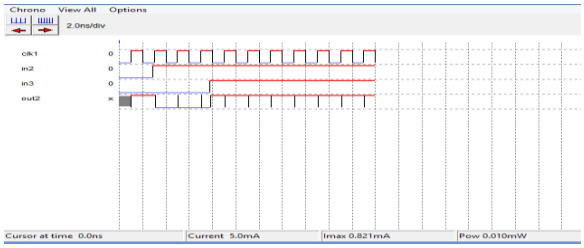


Fig4.1(b)

EXAMPLE OF PROPOSED SYSTEM LAYOUT:

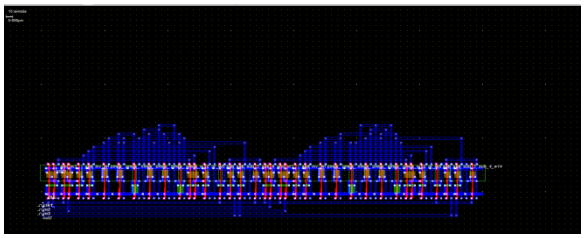


Fig4.2(a)

EXAMPLE OF PROPOSED SYSTEM OUPUT IN MICROWIND TOOL:

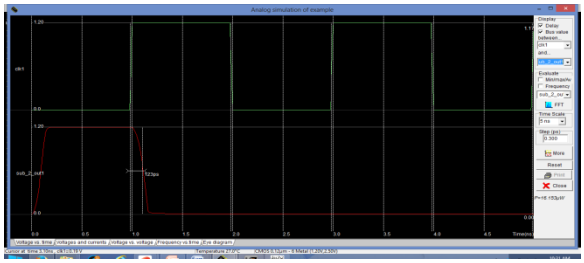


Fig4.2(b)

DSCH OUTPUT:

SYSTEM	POWER(mW)	Imax(mA)
Two Feedback Output	2.385	3.029
Example of One Feedback Output	0.017	1.286
Half Adder Proposed Output	0.012	1.00
Full Adder Proposed Output	0.005	0.571

Table1.1 COMPARISON BETWEEN TWO FEEDBACK & ONE FEEDBACK CIRCUIT IN DSCH

MICROWIND OUTPUT:

SYSTEM	POWER(microW)	Time(ns)
Two Feedback Output	20.513	19.93
Example of One Feedback Output	16.834	3.10
Half Adder Proposed Output	16.153	1.35
Full Adder Proposed Output	16.834	5.00

Table1.2 COMPARISON BETWEEN TWO FEEDBACK & ONE FEEDBACK CIRCUIT IN MICROWIND TOOL

DESIGN CIRCUI &LAYOUT ANALYSIS:

The circuits are designed using DIGITAL SCHEMATIC EDITOR TOOL. The DSCH program is a logic editor and simulator. DSCH is used to validate the architecture of the logic circuit before the microelectronics design is started. DSCH provides a user-friendly environment for hierarchical logic design, and fast simulation with delay analysis, which allows the design and validation of complex logic structures. DSCH also features the symbols, models and assembly support for 8051 and 16F84 controllers. Designers can create logic circuits for interfacing with these controllers and verify software programs using DSCH. The power can be calculated in MICROWIND TOOL.Microwind is truly integrated EDA software encompassing IC designs from concept to completion, enabling chip designers to design beyond their imagination. MICROWIND integrates traditionally separated front-end and back-end chip design into an integrated flow, accelerating the design cycle and reduced design complexities. The figure 3.1 can be representing the full adder circuit. It is used as a input of the circuit & the figure 3.2 are represented by the full adder circuit power are calculate in the Microwind tool. It tightly integrates mixed-signal implementation with digital implementation, circuit simulation, transistor-level extraction and verification providing an innovative education initiative to help individuals to develop the skills needed for design positions in virtually every domain of IC industry. The figure 4.1&4.2 are representing the example for the combinational circuit testing in DSCH and MICROWIND TOOL.

CONCLUSION:

We proposed the application of a tunable adaptive feedback equalizer circuit to reduce the normalized variation of total delay along the critical path and the dominant leakage energy of the digital CMOS logic operating in the subthreshold regime. Adjusting the switching thresholds of the gates before the flip-flop based on the gate output in the previous cycle, the adaptive feedback equalizer circuit enables a faster switching of the gate outputs and provides the opportunity to reduce the leakage energy of digital logic in weak inversion region. We implemented a nonequalized and an equalized design of a 64-bit adder in UMC 130-nm process using static complementary CMOS logic. Using the equalized design the normalized variation of the total critical path delay can be reduced from 16.1% (nonequalized) to 11.4% (equalized) while reducing the EDP by 25.83% at minimum energy supply voltage. Moreover, we showed that in case of worse than expected process variation, the tuning capability of the equalizer circuit can be used postfabrication to reduce the normalized variation ($3\sigma/\mu$) of the critical path delay with minimal increase in energy.

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