Design & Study of Low-Dropout Voltage Regulators for Low-Voltage VLSI Devices.

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***Abstract*— This brief presents a design and study of low-voltage Low-dropout Voltage regulators for low-voltage VLSI devices, which can achieve operation below 1V,fast transient response, high power supply rejection with a low quiescent current under a wide range of operating conditions. The proposed LDO regulator was designed and fabricated using 90nm CMOS technology. The area and the loss of power can be minimized. In addition, a maximum output variation for a load transient, and a maximum current efficiency was achieved. Using the bipolar transistor technology or a complex circuit to achieve a high PSR at the expense of a high quiescent current however, unnecessary for the post regulator of a general purpose switching regulator. The dynamic biasing technique is widely adopted by conducting a very small quiescent current under a light load condition. This inevitably sacrifices the transient response during a light to heavy load transition.**

Keywords*— Low-Dropout (LDO)regulator, Fast transient low voltage, small area, maximum current efficiency, maximum dynamic range, reduction in power loss

I. INTRODUCTION

Extremely low quiescent current power management circuits are highly desirable for battery powered applications,as any current drained from the battery would encroached into the remaining battery capacity.But unlike many low power applications like passive RFIDs, portable multimedia electronics such as tablets,laptops and phoes, require their power supply modules to source a much wider output current range to support the ever increasing functionality and processing power in the gadgets.

Low-dropout regulators(LDOs) are one of the most widely used power supply modules for noise sensitive analog. And LDO are key components of SOC application. A switching pre-regulator is usually followed by a low dropout(LDO)regulator to provide a regulated power source for noise sensitive blocks. It has a simple architecture and a fast-responding loop, which makes it the best candidate to implement these post regulators.

The design in [2],[3],[11] is focused on enhanching the transient response and drive a large current.The LDO regulators proposed in [11] achieved a high PSR over a wide frequency range.

II. ARCHITECTURE AND DESIGN OF PROPOSED LDO REGULATOR

A basic LDO regulator composed of an EA, a power MOS transistor(Mp),biasing circuit, and a feedback network as shown in fig.1.An off chip output capacitor used to check the output variation during the load transient.The challenges and the concept of designing a low-voltage LDO regulator are briefly discussed below.

A. Input voltage and low quiescent current

A high loop gain is mandatory in LDO regulator design to achieve optimum performance values as accurate output and PSR.A low supply voltage and output resistance reduction induced by a shrinking technology limit the achievable gain of the EA.

To achieve a low-voltage operation , an error amplifier with more than three stacked transistors between the supply voltage and ground is preferred. The EA requires a wide output swing to minimize the size of pass device and hence easy the requirement on voltage change(slew rate) of the EA.

B. Fast transient Response

The transient response is the voltage variation and recovery time during the load current transient.The voltage variation is more important than the recovery time,as even a small output voltage variation can cause severe performance degradation to the load circuit operation.To reduce the output voltage variation,both a large close loop bandwidth of the LDO regulator and a large output current slew rate of the EA is required.

Increasing the closed loop bandwidth may,however affect the pole/zero lacations and the circuitry may become too complex, consuming more quiescent current.The concept of the transconductance amplifier is shown.

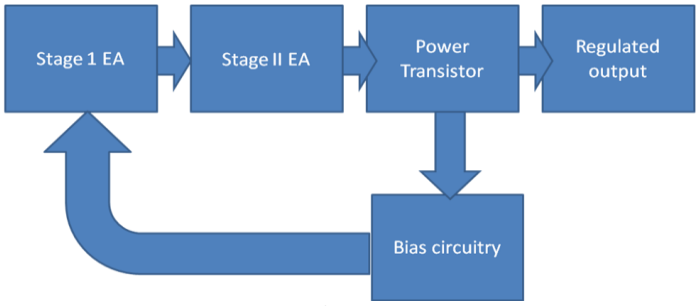

Fig.1 Block diagram of proposed LDO regulator

C. *power supply rejection*

To provide a clean and accurate output voltage with a low voltage level,noise suppression is needed.It is difficult to achieve a high loop gain with a low supply voltage.The concept of resource sharing power noise cancellation mechanism as shown in Fig.1 The first stage EA attenuates the power noise ,Second stage rejects the common mode noise at its inputs,and creates a replica of the supply noise at the output.

D. *Small area*

In a low voltage LDO regulator design several performance
enhancing auxiliary circuits and a large *Mp* occupy space considerably.To support a wide load current range and a wide output voltage range ,the *Mp* may enter the triode region. Similarly,the LDO regulator can respond to the load current transient in time for such a wide range of operating conditions.

E. *Stability*

The dominant pole for an off-chip capacitor compensated LDO regulator, exists at the output node. As a large *Mp* contributes the first nondominant pole(*Pg*) at a relative low frequency,a large equivalent series resistance of C_L is required to generate a low frequency zero to cancel p_g..A wide output swing EA can reduce the size of the *Mp* implying that pole zero cancellation is taking place at a higher frequency with a related small R_{esr}.

III. CIRCUIT REALIZATION AND SIMULATION RESULTS

To achieve the required goals of compact and low-voltage operation while achieving a fast transient response,low I_Q and high PSR ,are optimized. The circuit schematic is shown in Fig.2. We first apply the simple symmetric OTA as the EA.

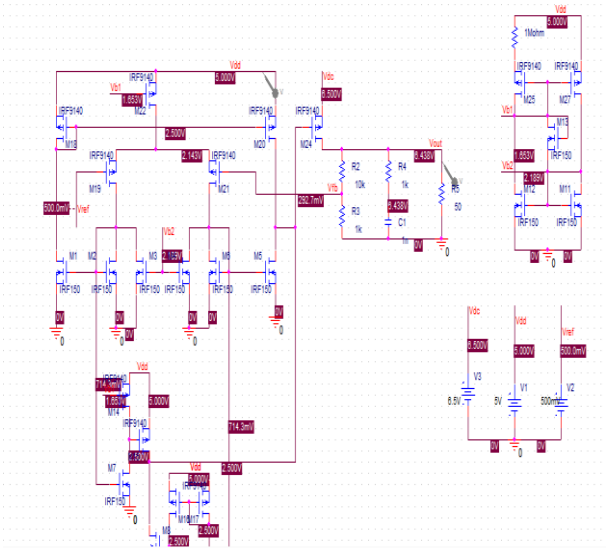

Fig. 2 Circuit schematic of the proposed LDO

The OTA type EA requires no compensation capacitor ,and operates at a minimum supply voltage equal to one threshold voltage plus twice the overdrive voltage.Thus,the EA can

$$A_{EAO} = g_{m2}\times A\times(r_{O7}\|r_{O9})$$

$$\approx g_{m2}\times A\times r_{O9}$$

$$= (2Id2\div Vov2)\times A\times(1\div \lambda_9\times A\times I_{d2})$$

$$= 2\div(V_{ov2}\times \lambda_9) \quad (1)$$

Where we assume $(r_{O7}\|r_{O9})$ and let $\{I_{d2},V_{ov2},A\}$ represent the bias current,overdrive voltage and the current ratio between the first and second stages of EA.The A_{EAO} in (1) is too low to achieve a fast transient response and high PSR.Therefore we apply a current splitting technique shown in Fig.3. to boost the gain by maintaining g_{m2} and increasing r_{O9}. Thus,the gain of the modified EA(A_{EAM}) is boosted by a factor of 1/B as follows:

$$A_{EAM} \approx g_{m2}\times A\times r_{O9}$$

$$=(2Id2\div Vov2)\times A\times(1\div \lambda_9\times A\times B\times I_{d2})$$

$$=A_{EAO}\div B$$

Where B is the current splitting ratio and is <1.
The gain boosted OTA-based EA improves the loop gain of the LDO regulator, which in turn enhances the PSR performance.The two equivalent resistors between the output nodes (Vx andVy) of the first stage of the EA and the ground

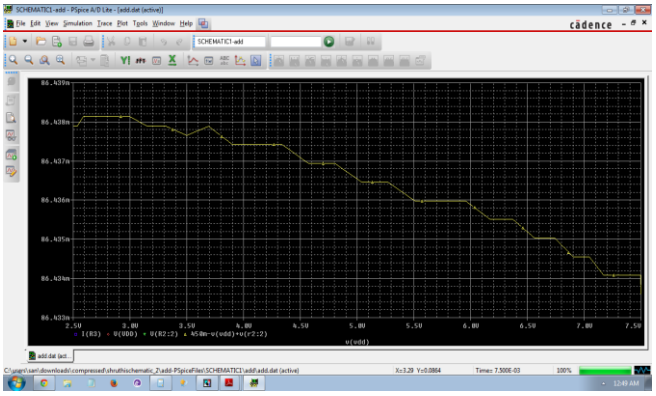

Fig.3. Measurement of dropout voltage with the change in input voltage

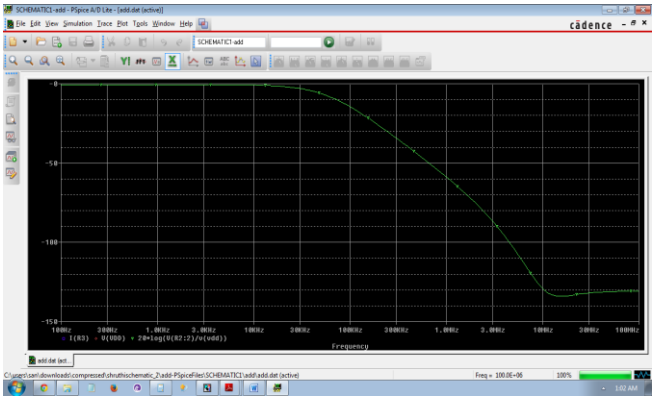

Fig.4. Simulated frequency response of the proposed LDO regulator

_ Measurement of dropout voltage with the change in input voltage Fig.3.We first assume that the power noise is propagated by stage 1_EATA through the common mode signal V_{icm} and causes fluctuation on V_{g6}. The output V_g induced by V_{icm} is,given by

$$V_g = (g_{m7}V_{g6} - g_{m9}V_{icm}).(ro7 \| r_{o9})$$

$$\approx (g_{m7}(g_{m8} \div g_{m6}) - g_{m7}V_{icm})(ro7 \| r_{o9})$$

$$= ((g_{m7} \div g_{m6})\, g_{m8} - g_{m9})V_{icm}(ro7 \| r_{o9})$$

$$\approx 0 \qquad (3)$$

Where we assume that M_{EA8} and M_{EA9} are matched devices.To cause g_{m6} to be close to g_{m7} , the channel length of M_{EA6} and M_{EA7} are selected to be five times the minimum length to reduce the effect of channel length modulation. then,we ground both the nodes V_x and V_y and input the power noise from the power supply. The small signal model shown at the top of Fig.3 is used to show how the power noise is replicated to V_g. The result is given as

$$V_g = V_{dd}\,(r_{o9} \div (\, r_{o7} + r_{o9})) + i_{dd}(ro7 \| r_{o9})$$

$$\approx V_{dd}\,(r_{o9} \div (\, r_{o7} + r_{o9})) + V_{dd}(ro7 r_{o9} \div ro7 + ro9)$$

$$= V_{dd}$$

As the frequency of the power noise increases, the small signal model shown in Fig.3 is no longer valid as the equivalent
impedance of the parasitic capacitance of *Mp* becomes finite and can no longer be ignored.

The proposed LDO regulator shown in Fig.2 has three poles(*Po*,*Px and Pg*) and one zero(*Zesr*), and the simulated frequency response of the loop gain for the different load currents , output voltage and series resistance are shown in Fig.4.The dominant pole is *Po* due to the large off-chip compensation capacitor C_L.The second dominant pole Pg s located at a relatively high frequency as the wide output swing of the EA reduces the size of the *Mp*.Thus, *Pg* can be easily cancelled by the zero with the series resistor.The third pole *Px*
Is far beyond the UGF because of the simple architectire of the OTA based EA,and therefore does not affect the stability.Fig.4. guarantees the stability of the proposed LDO regulator for a wide range of operating conditions.

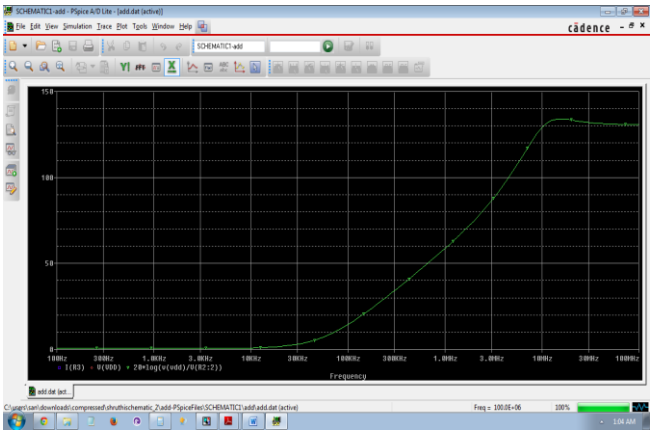

Fig.6. shows the measured PSR performance

IV. RESULTS

Fig.2. shows the schematic of the low dropout low voltage regulator. The above schematic is created in PSPICE. Fig.4. shows the simulation results of the low dropout regulator.

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