Design of VGA Display System Based on CPLD and Sram

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Abstract

VGA is Video Graphics Array and it is come in account in 1987. It displays approximate 256 simultaneous colours. Also it has 640 X 480=307,200 pixels maximum resolution. But with this resolution graphic card able to generate only 16 colours.

This design is used to eliminate the use of CPU to display the textual data .The design will be developed using programmable logic device- based logic analyzer. And also it is used to combine video display controller with SRAM memory controller. And this design used to create a Video frame buffer. The SRAM should be 256Kx16 CMOS static ram memories. And these memories are used to store images that will be displayed on the VGA screen

Now data from logic analyzer designed by other is combined to this design. Final goal is by using single chip CPLD and SRAM based logic analyzers which display the output measurement to monitor without interfaced to CPU. CPLD includes generation of VGA timing signal, finite state machine and logic control.

1. Introduction

The main intention of this design is to display an image into RAM, and onto a VGA monitor. This can be obtained by using an Xilinx XS95-108 board. This consists of the 32 KB SRAM and Xilinx XS9500 CPLD. This board is operated with 9 V power supply and it has 25 pins to download program. The VGA port is provided to connect to a VGA monitor. This port consists of 5 pins, Out of that, Two for TTL compatible signal, and three for colour (red, green and blue).

Generally to display the output on the monitor the logic analyzer uses C.P.U. But if we use such logic analyzer then there is problem of extra software that means it requires extra software for proper function. So by eliminating the use of CPU and to display the data on the monitor VGA display based on the CPLD and SRAM is necessary. With the help of such design data that gets from the controller in the SRAM is stores and then convert the data into analog signals to display on the VGA monitor. And all this operation is controlled by CPLD.

Before going to see system development of this design, we have to see its major component like, what CPLD is and which program downloading technique is used.

CPLD

CPLD (complex programmable logic device) is a device erasable programmable logic device that can be programmed with schematic and behavioural design CPLDs, which provides the features in between FPGA and PLAs. CPLD consist of number of circuits which contain series of gates and macro cells, each macro cell capable of implementing combinational and registered function. CPLD are ideal for complex box with large number of input. It require less board pace than FPGA, hence it has less board complexity than FPGA. In this design CPLD operates using its sampler module. This module is responsible to sampling appearance of the CPLD controller. CPLD also operate using Displayer module, this module takes care of the visuals of the oscilloscope.

VHDL

The 'V' stands for Very High Speed Integrated Circuit (VHSIC) and 'HDL' stands for Hardware Descriptive Language. VHDL is mainly dealing with the digital system. To verify the integrated system using single language VHDL is used. It is computer language used for formal description of the electronic device. VHDL is used to describe the circuit operation, its design, and tests to verify its circuit operation, also its basic concepts are analysis, elaboration, simulation, synthesis, test benches, interface, behaviour and structure. In our design behavioural modelling is used. Behavioural modelling is used to describe the algorithm performed by the design. Behavioural modelling contains process statement, sequential statment, signal assignment statement. Whole functioning of VHDL depends on the input and output port.

2. System Development

To implement VGA system without Central processing unit then we have to use CPLD and PC based logic analyzer instead of CPU. If we generate VGA signal by using CPU then system requires extra software.

The basic building blocks of the design are synchronous counter with 25 MHz clock frequency, pixel RAM and Character-Generator ROM, and VGA signal generator.

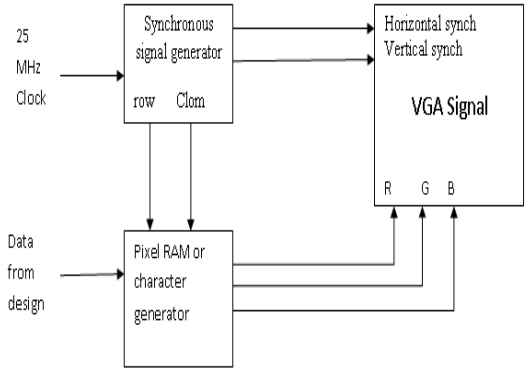

Figure (1): block diagram of VGA signal generator

To generate the VGA image with the help of CPLD and SRAM, we required VGA video signal. A VGA video signal consists of 5 analog signals. Out of that 5 signals two signals are TTL compatible signals, and remaining three signals are colour signals, with 0.7 to1.0 V peak to peak voltage levels. These 3 signals are used to control the colours of VGA generator. The colour signals are RED, GREEN, and BLUE. And two TTL compatible signals are horizontal synchronous signal and vertical synchronous signal. These TTL compatible signals are used for video signal synchronization purpose. Circuit using resistor and diode is used to convert TTL output from the CPLD to the RGB signals for the video signal generation.

Red, Green, Blue signals combine known as the RGB signals. To generate number of colours using RGB signal, analog levels of thses three signal are changes.
This design uses colour CRT tube, these tubes are similar to normal black and white CRT tube, except it has electron beam which are projected to Red, Green, Blue phosphor plate. At this plate there is three dot for each colour, all these dot are combined to form a pixel.
As we know the VGA signal has 640 by 480 pixel picture resolutions. To reduce flicker and to provide motion to the picture video signal must redraw the entire screen 60 times per second. That means the entire screen is refreshed 60 times per second. And this refreshing period is nothing but refresh period. Hence we can say VGA has 60 Hz standard refreshing rate.

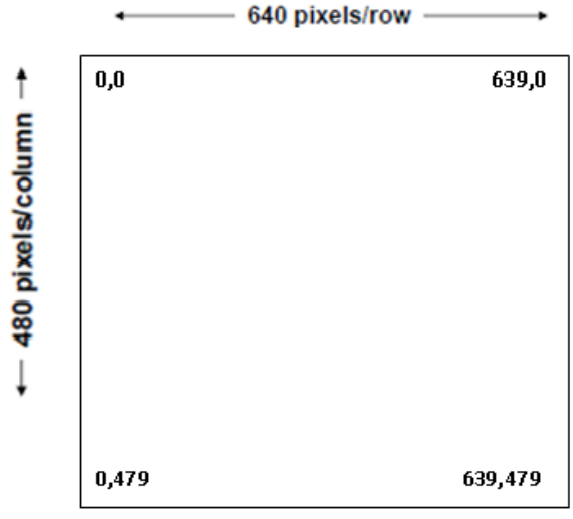

Figure 2: Redrawing process of VGA

Out of two TTL signal vertical sync signal used to tells monitor to start displaying a new image. And it is shown by monitor starts in the upper left corner with pixel 0, 0. And the horizontal sync signal used to tells the monitor to refresh another row of 640 pixels. Now after each 480 row of pixels are refreshed with horizontal scan, And the be horizontal scanning rate should be 480 pixel.

Conclusions

To display the output on monitor most of the logic analyzer uses C.P.U. But the problem with existing PC based logic analyzer is that it requires extra software to function properly. Hence by eliminating the use of CPU to display the data on the monitor VGA display based on the CPLD and SRAM is used. The VGA used in the embedded system. But due to unavibality of professional VGA display controller blank screen, splash screen problems are generated during the high resolution video image. Hence VGA generator based on CPLD and SRAM is used to overcome the above screen problems. Here CPLD is used to control the whole operation of the system. In this case the received data is stored in SRAM and then it could be read out in the form of analog signal. Hence we can conclude that VGA signal generation based stores data that gets from the on CPLD and SRAM can overcome the problem caused due to the insufficient bandwidth in displaying and also it reduces the pressure on CPU.

Advantages

It does not require extra software like CPU.

It uses to convert signal from the CPU by the video adapter and sent to a monitor with VGA input.

VGAs provide are More Secure Signal.

This design also provides improved videos quality. With this, we didn't receive blurry images or videos in really poor resolution.

Disadvantages

This system is slow as compared to VGA signal generation using CPU.

It requires extra maintenance.

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10. References

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