Design of Vedic Multiplier based on Logic Gates Employing Multiplexer using Logic Optimization Techniques

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***Abstract*— In low power digital electronics era, the multiplier is one of the fundamental elements in many of the applications like Digital Signal Processing (DSP) Systems and Processors. ALU is one of the major elements in many processors which require a computational unit that has to perform the computations in a fast manner adopting fast elements maintaining minimum area and power consumption Thus, the multiplier is one of the key elements in ALU which has a vital role in deciding the performance of the ALU especially in terms of speed, area and power which in accordance determines the cost of the processor. The design units in the developed multiplier here are based on the ancient Vedic mathematics and modified logic gates because Vedic multiplier using Urdhva Tiryagbhyam algorithm is found to be one of the fastest multipliers. To further improve the performance of the multiplier, these modified elements are incorporated in the design and performance analysis for the designed units using Vivado 2017.2 software on an I5, 8th generation processor.**

Keywords*— *Urdhva Tiryagbhyam algorithm, Vedic multiplier, Modified Logic Gates, Logic optimization techniques and VLSI multiplier

I. INTRODUCTION

The multipliers developed based on ancient mathematics consume large area and power and delay is more because the additions performed for the partial products in which carry plays the key role in deciding the speed factor. And also due to more computations while adding the generated partial products, area and power consumption also increased. Therefore, the design by incorporating logic optimization technique to reduce power and area played thekey role in low power VLSI system design. Thus, during the survey on multipliers, multiplier designs based on Vedic mathematics [1]-[4] are more speed efficient designs when compared to most ancient array multipliers [5]. Thus, to further improve the performance of a multiplier, the generated partial products areaddedin an efficientmanner by adoptingvarious adder designs. Different adder designs developed based on modifications in the logical structure of full adder and the performance analysis is explained in [6].

The basic modifications done here are modified AND gate, modified OR gate and modified XOR gate by using logic optimization technique. Section II describes the Vedic multiplier architecture, modified AND gate, modified OR gate and modified XOR gate.

II. VEDIC MULTIPLIER USING MODIFIED LOGIC GATES

In this section, the basic modules designed for OR gate, XOR gate and AND gate using 2:1 multiplexer andthe basic Vedic multiplier using Uradhva Tiryagbhyam algorithm is explained.

Logic gates such as AND, OR, and XOR gates are designed using multiplexers such that they can reduce the power, and number of LUTs.

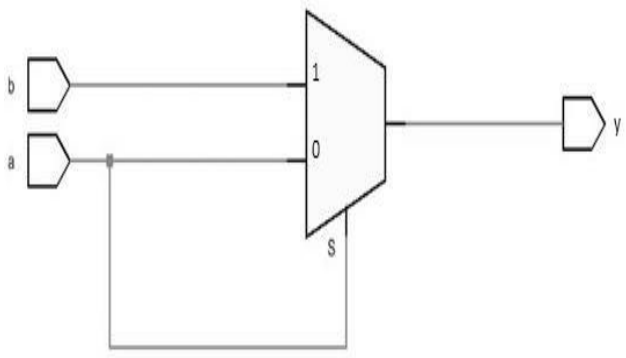


Fig-1: Modified AND gate

The Modified AND gate is designed by using a 2:1 multiplexer for which the inputs to the multiplexer are ‘a’ and ‘b’. Input ’a’ also acts as selection line for multiplexer and the obtained output is named as ‘y’ which is shown in Fig.1.

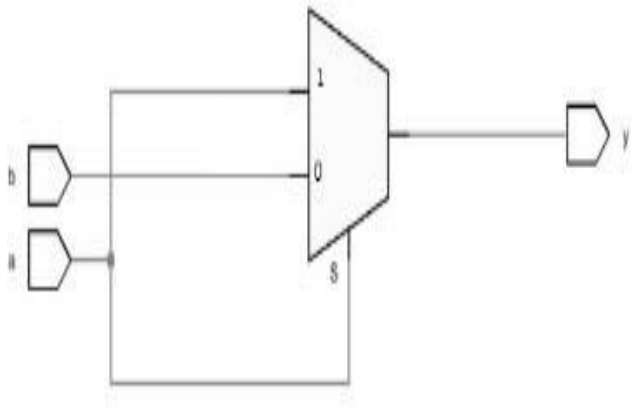


Fig-2: Modified OR gate

The Modified OR gate is designed by using a 2:1 multiplexer for which the inputs to the multiplexer are 'a' and 'b'. Input 'a' also acts as selection line for multiplexer and the obtained output is named as 'y' which is shown in Fig.2..

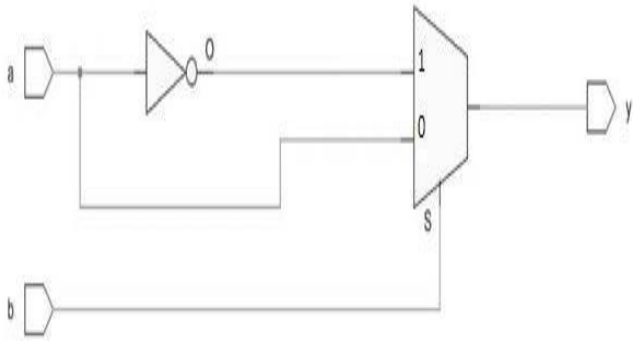


Fig-3: Modified XOR gate

The Modified XOR gate is designed by using a 2:1 multiplexer and a NOT gate for which the inputs to the multiplexer are 'a' and '~a'. Input 'b' acts as selection line for multiplexer and the obtained output is named as 'y' which is shown in Fig.3.

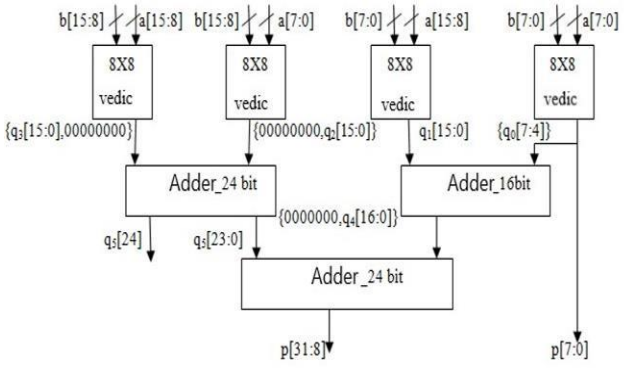


Fig-4 : Architecture of 16-bit vedic multiplier

The 16-bit Vedic multiplier architecture is designed based on Urdhva Tiryagbhyam principle in which addition is carried out using normal adders and partial products are generated using AND gates is shown in Fig.4. From this architecture, it is observed that the majority components are AND gates, OR gates and XOR gates. Initially. this design is carried out using conventional gates. Later, this architecture is modified using modified AND gate, modified OR gate and modified XOR gate. The combinations that are designed for vedic multiplier adopting Urdhva Tiryagbhyam Principle are:

1. Vedic Multiplier (VM)
2. Vedic Multiplier using Modified AND(VMMA)
3. Vedic Multiplier using Modified OR(VMMO)
4. Vedic Multiplier using Modified XOR(VMMX)
5. Vedic Multiplier using Modified AND and Modified OR(VMMAMO)
6. Vedic Multiplier using Modified AND and Modified XOR(VMMAMX)
7. Vedic Multiplier using Modified OR and Modified XOR(VMMOMX)
8. Vedic Multiplier using Modified AND and Modified OR and Modified XOR(VMMAMOMX)

III. SIMULATION RESULTS

Simulation and Synthesis is carried out using Vivado 2017.2 software on an I5 processor with 8GB RAM and 64-bit operating system. Initially 4-bit multiplier for all the above mentioned eight combinations are coded in Verilog HDL. Then, 8-bit multiplier for all the above mentioned eight combinations are coded in Verilog HDL. Finally,16-bit multiplier for all the above mentioned eight combinations are coded in Verilog HDL.

The inputs a[3;0], b[3:0] are given to a 4-bit VMMA and the obtained output c[7:0] alongwith theintermediate results such as q0,q1,q2,q3 is shown in Fig.5.

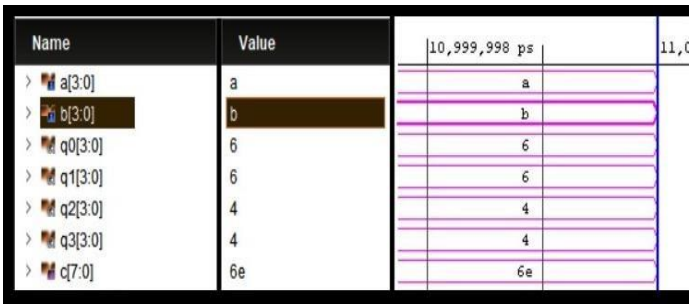


Fig-5: simulation results of 4-bit vedic multiplier

The inputs a[7;0], b[7:0] are given to a 8-bit VMMA and the obtained output c[15:0] along with the intermediate results such as q0,q1,q2,q3 is shown in Fig.6.

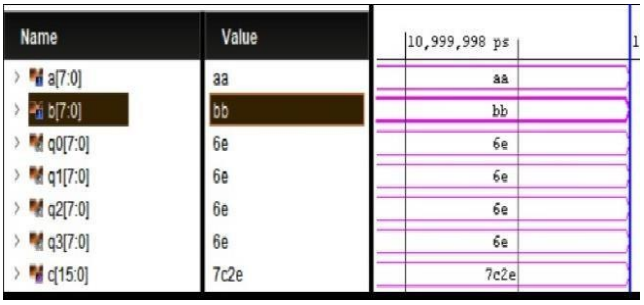


Fig-6: simulation results of 4-bit vedic multiplier

The inputs a[15:0], b[15:0] are given to a 16-bit VMMA and the obtained output c[31:0] along with the intermediate results such as q0,q1,q2,q3 is shown in Fig.7.

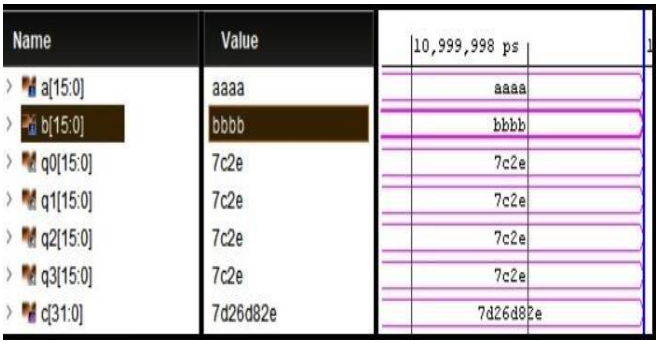


Fig-7: simulation results of 4-bit vedic multiplier

IV. COMPARISION RESULTS

In this section performance analysis for all the eight combinations using Vivado 2017.2 software is reported by considering the performance metrics such as LUTs, power and delay.

The performance parameters for VM for the data width ranging from 4-bit to 16-bit is reported in Table-1.

Table-1: Parameters reported for VM

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.757	2.417	3.886
8 X 8	86	11.082	2.563	13.443
16 X 16	410	17.38	2.685	38.289

The performance parameters for VMMA for the data width ranging from 4-bit to 16-bit is reported in Table-2.

Table-2: Parameters reported for VMMA

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.521	2.385	3.886
8 X 8	90	11.945	2.487	13.269
16 X 16	407	17.886	2.657	37.922

The performance parameters for VMMO for the data width ranging from 4-bit to 16-bit is reported in Table-3.

Table-3: Parameters reported for VMMO

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.652	2.352	3.894
8 X 8	90	11.349	2.545	13.321
16 X 16	410	17.086	2.705	38.344

The performance parameters for VMMX for the data width ranging from 4-bit to 16-bit is reported in Table-4.

Table-4: Parameters reported for VMMX

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.547	2.357	3.891
8 X 8	87	10.779	2.502	13.344
16 X 16	412	17.597	2.573	38.411

.The performance parameters for VMMAMO for the data width ranging from 4-bit to 16-bit is reported in Table-5.

Table-5: Parameters reported for VMMAMO

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.645	2.406	3.885
8 X 8	90	11.349	2.545	13.321
16 X 16	410	17.086	2.705	38.344

The performance parameters for VMMAMX for the data width ranging from 4-bit to 16-bit is reported in Table-6.

Table-6: Parameters reported for VMMAMX

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.5	2.354	3.891
8 X 8	90	11.426	2.598	13.445
16 X 16	410	17.731	2.83	38.254

The performance parameters for VMMOMX for the data width ranging from 4-bit to 16-bit is reported in Table-7.

Table-7: Parameters reported for VMMOMX

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.524	2.414	3.89
8 X 8	90	10.822	2.575	13.427
16 X 16	411	17.688	2.244	38.377

The performance parameters for VMMAMOMX for the data width ranging from 4-bit to 16-bit is reported in Table-8.

Table-8: Parameters reported for VMAMOMX

Data Width	LUTs	DELAY (SETUP)	DELAY (HOLD)	POWER
4 X 4	16	7.524	2.414	3.89
8 X 8	90	10.822	2.545	13.427
16 X 16	411	17.688	2.673	38.377

The comparisons for the 4-bit multipliers for different combinations such as VM, VMMA, VMMO, VMMX, VMMAMO, VMMAMX, VMMOMX and VMMAMOMX are shown in Fig 8.

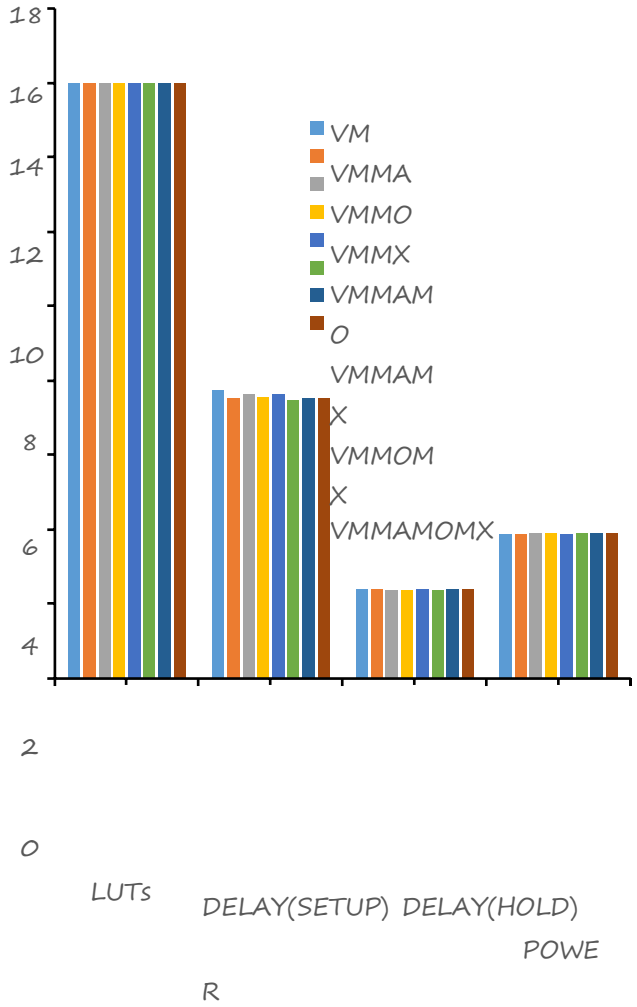
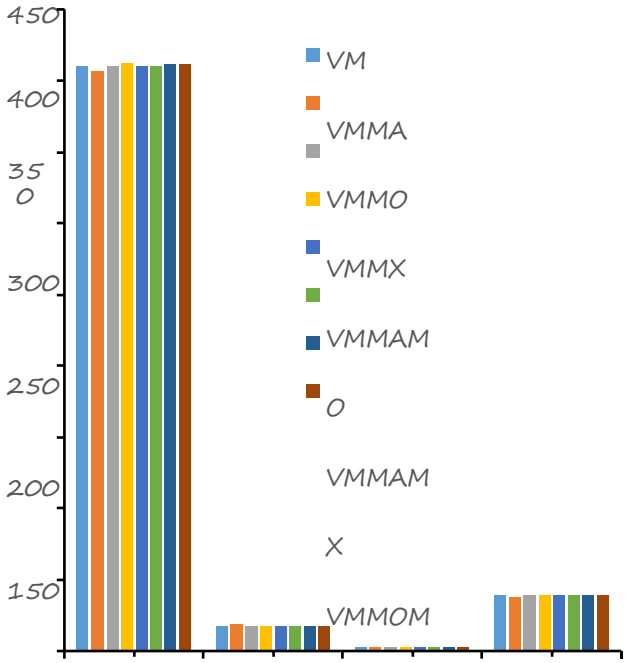
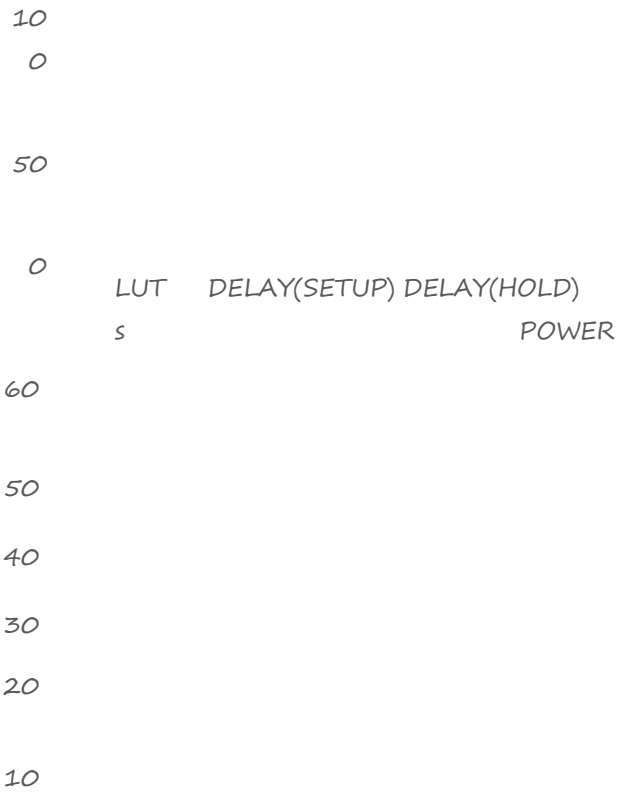


Fig-8: Comparison of performance parameters for 4-bit multiplier architectures

The comparisons for the 8-bit multipliers for different combinations such as VM, VMMA, VMMO, VMMX, VMMAMO, VMMAMX, VMMOMX and VMMAMOMX are shown in Fig 9.

The comparisons for the 16-bit multipliers for different combinations such as VM, VMMA, VMMO, VMMX, VMMAMO, VMMAMX, VMMOMX and VMMAMOMX are shown in Fig 10.





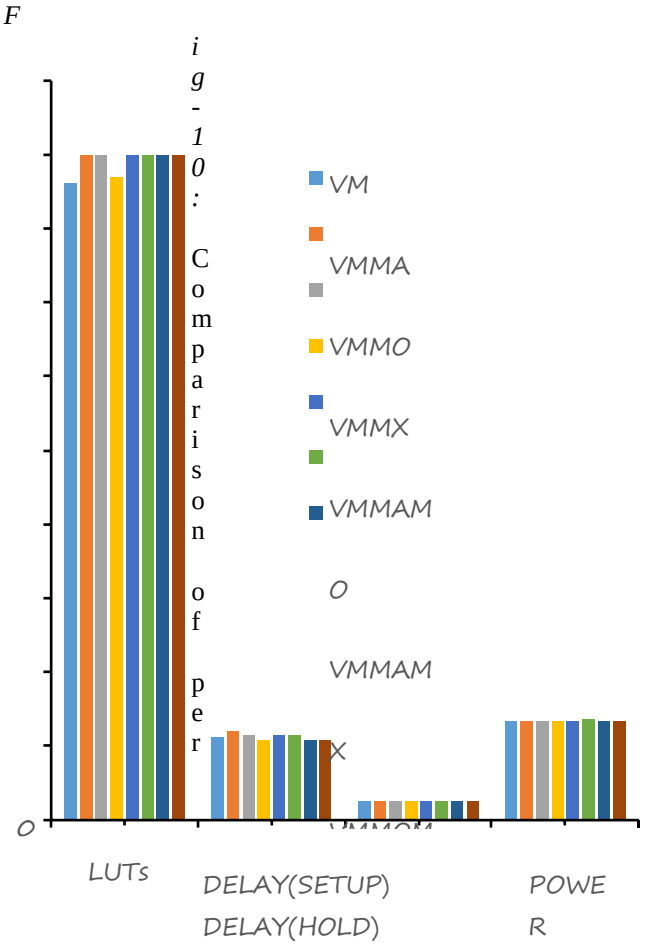


Fig-9: Comparison of performance parameters for 8-bit multiplier architectures

formance parameters for 16-bit multiplier architectures

From Fig 8, Fig 9 and Fig 10 it is observed that VMMA for the data width rangingfrom 4-bit to 16-bit consumes less area and power when compared to the rest of the architectures.

V. CONCLUSION

In this brief, performance analysis for Vedic multiplier adopting Urdhva Tiryagbhyam principle is done for total eight combinations i.e., for conventional vedic multiplier and for the modified logic gates using multiplexers. AND gate, OR gate and XOR gate are modified using multiplexers and developed total seven combinations by using these modified gates. In the present low power digital era, the multiplier design in many applications impacts the cost of the chip as the area in turn increases the cost. From this result analysis, it has been concluded that VMMA design is carried out by using modified AND gate which reduces area and power. Thus, VMMA design is suited for low power applications as the area and power consumption is reduced by adopting Modified AND gate which leads to reduction in cost of the chip.

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