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Design Of Two Stage CMOS Op-Amp With Low Power And High Slew Rate.

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I. ABSTRACT

In this paper a CMOS operational amplifier is presented which operates at 1.5V power supply and 20uA input bias current at 1 um technology using non conventional mode of operation of MOS transistors and whose input is depended on bias current. The unique behavior of the MOS transistors in sub-threshold region not only allows a designer to work at low input bias current but also at low voltage. While operating the device at weak inversion results low power dissipation but dynamic range is degraded. Optimum balance between power dissipation and dynamic range results when the MOS transistors are operated at moderate inversion. In comparison with the reported low power low voltage op-amps at 1 um technology, this op-amp has very low standby power consumption with a high driving capability and operates at low voltage. The proposed two stage op amp produces gain bandwidth (GBW) of 10MHZ operated at 1.5v power supply.

II. INTRODUCTION

CMOS op-amps are ubiquitous integral parts in various analog and mixed-signal circuits and systems. The two-stage op-amp shown in fig.1 is widely used because of its structure and robustness. In designing an op-amp, numerous electrical characteristics, e.g. gain bandwidth, slew rate, common mode range, output swing, offset, all have to be taken into consideration. Furthermore, since op-amps are designed to be operated with negative-feedback connection, frequency compensation is necessary for closed-loop stability. Power dissipation can be reduced by reducing either supply voltage or total current in the circuit or by reducing the both. As the input current is lowered though power dissipation is reduced, dynamic range is degraded. As the supply voltage decreases, it also becomes increasingly difficult to keep transistors in saturation with the voltage headroom available. Another concern that draws from supply voltage scaling is the threshold voltage of the transistor. A decrease in supply voltage without a similar decrease in threshold voltage leads to biasing issues. In order to achieve the required degree of stability, generally indicated by phase margin, other performance parameters are usually compromised. As a result, designing an op-amp that meets all specifications needs a good compensation strategy and design methodology.

The reported low power low voltage amplifiers using classical schemes have good small signal characteristics but their slew rate is small. By using the same technique slew rate is improved, as well as lower power dissipation is achieved. Also as the transistors are operated at weak and moderate inversion of MOS transistor, the op-amp operates at low power as well as low voltage

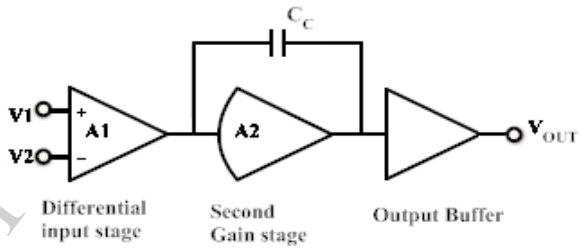


Fig.1 A Two stage op amp (block diagram)

The design of two stage op-amp was done with given specification;

- slew rate = 10 v/µs
- V_{out}(max) = 1.25v
- V_{out}(min) = 0.75v
- V_{ic}(min) = 1.0v
- V_{ic}(max) = 2.0v
- GB = 10.0 MHZ
- Phase margin = 60° when, the output pole= 2GB and, the rhp zero = 10GB.
- Mirror pole is kept at >= 10GB,
- Oxide capacitance cox = 0.5f/µm^2.

Model parameters;

- K'_N = 24.0 µA/V^2
- K'_P = 8.0 µA/V^2
- V_{TN} = $-V_{TP}$ = 0.75 V
- λ_N = 0.01/V,
- λ_P = 0.02

III. ANALYSIS

1 CIRCUIT DIAGRAM

The circuit diagram of two stage op-amp is given below. It consists of twelve transistors.

The circuit comprises of active load, differential amplifier, and current mirror for biasing, output buffer stage. The current source provides the necessary biasing needed. M5 and M8 are used to reduce the fluctuations in current to give constant current for driving. M3 and M4 (current mirror) provides necessary current to output stage or to bias the output stage.

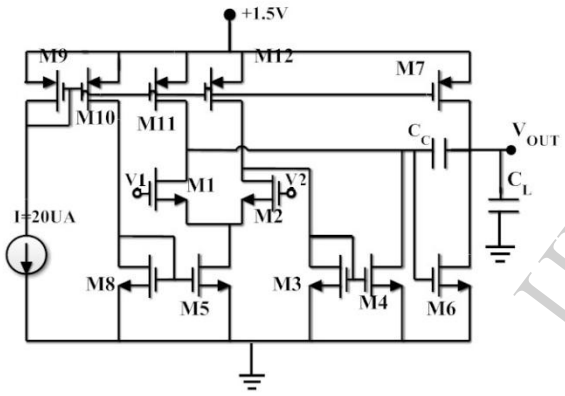


Fig.2 transistor level diagram

M6 and M7 increase the gain of the circuit.
All transistors work in saturation mode as the dynamic range is large in this mode. Aspect ratio of each transistor is calculated which helps in simulation to great extent.
to add flexibility.

2. CALCULATIONS

Vdd = 1.5V

Slew rate = sr = 10V/µs

Load capacitance = Cl = 10 pf

Capacitance in output stage = Cc = Cl/5

$I = Cc * sr$ (1)

Conductance = $gm1 = 2\pi.GB.Cc$ (2)

$(W/L)1 = (W/L)2 = gm1^2/2.K_N.(I/2)$ (3)

$Vd5 = Vic(min) - (\sqrt{(I/K_N*W1)} + Vtn)$ (4)

$(W/L)5 = (W/L)8 = 2I/(K_N*Vd5^2)$ (5)

$Vd11 = Vdd + Vtn - Vic(max)$ (6)

$(W/L)11 = (W/L)12 = 2 *1.5I/(Kp* Vd11^2)$ (7)

$(W/L)6 = 2 *10I/(K_N*(1.2323 -Vtn)^2)$ (8)

$(W/L)3 = (W/L)4 = 2I/(K_N*(1.25-Vtn)^2)$ (9)

Vd7 = 0.25v

$(W/L)7 = 2*10I/(Kp*Vd7^2)$ (10)

(W/L)9 = (W/L)10 = (W/L)7/10 (11)

Power dissipated = P_{diss} = 15I*1.5 W (12)

= 15*20*1.5= 450mW

Length of each transistor is taken as constant which is equal to 1micrometer.

3. T SPICE CODE

I. DC ANALYSIS OF TWO STAGE OP AMP

```
vd 101 0 dc 0.05v
e+ 2 100 101 0 +0.025
e- 4 100 101 0 -0.025
rd 101 0 1
vci 100 0 dc 2v
M1 3 2 1 0 NMOS1 W=33U L=1U
M2 5 4 1 8 NMOS1 W=33U L=1U
M3 5 5 8 8 NMOS1 W=7U L=1U
M4 3 5 8 8 NMOS1 W=7U L=1U
M5 1 9 8 8 NMOS1 W=202U L=1U
M6 10 3 8 8 NMOS1 W=71.65U L=1U
M7 10 6 7 7 PMOS1 W=800U L=1U
M8 9 9 8 8 NMOS1 W=202U L=1U
M9 6 6 7 7 PMOS1 W=80U L=1U
M10 9 6 7 7 PMOS1 W=80U L=1U
```

M11 3 6 7 7 PMOS1 W=120U L=1U

M12 5 6 7 7 PMOS1 W=120U L=1U

IBIAS 6 8 20UA

vdd 7 0 dc 1.5v

v8 8 0

CC 3 10 2pf

.MODEL NMOS1 NMOS VTO=0.75 KP=24U LAMBDA=0.01

.MODEL PMOS1 PMOS VTO=-0.75 KP=8U LAMBDA=0.02

cl 10 0 10pf

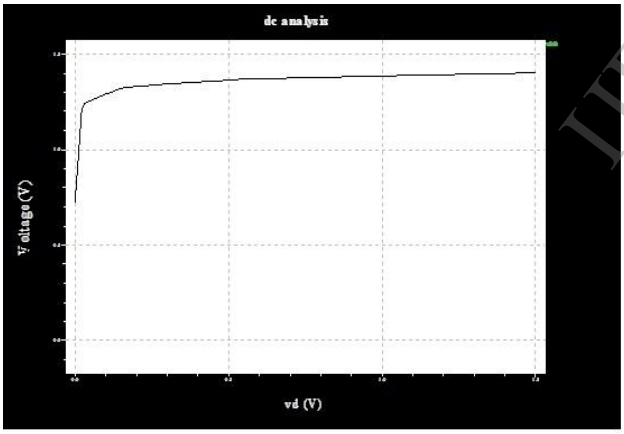
.dc vd 0v 1.5v 0.01v

.print dc v(10)

.OP

.END

Waveform



II. AC ANALYSIS OF TWO STAGE OP AMP

vdd 7 0 DC 1.5V

vss 8 0

vd 101 0 DC 0V AC 1V

e+ 2 100 101 0 +0.5

e- 4 100 101 0 -0.5

rd 101 0 1

VIC 100 0 DC 2v

M1 3 2 1 8 NMOS1 W=33U L=1U

M2 5 4 1 8 NMOS1 W=33U L=1U

M3 5 5 8 8 NMOS1 W=7U L=1U

M4 3 5 8 8 NMOS1 W=7U L=1U

M5 1 9 8 8 NMOS1 W=202U L=1U

M6 10 3 8 8 NMOS1 W=71.65U L=1U

M7 10 6 7 7 PMOS1 W=800U L=1U

M8 9 9 8 8 NMOS1 W=202U L=1U

M9 6 6 7 7 PMOS1 W=80U L=1U

M10 9 6 7 7 PMOS1 W=80U L=1U

M11 3 6 7 7 PMOS1 W=120U L=1U

M12 5 6 7 7 PMOS1 W=120U L=1U

CL 10 0 10pf

.MODEL NMOS1 NMOS VTO=0.75 KP=24U LAMBDA=0.01

.MODEL PMOS1 PMOS VTO=-0.75 KP=8U LAMBDA=0.02

.ac dec 20 100 30meg

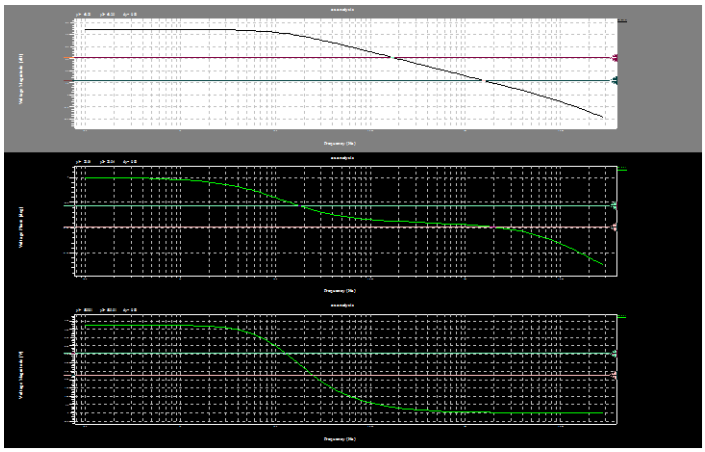
.tf v(10,0) vd

.print ac vm(10), vp(10), vdb(10)

.OP

.END

Waveform



III. TRANSIENT ANALYSIS OF TWO STAGE OP AMP

M1 3 2 1 8 NMOS1 W=33U L=1U

M2 5 4 1 8 NMOS1 W=33U L=1U

M3 5 5 8 8 NMOS1 W=7U L=1U

M4 3 5 8 8 NMOS1 W=7U L=1U

M5 1 9 8 8 NMOS1 W=202U L=1U

M6 10 3 8 8 NMOS1 W=71.65U L=1U

M7 10 6 7 7 PMOS1 W=800U L=1U

M8 9 9 8 8 NMOS1 W=202U L=1U

M9 6 6 7 7 PMOS1 W=80U L=1U

M10 9 6 7 7 PMOS1 W=80U L=1U

M11 3 6 7 7 PMOS1 W=120U L=1U

M12 5 6 7 7 PMOS1 W=120U L=1U

IBIAS 6 8 20UA

VDD 7 0 dc 1.5v

V8 8 0 dc 0v

CC 3 10 2pf

.MODEL NMOS1 NMOS VTO=0.75 KP=24U LAMBDA=0.01

.MODEL PMOS1 PMOS VTO=-0.75 KP=8U LAMBDA=0.02

cl 10 0 10P

VIN 2 0 PULSE(0V 1.5V 5US 1NS 1NS 20US 30US)

V_{SHORT} 4 10 DC 0V

.trans 1ns 30us

.print tran v(2) v(10)

.PROBE

.END

Waveform

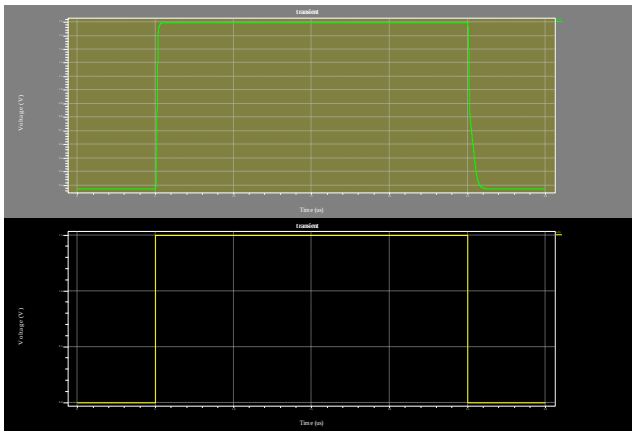


TABLE 1

OP-AMP DESIGN

Step 1	Cc = Cl/5 where Cl = 10pf
Step 2	I = slew rate * Cc
Step 3	$(W/L)_{1,2} = (2\pi.GB.Cc)/(2.Kn.(I/2))$
Step 4	$(W/L)_{5,8} = 2I/(Kn(Vic(min) - (\sqrt{(I/Kn.(W/L)1) + Vtn})$
Step 5	$(W/L)_{11,12} = 2*1.5I/(Kp(Vdd+Vtn-Vic(max))^2)$
Step 6	$(W/L)_6 = 2*10I/(Kn(1.2323 – Vtn)^2)$
Step 7	$(W/L)_{3,4} = 2I/(Kn(1.25-Vtn)^2)$
Step 8	$(W/L)_7 = 2*10I/Kp(0.25)^2$
Step 9	$(W/L)_{9,10} = (W/L)_7$

IV. LAYOUT

The layout of my circuit shown in figure below is done using professional software TANNER. The layout is both DRC and LVS clean. Parasitic extraction and Post Simulation is performed successfully.

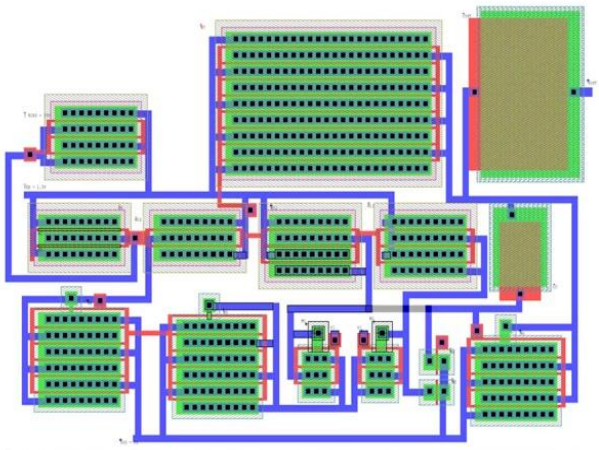


TABLE 2

DESIGN PARAMETERS OF OPAMP

Name	Unit (µm/µm)
$(W/L)_{1,2}$	32.865
$(W/L)_{3,4}$	6.667
$(W/L)_{5,8}$	202.310
$(W/L)_{6}$	71.649
$(W/L)_{7}$	800.000
$(W/L)_{9,10}$	80.000
$(W/L)_{11,12}$	120.000
Cc	12pf

Output Specification:

Slew rate	10 Volts/ µs
Output Voltage(max)	1.25 Volt
Output Voltage(min)	0.75 Volt
Phase Margin	60°
Power dissipated	450 mW
Gain (Av)	

V. CONCLUSION

The amplifier presented in this paper operates in saturation mode and regulates its bias current. When a signal is applied the current in the amplifier increases so that these amplifiers have very high driving current. The op-amp has low power as well as low voltage. Its slew rate is higher than reported low power low voltage amplifiers at 0.5 um technology.

VI. REFERENCES

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