Design of Time Efficient 8-Bit Ring Counter using Pulsed Latches

Vanishri Yandigeri
Dept. of Electronics and Communication
Shri Dharmasthala Manjunatheshwara College of Engineering and Technology
Dharwad, India

Prof. Jayashree Nidagundi
Dept. of Electronics and Communication
Shri Dharmasthala Manjunatheshwara College of Engineering and Technology
Dharwad, India

***Abstract*—This paper proposes 8-bit ring counter using pulsed latches. In recent years time efficient circuits are given utmost importance. Ring counters are the digital circuits that can be used in many applications like frequency divider circuits, counting the data etc. The proposed architecture reduces time consumption by using pulsed latches and clock pulse generator circuit. Pulsed latches can be used as an alternative to flip-flops. Pulsed latches use delayed pulses instead generated from clock to operate, thus consuming less time to operate compared to flip-flops. Pulsed latches are given more importance in sequential circuits as they are easy to design and can be designed and used in many applications.**

Keywords—Pulsed latches, flip-flops, delayed clock pulse generator, ring counter

I. INTRODUCTION

Ring counter is a type of counter, which normally uses D flip-flops to shift the data in circular fashion. The output of one flip-flop is connected as an input to the next flip-flop. The output of last flip-flop is connected as an input to the first flip-flop thus making data shift in ring structure or circular structure. 4-bit ring counter uses 4 D flip-flops, 8-bit ring counter uses 8 D flip-flops and so on. They are usually used in ASIC and FPGA hardware design. Conventionally N-bit Ring counter consisted of N D flip-flops. To implement time efficient Ring counter, pulsed latches can be used instead of flip-flops. As the pulsed latches in the circuit share the pulse generation circuit which uses single clock pulse as an input, time consumption can be reduced significantly [2].

Using pulsed latches also have many advantages including reduction in dynamic power consumption i.e. dynamic power consumption can be reduced upto 20 percent which is mainly due to reduction of power in clock networks [4]

Flip-flops impose overhead in terms of area of circuit, delay and clock load, thus without altering anything in terms of functionality, latches can be feasible solution [5] Using pulsed latches reduce clocking power, clocking power can be reduced by 24 percent and also wire length can be increased by little amount [6]

Conventional 8-bit Ring counter designed using D flip-flops as shown in the fig.1 below

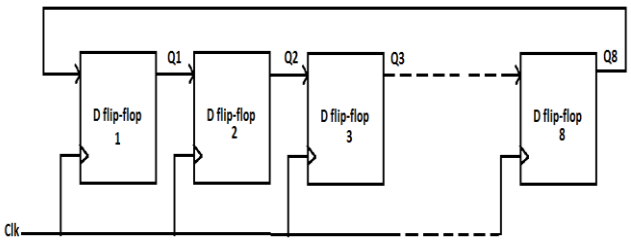

Fig. 1 8-bit Ring counter using D flip-flops

In the above fig.1 Q1 is the output of first flip-flop (D flip-flop 1) that is given as an input to D flip-flop 2 and so on. The output of last flip-flop(D flip-flop 8) Q8 is given as an input to first flip flop (D flip-flop 1).

The below table I, shows the truth table of 8-bit ring counter.

Table I
Truth table of 8-bit Ring Counter

Clk	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8
0	1	0	0	0	0	0	0	0
1	0	1	0	0	0	0	0	0
2	0	0	1	0	0	0	0	0
3	0	0	0	1	0	0	0	0
4	0	0	0	0	1	0	0	0
5	0	0	0	0	0	1	0	0
6	0	0	0	0	0	0	1	0
7	0	0	0	0	0	0	0	1
8	1	0	0	0	0	0	0	0

From the above truth table we can see that the sequence is repeated after 8 clock cycles for 8-bit ring counter. Similarly for 4-bit ring counter, sequence is repeated after 4 clock cycles and so on.

Pulsed Latches:

Conventionally two latches i.e. master slave flip-flops were used, so that circuit functions properly as shown in fig.2(a). The same circuit can be designed using pulsed latch as shown in fig.2(b). The clock pulses to pulsed latches is given from the clock signal generator circuit.

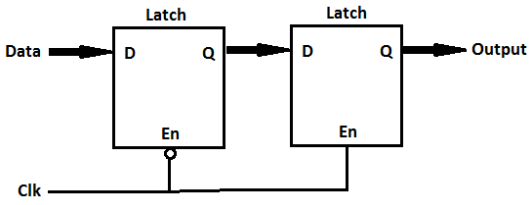

Fig. 2(a) Master slave flip-flop

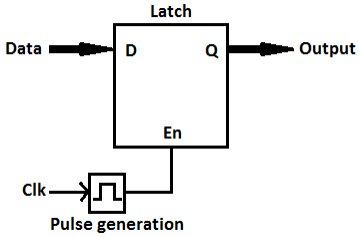

Fig. 2(b) Pulsed latch

Clock Pulse Generator:

Clock can be divided into required clock pulses using the circuit called as clock pulse generator [1]. Clock pulse generator takes clock signal as an input and divides it into clock pulses which are also called as delayed clock pulses. Number of clock pulses generated is dependent on application. In this paper, 8-bit ring counter is demonstrated, thus 8 clock pulses are required. Generation of clock pulses is done using the below circuit.

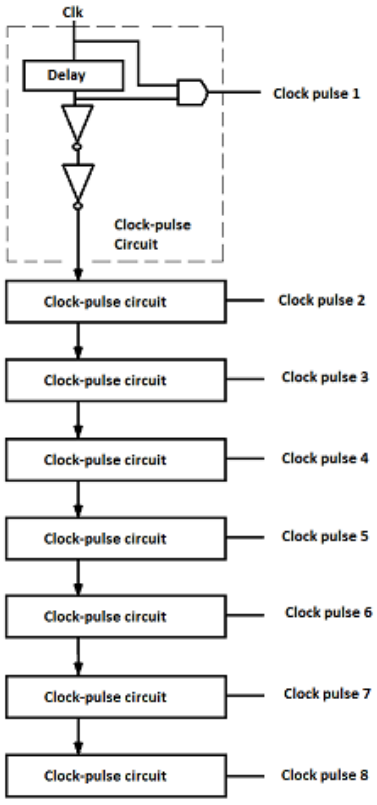

Fig.3(a) Clock pulse generator circuit

Fig.3(b) shows the minimum clock cycle time (T_{CLK}) of the proposed ring counter. T_{CLK} is equal to $T_{CP}+8\times T_{DELAY}$, where T_{CP} is the delay from the rising edge of the clock signal (Clk) to the rising edge of the first pulsed clock signal (clk_pulse_1), and T_{DELAY} is the delay of two neighboring pulsed clock signals [1].

$$T_{CLK} = T_{CP}+8\times T_{DELAY} \quad (1)$$

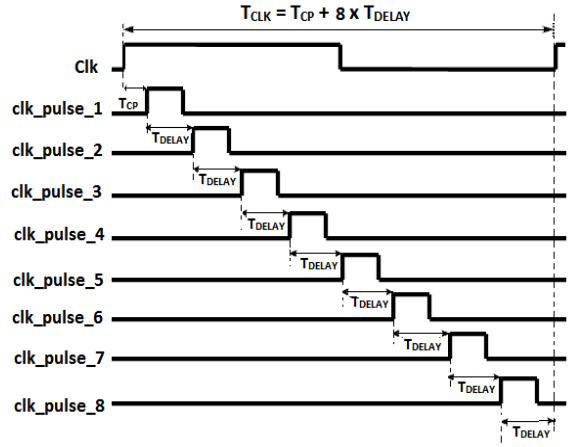

Fig.3(b)Minimum clock cycle time of Ring counter

II. PROPOSED ARCHITECTURE

Fig.4 shows block diagram of proposed ring counter using pulsed latches. 8-bit ring counter can be realized by using 8 D latches, that are connected in series and by giving output of last latch as an input to the first latch. The output of first pulsed latch Q1 is connected as an input to second pulsed latch and so on.

The clock pulses are generated using clock pulse generator circuit. The first pulse generated clk_pulse_1 is given to first D latch, clk_pulse_2 is given to second D latch and so on. For 8-bit ring counter, 8 clock pulses are generated. The generated clock pulses are also called as delayed pulses.

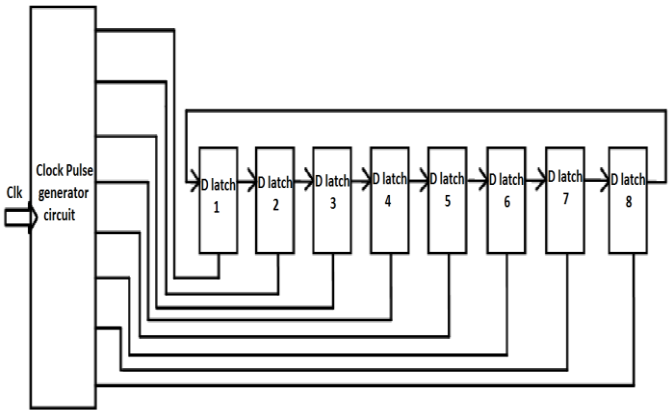

Fig. 4 Block diagram of proposed architecture

III. METHODOLOGY

Pulsed latches are used in proposed architecture. Pulsed latches are considered as an alternative to Flip-flops. They have advantages of flip-flops and latches i.e. they can store data as well as they are faster. Clock pulse generator circuit is used to generate clock pulses or delayed clock pulses, which are used by the pulsed latches.

The proposed design is implemented on Xilinx ISE 17.5 software using Verilog HDL language. VHDL or Verilog could be used to design the proposed architecture.

IV. RESULTS

Simulation:

Fig. 5(a) shows the RTL schematic of the clock pulse generator circuit. As shown in the block diagram, the input to the circuit is clock pulse and outputs are 8 clock pulses generated. Fig. 5(b) shows the simulation waveforms of the clock pulse generator circuits. Each clock signal period is divided into 8 equal clock pulses.

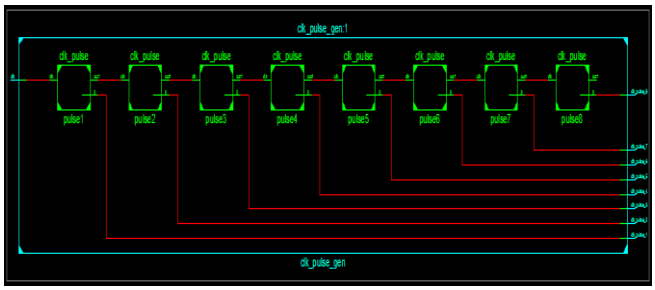

Fig. 5(a) RTL schematic of clock pulse generator circuit

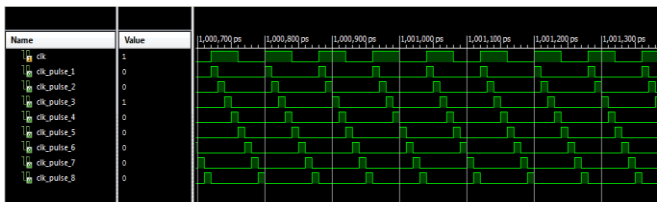

Fig. 5(b) Simulation waveforms of clock pulse generator circuit

Fig. 6(a) shows the output waveform of ring counter using pulsed latches. As the architecture is designed for 8 bits, the sequence repeats after every 8 clock pulses. Initially, the output is set to '10000000', thus the same sequence is '10000000' repeated after 8 clock pulses. Fig. 6(b) shows the RTL schematic of proposed 8-bit ring counter using pulsed latches.

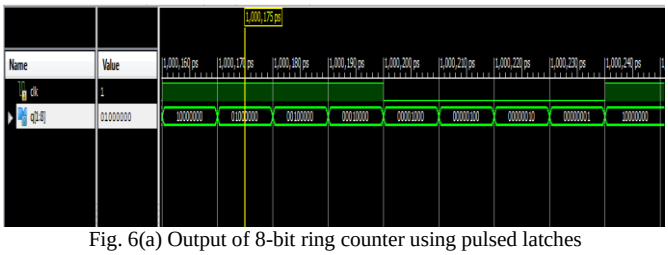

Fig. 6(a) Output of 8-bit ring counter using pulsed latches

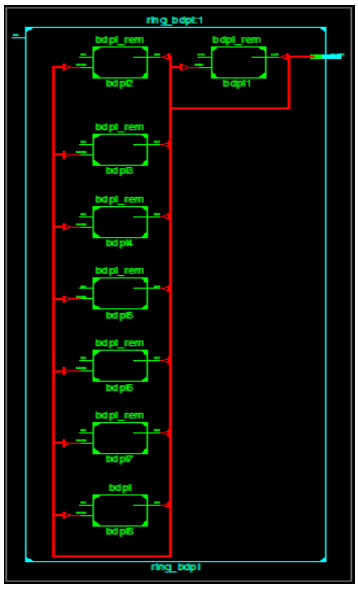

Fig. 6(b) RTL schematic of 8-bit ring counter using pulsed latches

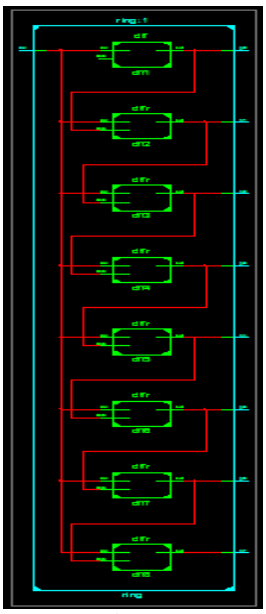

Fig. 6(c) RTL schematic of conventional ring counter

V. TIME ANALYSIS

Table II
Time analysis of conventional ring counter

Phases	Time in seconds
Phase 1	48
Phase 2	48
Phase 3	49
Phase 4	58

Phases	Time in seconds
Phase 5	58
Phase 6	58
Phase 7	58
Phase 8	58
Phase 9	58
Total Real time to Router completion	58
Total CPU time to Router completion	50

Table III
Time analysis of ring counter using pulsed latches

Phases	Time in seconds
Phase 1	37
Phase 2	38
Phase 3	38
Phase 4	48
Phase 5	48
Phase 6	48
Phase 7	48
Phase 8	48
Phase 9	48
Total Real time to Router completion	48
Total CPU time to Router completion	44

Time Comparison of Conventional Ring Counter vs Ring Counter using Pulsed latches

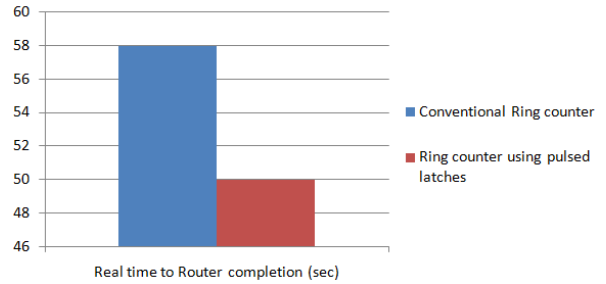

Fig. 7(a) Real time to router completion comparison (Conventional RC vs RC using PLs)

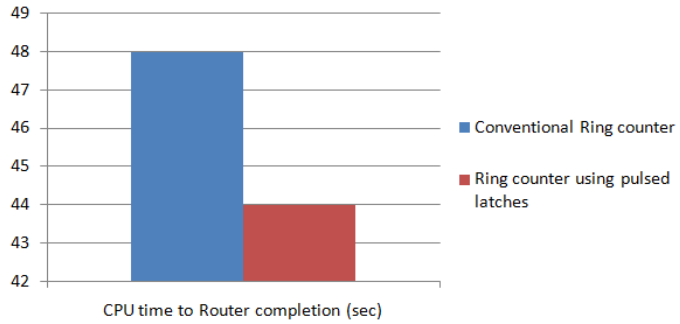

Fig. 7(b) CPU time to router completion comparison (Conventional RC vs RC using PLs)

VI. CONCLUSION

The proposed architecture uses pulsed latches instead of flip flops to construct 8-bit ring counter. Ring counter can be further used in many applications like to count data, in frequency divider circuit, to design LFSRs and Alternating step generators [10] so on. Pulsed latches consume less time to operate compared to flip flops. Pulsed latches can be used in several applications like to design shift register [3], bidirectional shift register [1], to design Johnson counter etc so that the circuit consume less time. Sometimes problem that is faced by using pulsed latches is that they cause timing problem as they face race condition. One solution for this problem is to use multiple non-overlapping delay pulse-latch and using additional short-term storage latches. To reduce area and power consumption, pulsed latch is a good option. But as the number of bits increase, the number of latches also increases. This problem can be solved by using Static differential Sense Amplification Shared Pulse Latch (SSASPL) which can be considered as future work.

REFERENCES

[1] Ki-Chan Woo, Hyeong-Ju Kang, and Byung-Do Yang, "Area-efficient bidirectional shift-registers using bidirectional pulsed-latches", *IEEE Transactions on Circuits and Systems II: Express Briefs*, 2019.

[2] B.-D. Yang, "Low-Power and Area-Efficient Shift Register Using Pulsed Latches", *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 62, no. 6, pp. 1564–1571, Jun. 2015.

[3] Roshan R Chavhan , Dr. Rajesh Thakare "Implementation of Shift Register using pulsed latches", *International Conference on Innovations in Information, Embedded and Communication Systems (ICIIECS)*, 2017.

[4] S. Shibatani, A. H. C. li, "Pulse latch approach reduce dynamic power", *EEtimes online*, 2006

[5] Tanushree Doi, Vandana Niranjan "Low power and high performance ring counter using pulsed latch technique", *2016 International Conference on Micro-Electronics and Telecommunication Engineering*

[6] Seungwhun Paik, Gi-Joon Nam, Youngsoo Shin "Implementation of Pulsed-Latch and Pulsed-Register Circuits to Minimize Clocking Power", *2011 IEEE/ACM International Conference on Computer-Aided Design (ICCAD)*, 7-10 Nov. 2011

[7] H. Li, M. Chen, and K. Ho, "System and method of replacing flip-flops with pulsed latches in circuit designs," *U.S. Patent 7694242 B1*, April 2010

[8] Youngsoo Shin, Seungwhun Paik "Pulsed-Latch Circuits: A New Dimension in ASIC Design", *IEEE Design & Test of Computers*, Volume: 28, Issue: 6, Nov.-Dec. 2011.

[9] Y.-L. Chuang et al., ''Pulsed-Latch Aware Placement for Timing-Integrity Optimization,'' *Proc. 47th Design Automation Conf. (DAC 10), ACM Press*, 2010, pp. 280-285.

[10] Shine P James , Sudhish N George , Deepthi P P "An Audio Encryption Technique based on LFSR based Alternating Step Generator", *2014 IEEE International Conference on Electronics, Computing and Communication Technologies (CONECCT)*.