Design of Three Stage Comparator for High Speed Conversion using CMOS Technology

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*Abstract -***As the scale of integration keeps growing, more and more sophisticated signal processing systems are being implemented on a VLSI chip. These signal processing applications not only demand great computation capacity but also require less computation delay. While performance and area remain to be two major design goals, delay factor has also become a critical concern in today's VLSI system design.**

We have designed a three-stage Voltage Comparator The first preamplifying stage amplifies the input signal to improve Comparator sensitivity . The output of the first stage is fed to the decision making stage which compares the two signals. Then the differential output of the second stage is fed to the output buffer stage (third stage) of the CMOS inverter for overall gain improvement.

Keywords- Comparator, Cmos, Tanner EDA, Latch

1 . INTRODUCTION

A Voltage Comparator is a device which compares two signal levels and outputs a digital signal based on the result of the comparison. The proposed Comparator will be designed to provide high speed and reduced delay to be used in fast analog to digital conversion. The proposed Comparator is designed using CMOS (complemented metal-oxide–semiconductor) technology which are high in noise immunity & low static power consumption. It also allows a high density of logic functions on a chip and
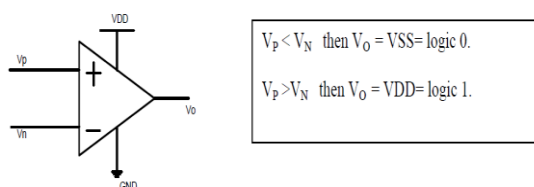

Fig. 1.1 Circuit Symbol of a Comparator

is the reason that CMOS become the most used technology to be implemented in VLSI chips.Designing and simulation of the proposed work will be carried out using Tanner Tools. Tanner Tools gives technologically robust products

& provides designer productivity needed to quickly & accurately cycle through the design process at a much lower cost than with other tools. There are three stages in this Comparator shown in figure 1.2. The pre-amplifier, a positive feedback or decision making stage and an output buffer stage. The pre-amp stage amplifies the input signal to improve the Comparator sensitivity and isolates the input of the Comparator from switching noise coming from the positive feedback stage i.e. kick back noise effect. This noise effect is reduced by using Latched based Comparator. The positive feedback stage is used to determine which of the input signal is larger. The output buffer amplifies this information and outputs a digital signal. Designing a Comparator can begin with considering input common mode range, power dissipation, propagation delay and Comparator gain.
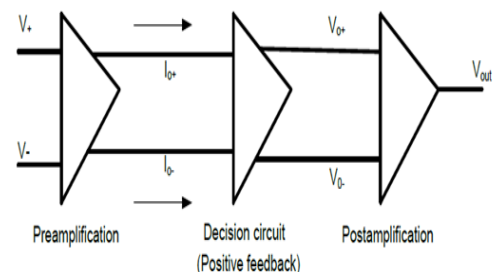

Fig. 1.2 Block Diagram of Comparator

2. CIRCUIT IMPLEMENTATION

In this the first stage is the preamplifier stage which amplifies the input signal to improve the Comparator sensitivity and isolate input of the Comparator from switching noise coming from positive feedback stage .The output of the first stage is fed to the decision making stage (second stage). In the decision making stage the Comparator first makes the comparison for the two signal levels and gives the output accordingly .then the output of the second stage is fed to the gain stage(third stage) of the CMOS inverter .This stage improves the overall gain of circuit.

2.1. Differential Amplifier Input Stage

This circuit is a differential amplifier with active loads. The sizes of NMOS_7 NMOS_8 and NMOS_9 are set by considering the diff-amp trans-conductance and the input resistance. The trans-conductance sets the gain of the stage, while the input capacitance of the Comparator is determined by the size of NMOS_7 NMOS_8 and NMOS_9. We will concentrate on speed in the design, and therefore we will set the channel lengths of the MOSFETs to100nm.
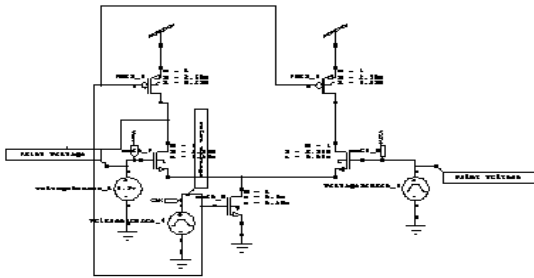

Fig 2.1 Preamplification Stage

2.2 Decision-Making Stage

The decision circuit is the heart of the Comparator and should be capable of discriminating mV level signals. We should also be able to design the circuit with some hysteresis for use in rejecting noise on a signal. The circuit uses positive feedback from the cross-gate connection of NMOS_1, NMOS_2, NMOS_3, NMOS_4, NMOS_5 and NMOS_6 to increase the gain of the decision element.
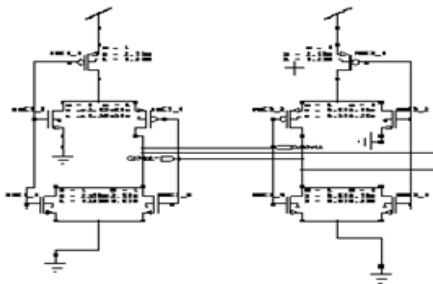

Fig 2.2 Decision Stage

2.3. Output buffer Stage

The final component in our Comparator design is the output buffer or post-amplifier. The main purpose of the output buffer is to convert the output of the decision circuit into a logic signal (i.e., 0 or 5V). The output buffer should accept a differential input signal and not have slew-rate limitations.
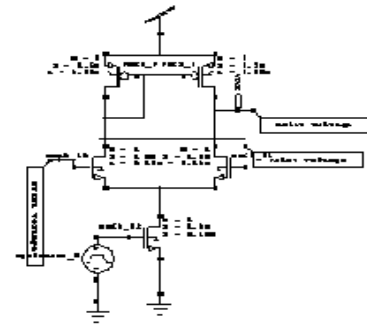

Fig.2.3 Output Buffer Stage

3. TRANSIENT ANALYSIS

Transient analysis is done in Tanner environment where inputs are applied at input differential stage and the outputs of this stage are then applied to dicision making stage.Buffer stage provides single ended output of the two outputs obtained from decision making stage.

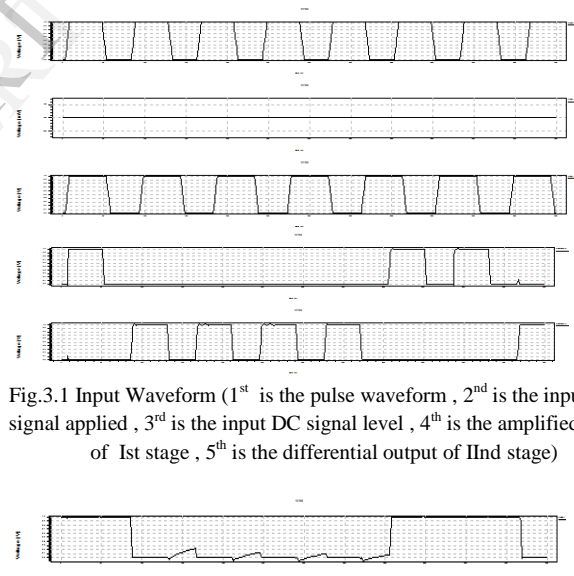Figure 3.1 and 3.2 shows Transient behavior of three stage Comparator.

Fig.3.1 Input Waveform (1st is the pulse waveform , 2nd is the input clock signal applied , 3rd is the input DC signal level , 4th is the amplified output of Ist stage , 5th is the differential output of IInd stage)

Fig.3.2 Output Waveform (Final waveform)

4. RESULTS

The results of a three stage Comparator are derived and are shown in Table.

Total delay is 89ns, rise time is 262ns, fall time 1.8ns and average time is 1ns are calculated in Tanner environment.

Table I

Delay Time (ns)	Rise Time (ns)	Fall Time (ns)	Average Time (ns)
89	262	1.8	1

ACKNOWLEDGEMENT

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